Ida Laboratory
Ultra Low Power Devices & Circuits

Steep Subthreshold Slope PN-Body Tied SOI-FET for Ultralow Power LSI, Sensor, and Neuromorphic Chip

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Outline

Background

PN-Body Tied SOI-FET

- Device structure
- I_d–V_g, I_d–V_d characteristics
- Scaling of PNBT SOI-FET
- Transient characteristics

Dual Gate PN-Body Tied SOI-FET

- Turn-off characteristics
- Application to neuromorphic chip

Compact Modeling of PNBT SOI-FET (& thyristor-like devices)

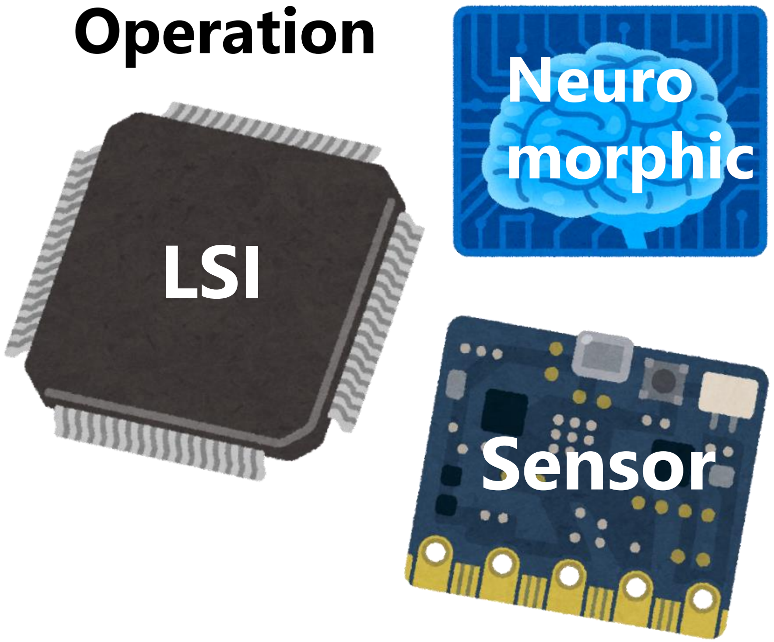
Summary

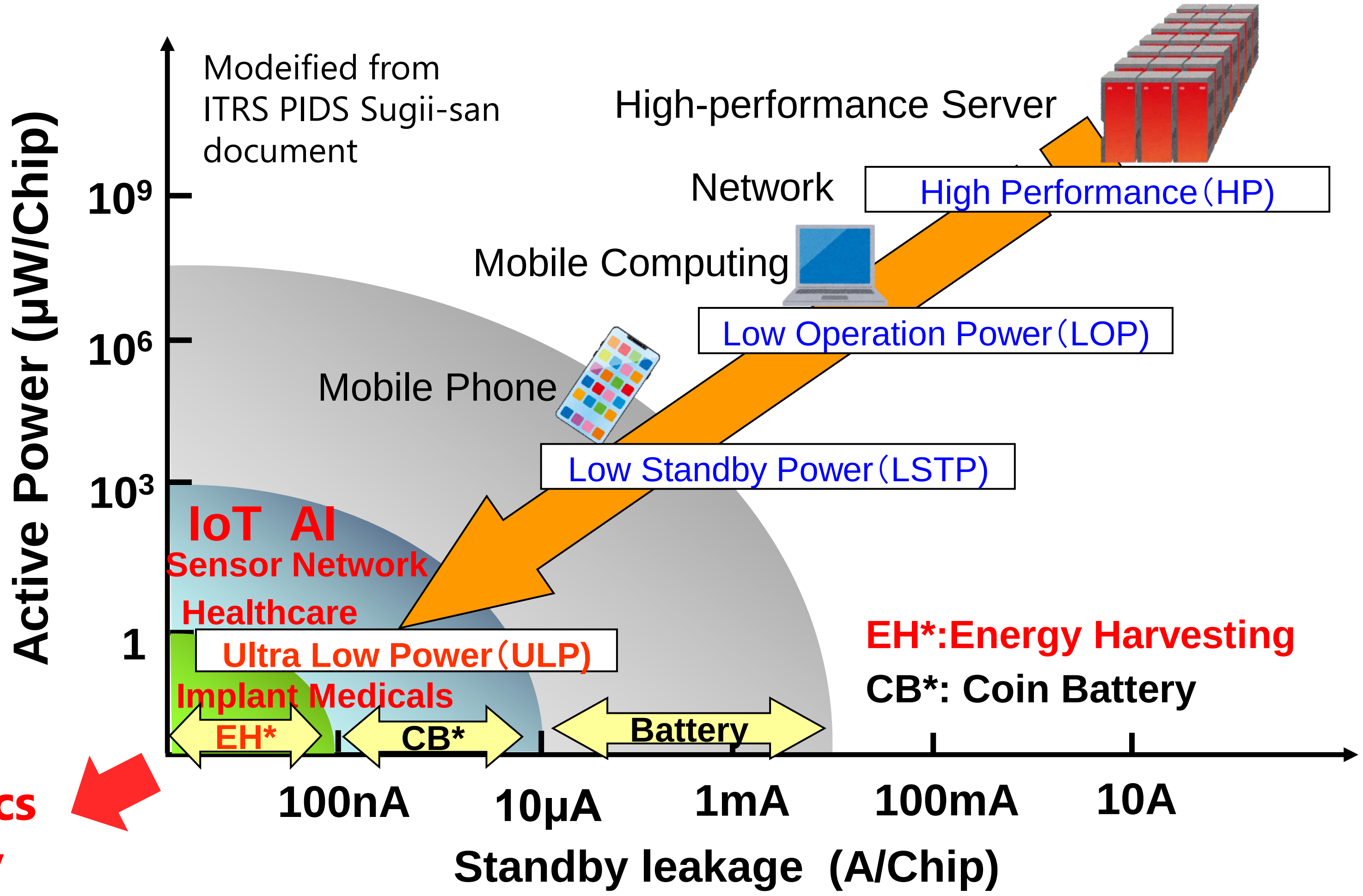
Necessity of ultralow power devices

Ultralow Power (Active<1 µ – 1 mW, Standby < 0.1 nA ⇒ µ & nW Electronics)

Ultimately, powered by energy harvesting （e.g. RF wave, Human heat, Vibration）

Ultralow Power Operation





Micro & Nano Watt Electronics for Next-Generation Society

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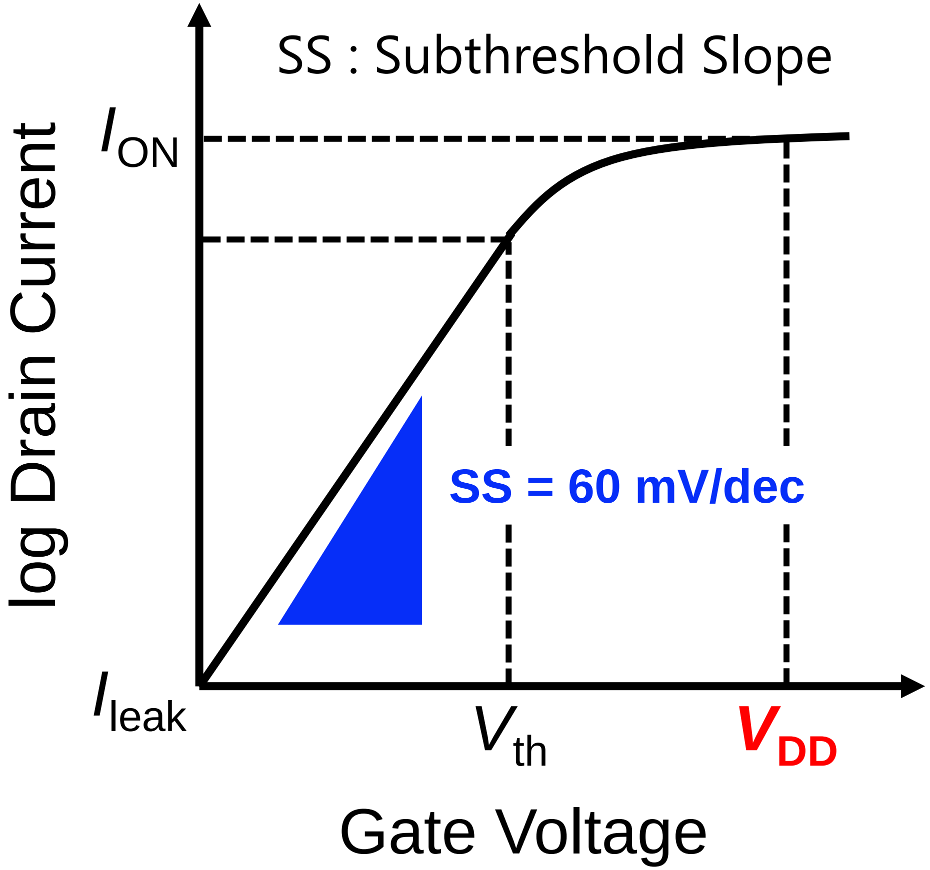
Subthreshold slope limitation of conventional MOSFET



Power consumption of LSI

$$P_{\text{active}} \propto f \cdot C_{\text{load}} \cdot V_{\text{DD}}^2$$

$$P_{\text{standby}} \propto I_{\text{leak}} \cdot V_{\text{DD}}$$

Conventional MOSFET
fundamental SS limitation (room temp.)

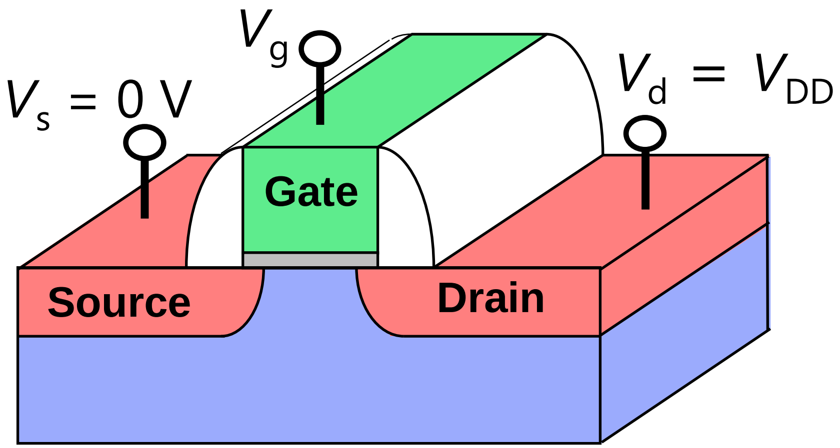
$$S = n\frac{kT}{q}\ln 10 \approx \underline{60\,(\text{mV/dec})}$$

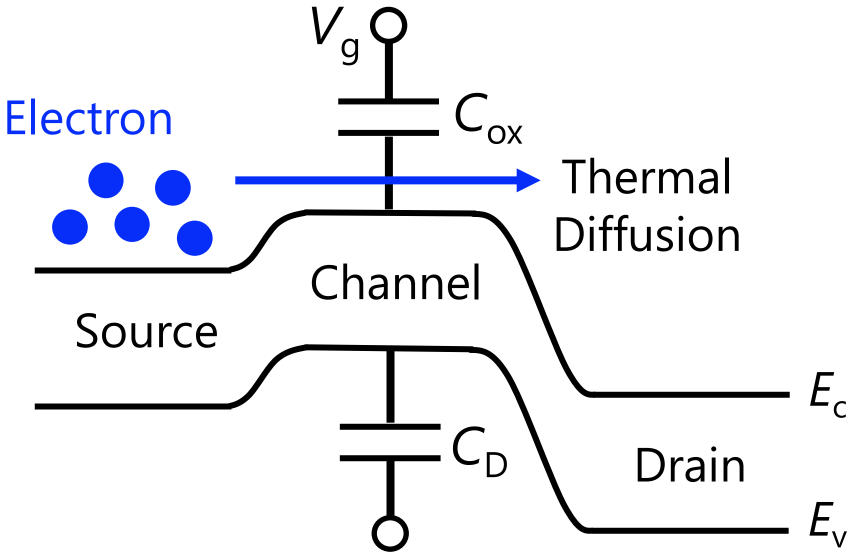
$$n = 1 + \frac{C_D}{C_{OX}}$$

Theoretical Limit

Fundamental SS limitation of conventional MOSFET is determined by thermal diffusion

Subthreshold slope limitation of conventional MOSFET





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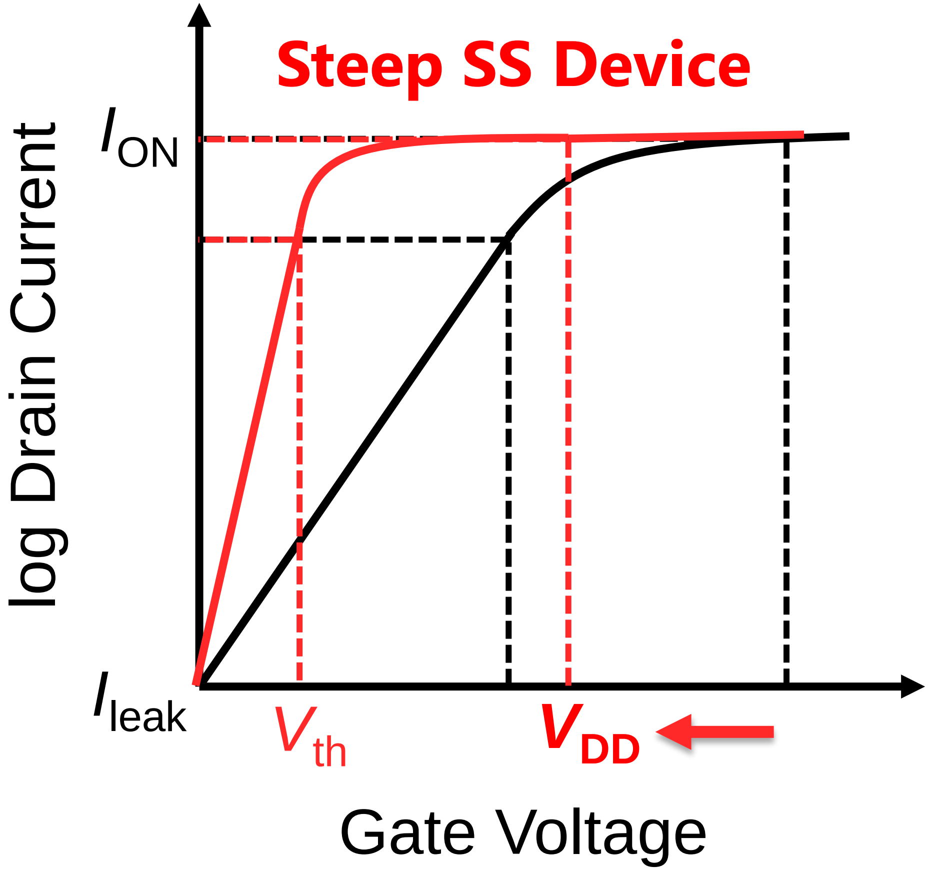
Steep subthreshold slope device



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Theoretical Limit

Steep Subthreshold Slope (SS) Device

Different switching mechanism (Not thermal diffusion)

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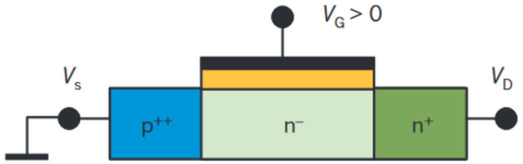
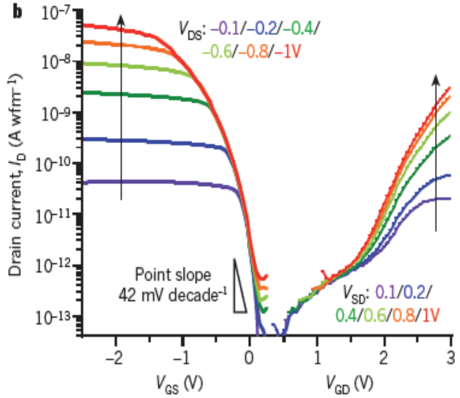
Candidates of steep SS device

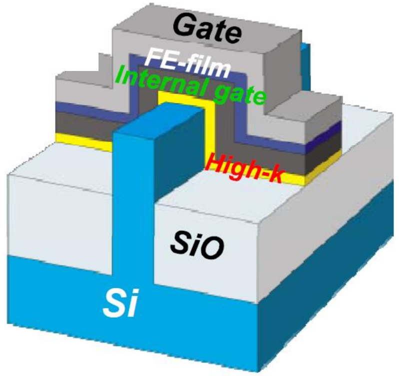
Tunnel FET

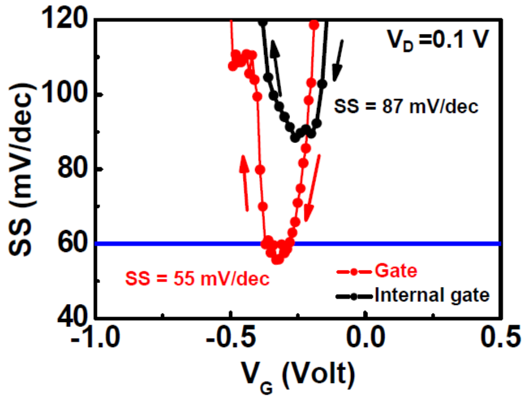




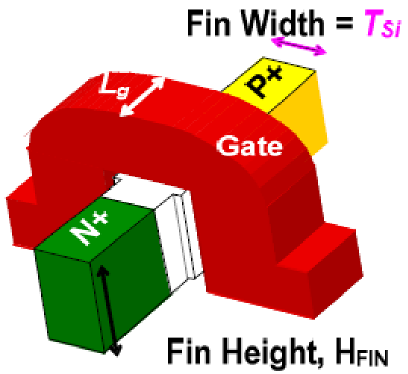
A. M. Ionescu *et al.*, *Nature* 2011.

Negative Capacitance FET



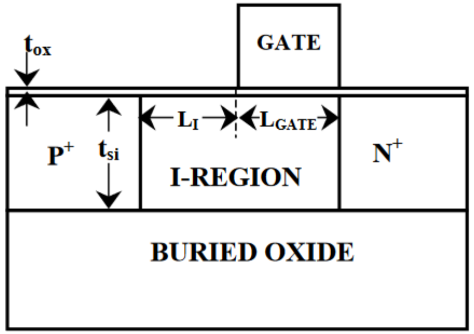


K.-S. Li *et al.*, *IEDM* 2015.



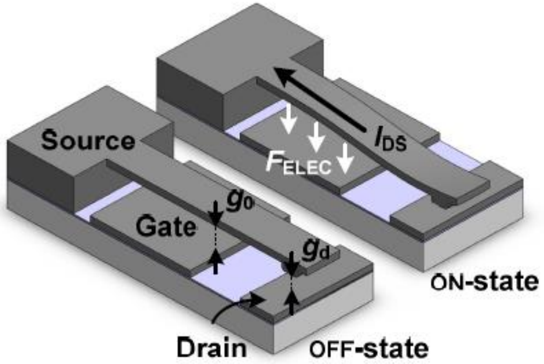
Feedback FET

A. Padilla *et al.*, *IEDM* 2008.



Impact ionization MOS

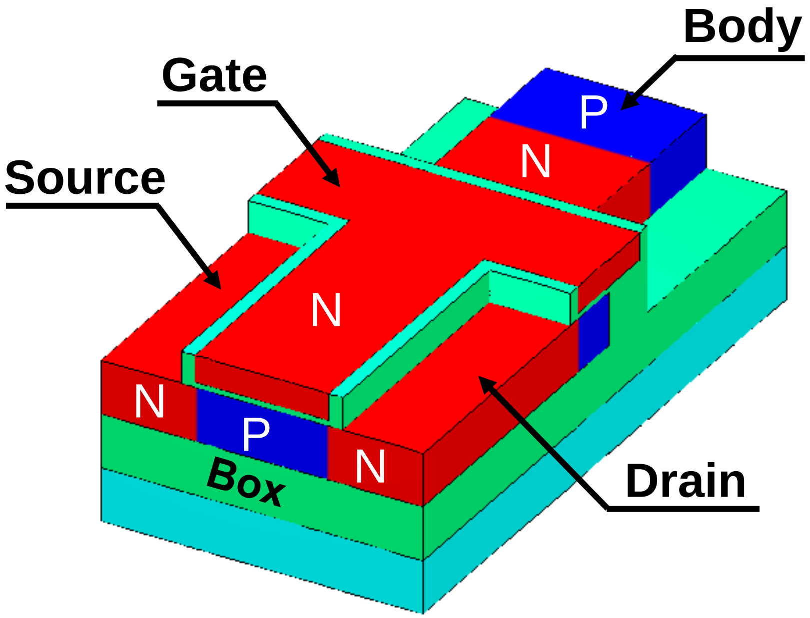
K. Gopalakrishnan *et al.*, *IEDM* 2002.



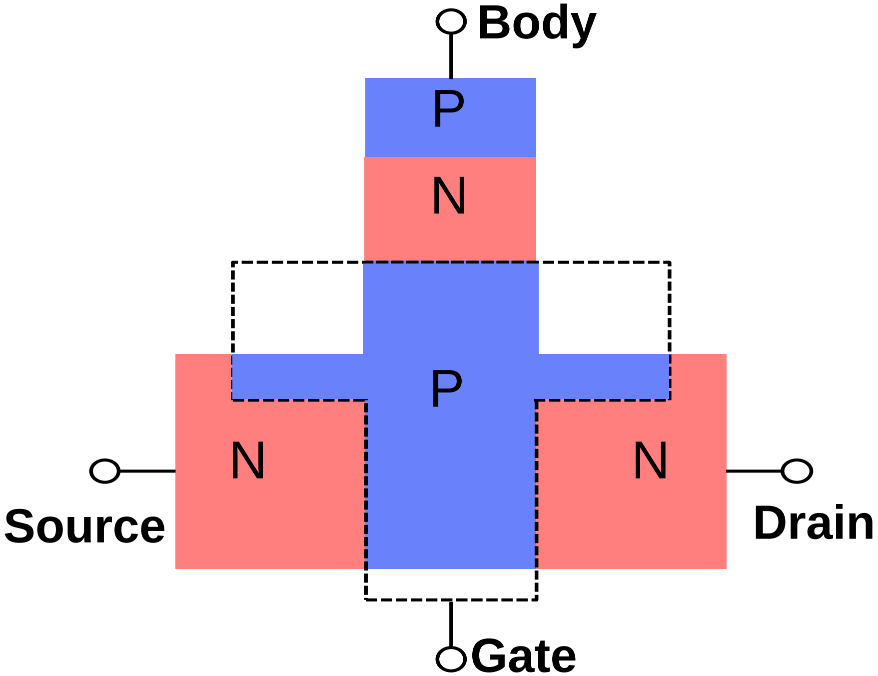
MEMS Logic Switch

T.-J. K. Liu *et al.*, *IEDM* 2011.

PN-Body Tied (PNBT) SOI-FET



Bird's eye view

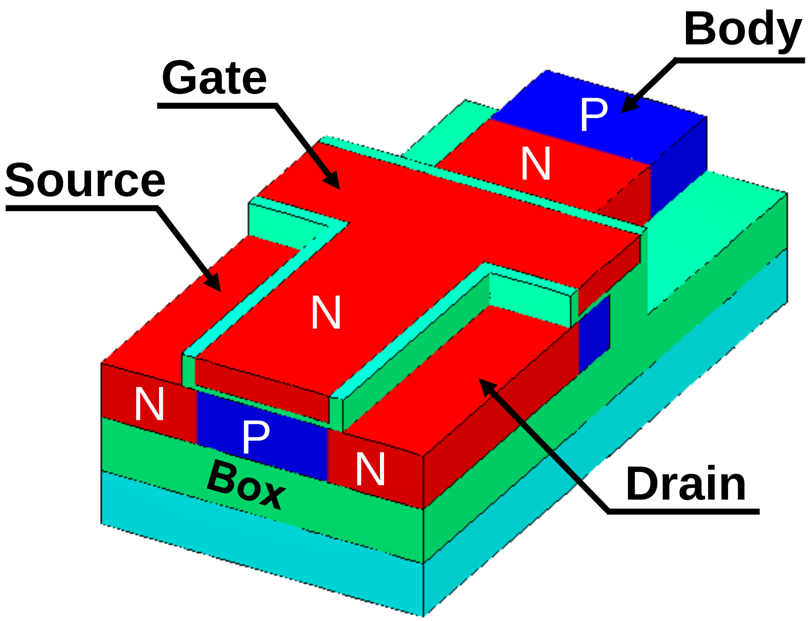


Top view

n-channel PNBT SOI-FET

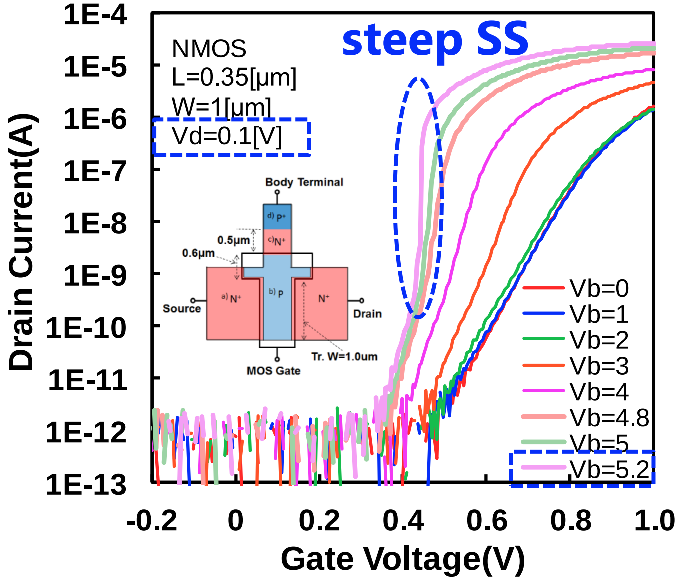
We proposed PN-Body Tied (PNBT) SOI-FET which has a **symmetry S/D** and demonstrated that N-channel PNBT SOI-FET has super-steep SS with **low drain voltage V_d (= 0.1 V)**

PN-Body Tied (PNBT) SOI-FET

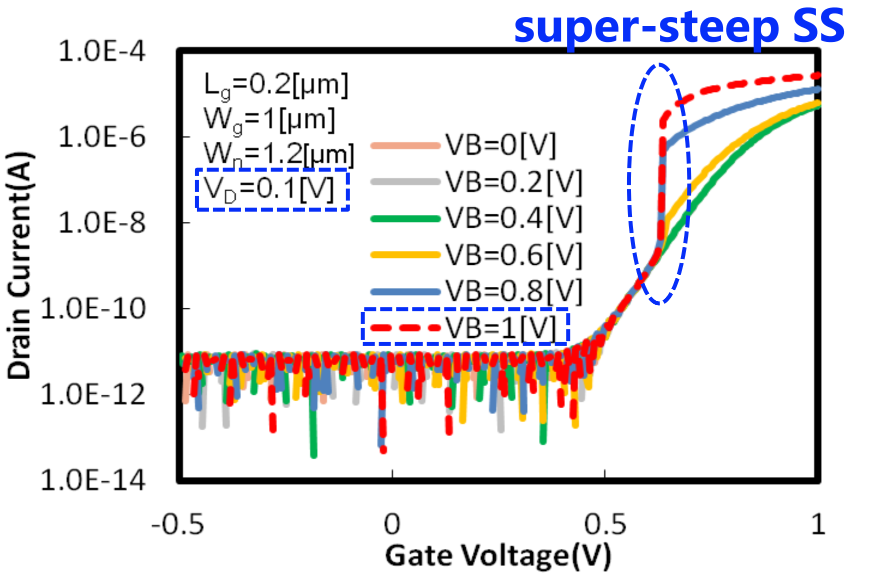


n-channel PNBT SOI-FET

J. Ida, T. Mori, *et al.*, *IEDM* 2015

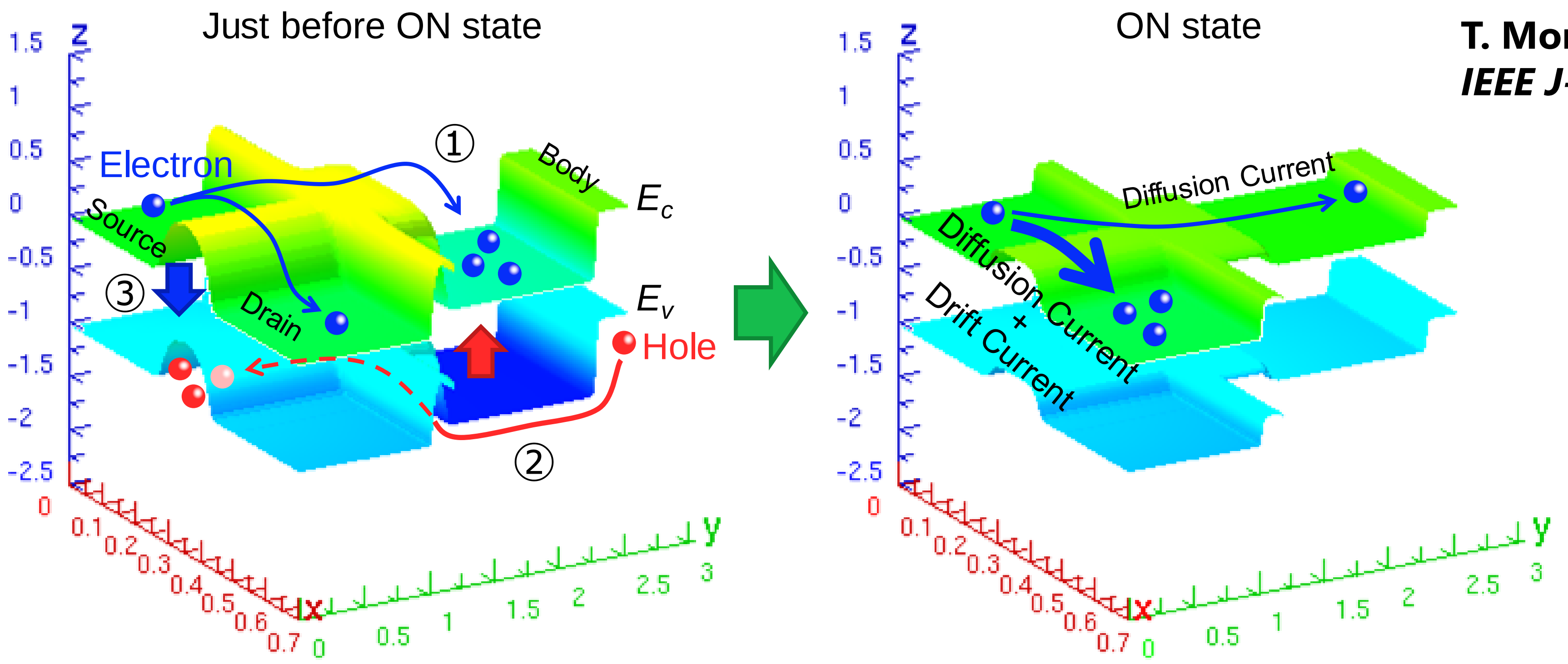


T. Yoshida, J. Ida *et al.*, *S3S* 2016



We proposed PN-Body Tied (PNBT) SOI-FET which has a **symmetry S/D** and demonstrated that N-channel PNBT SOI-FET has super-steep SS with **low drain voltage V_d (= 0.1 V)**

Operation principle of PNBT SOI-FET (n-channel)



T. Mori and J. Ida,
***IEEE J-EDS*, Oct. 2018.**

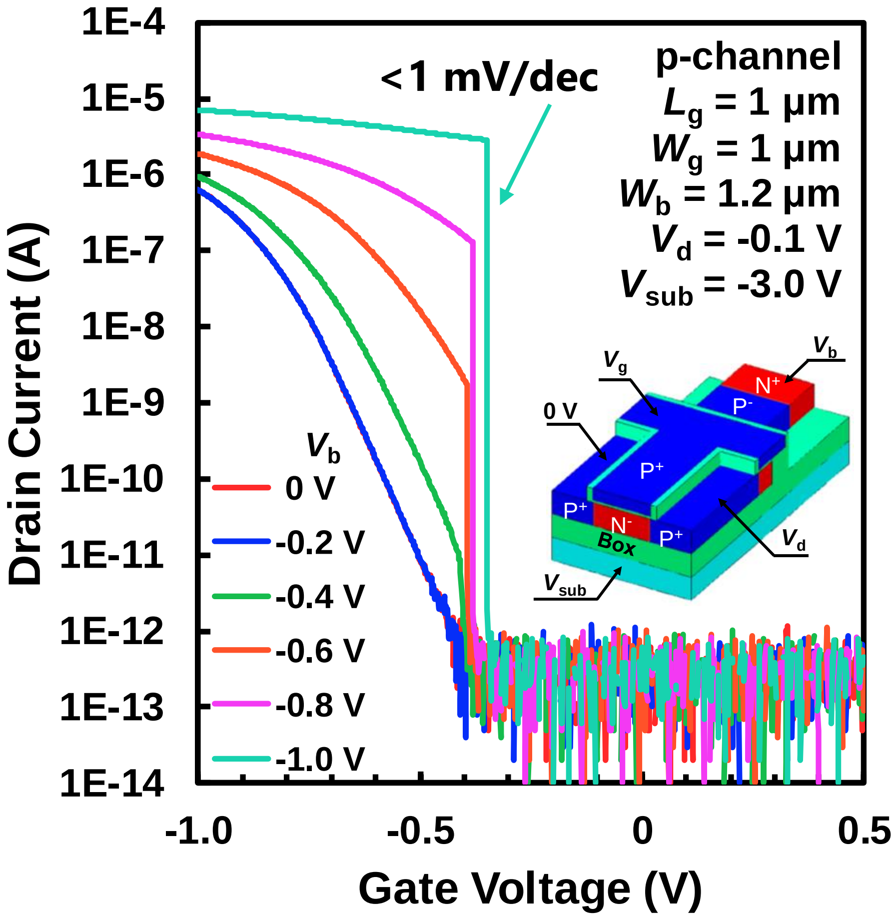
1. Electrons diffuse from source to body
2. Electrons lower barrier height for hole injection from body to channel region
3. Accumulated holes in channel region lower barrier height for electron injection from source to body

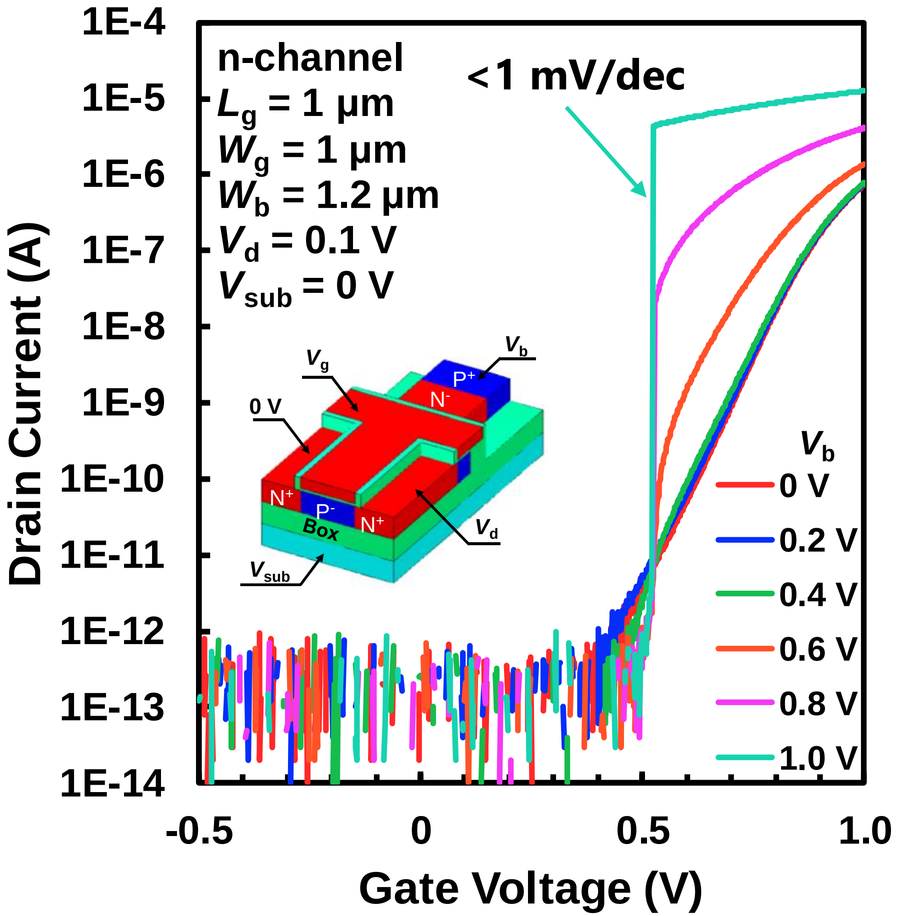
Mechanism is similar to thyristor-like devices

e.g.
・Field effect diode AA. Salman *et al.*, *IEDM* 2006.
・Feedback FET A. Padilla *et al.*, *IEDM* 2008.
・Z^2-FET J. Wan *et al.*, *Solid State Electron.* 2013.

I_d–V_g characteristics of p/n-channel PNBT SOI-FET

T. Mori and J. Ida, *IEEE J-EDS*, Oct. 2018.





Super-steep SS (<1 mV/dec) appears in both devices keeping low I_{off} (V_b>0.6 V)

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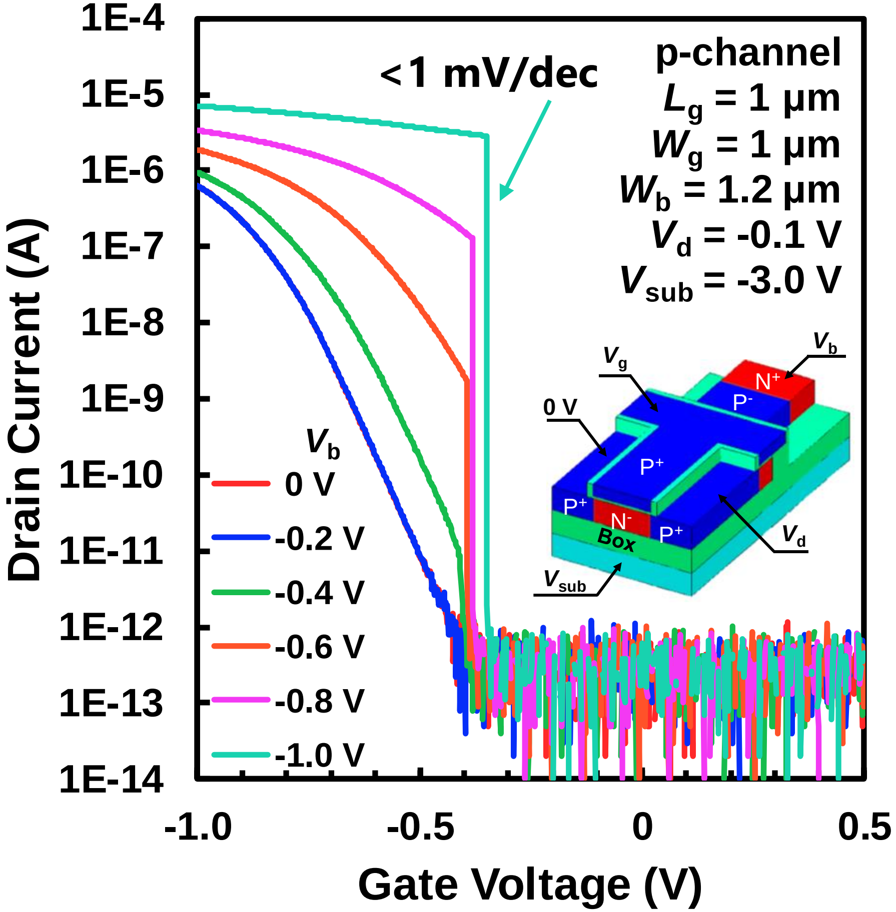
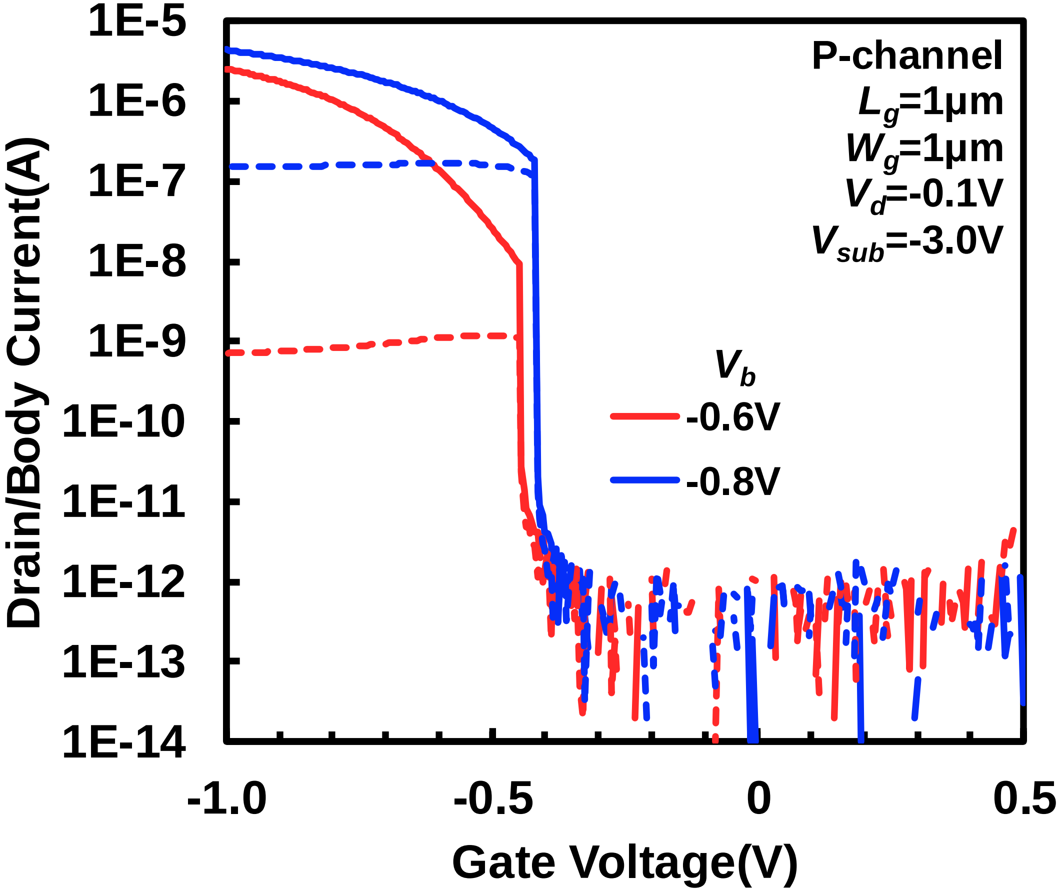
I_d–V_g characteristics of p/n-channel PNBT SOI-FET



Super-steep SS (<1 mV/dec) appears in both devices keeping low I_{off} (V_b>0.6 V)

solid line: I_d, dotted line: I_b



I_b is lower than I_d

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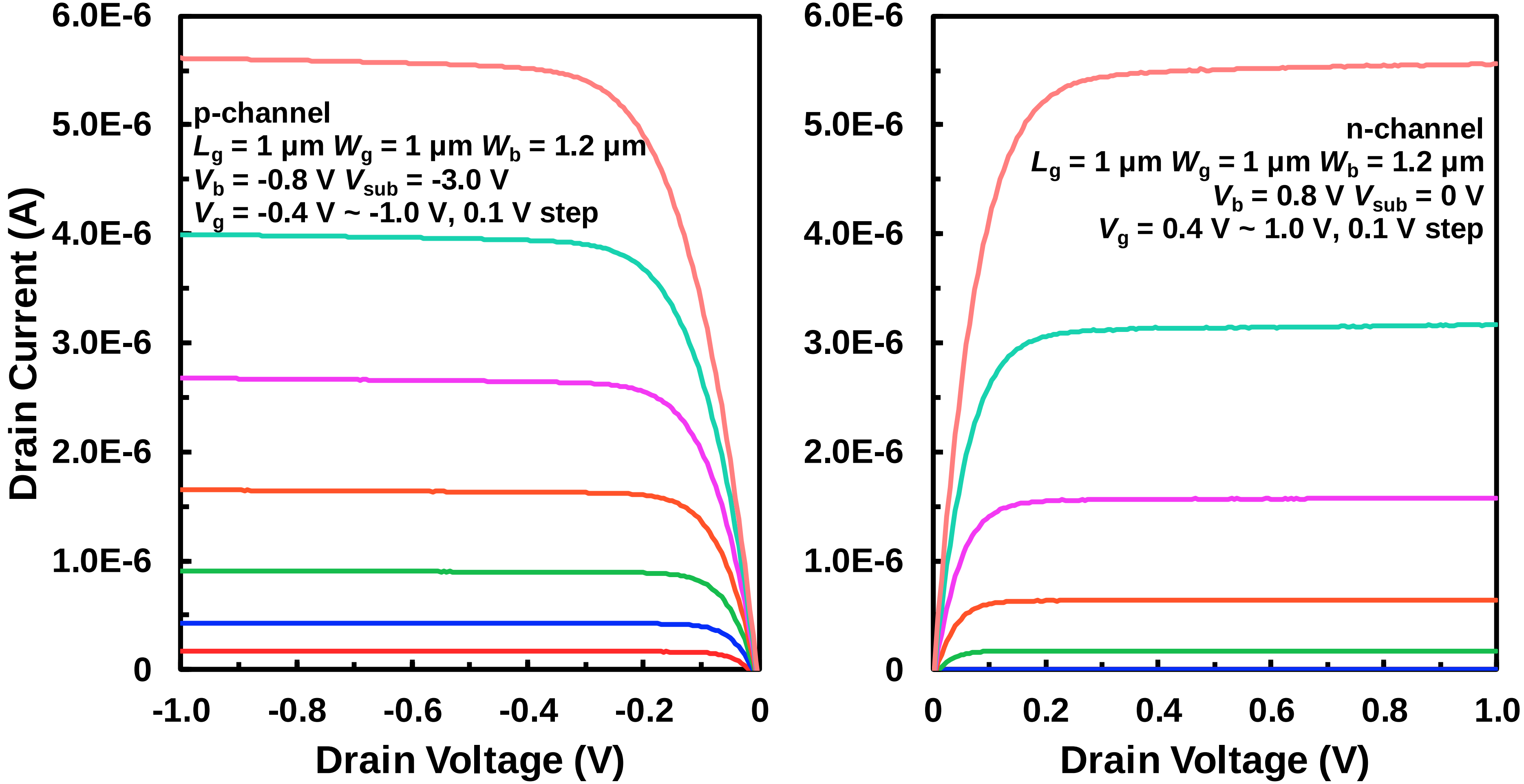
I_d–V_d characteristics of p/n-channel PNBT SOI-FET

T. Mori and J. Ida, *IEEE J-EDS*, Oct. 2018.



PNBT SOI-FET has realized

both super-steep SS and good I_d-V_d characteristic

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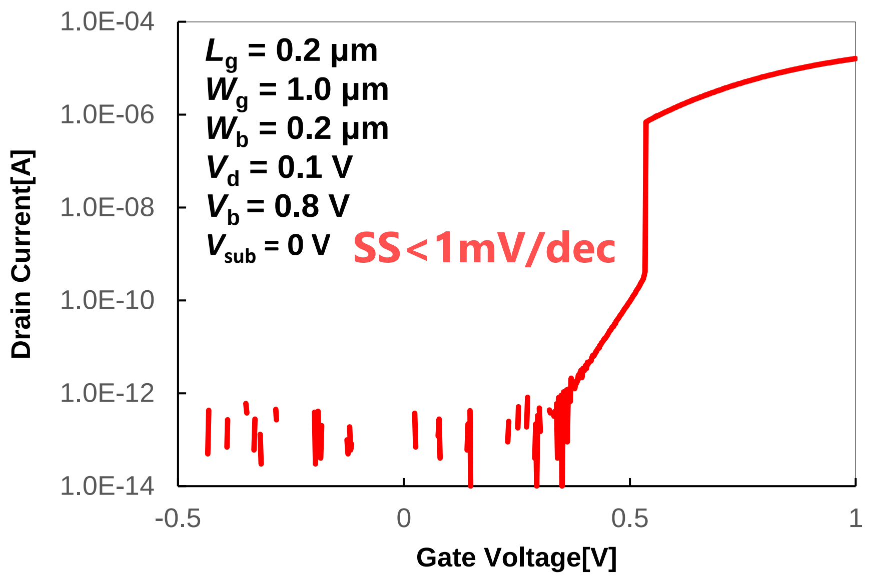
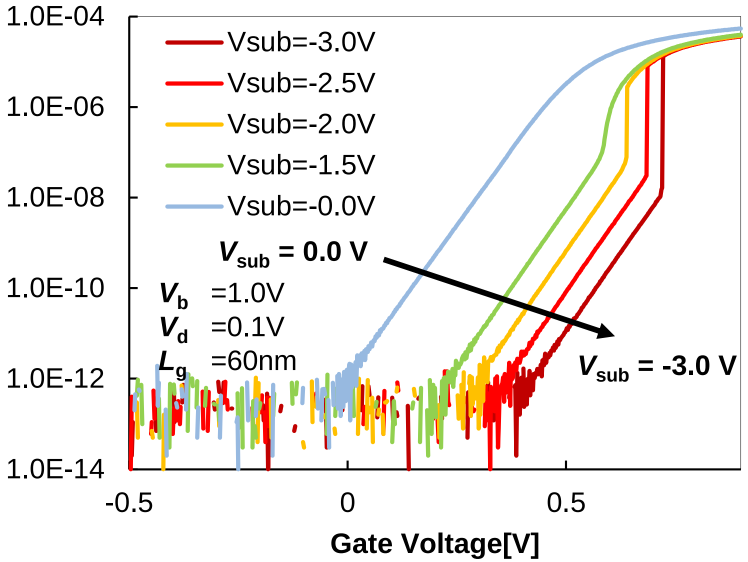
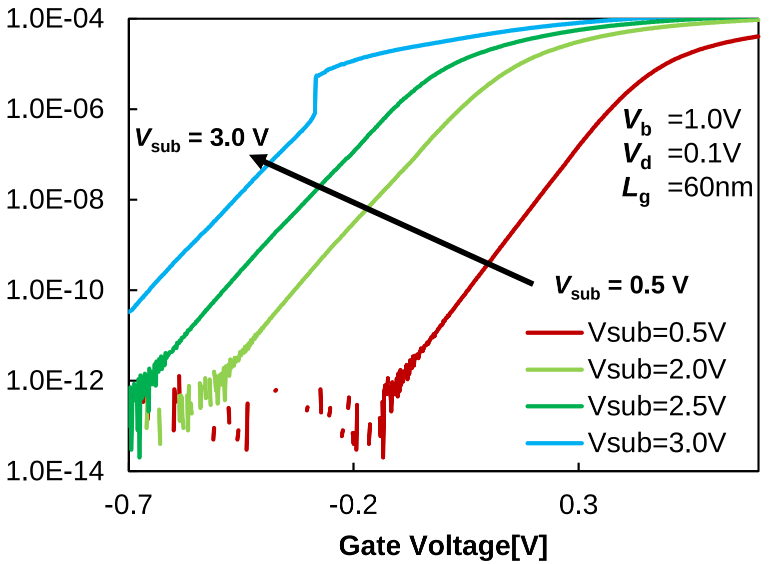
Scaling of PNBT SOI-FET



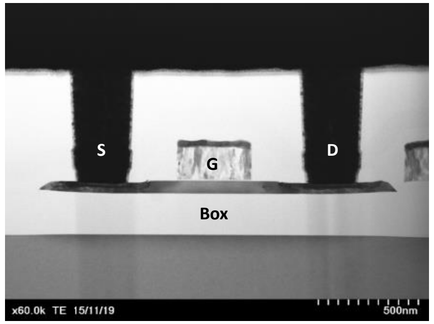




K .Daimatsu, J. Ida, *et al.*, *ICTA* 2019

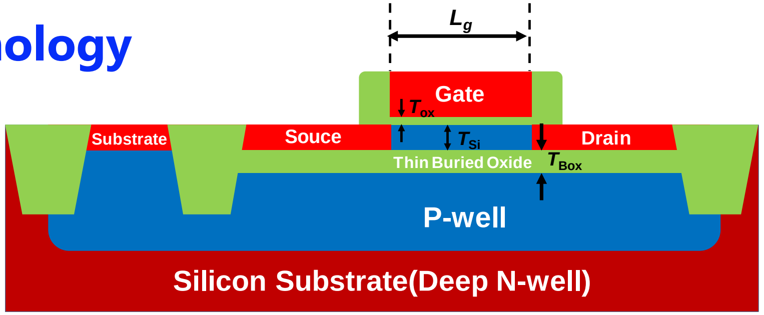
Lapis Semiconductor
200 nm SOI Technology

L_g = 200 nm
T_{ox} = 4.4 nm
T_{Si} = 40 nm
T_{Box} = 200 nm



Renesas Electronics
65 nm thin Box FD-SOI Technology

L_g = 60 nm
T_{ox} = 2 nm
T_{Si} = 12 nm
T_{Box} = 10 nm



PNBT SOI-FET can operate at 65 nm thin Box FD-SOI Technology.

We need more study about scaling limit…

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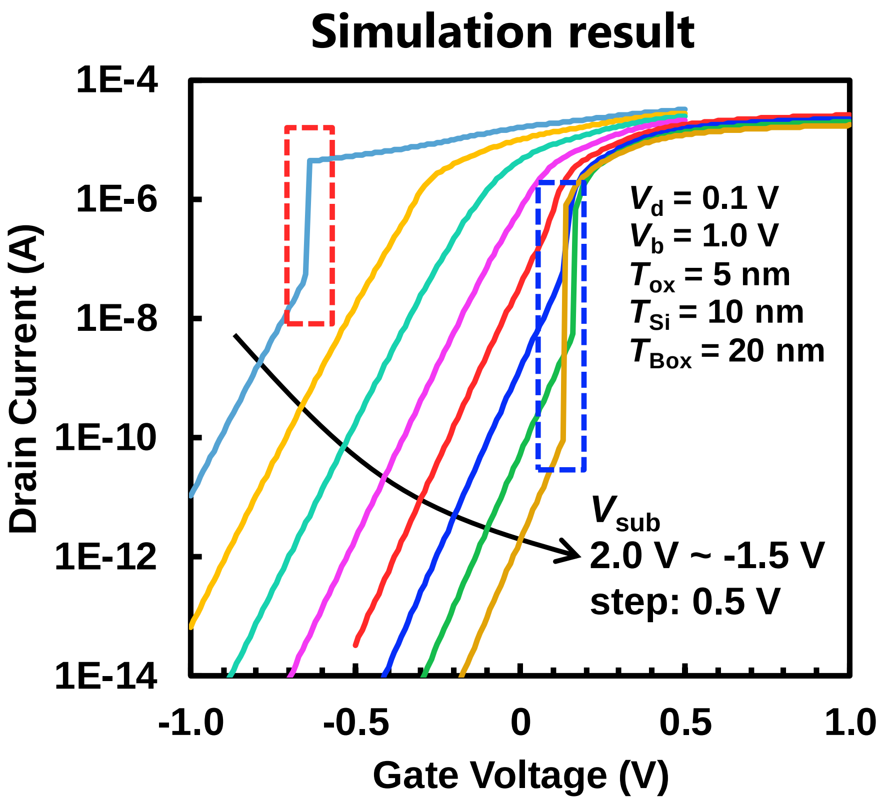
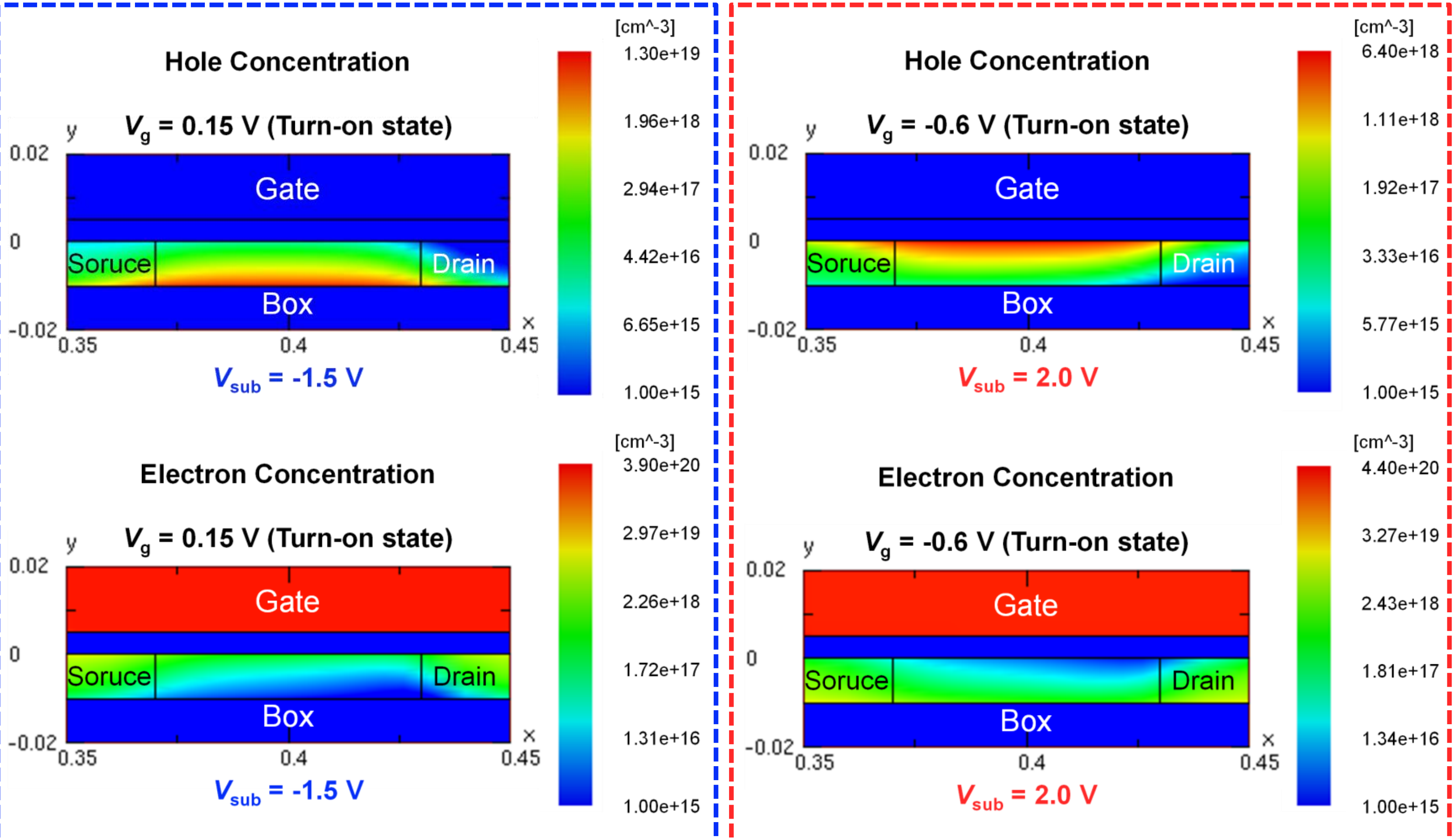
Difference of operation mode on thin Box FD-SOI

T. Mori, J. Ida, *et al.*, *VLSI-TSA* 2020.



Operation mode is different

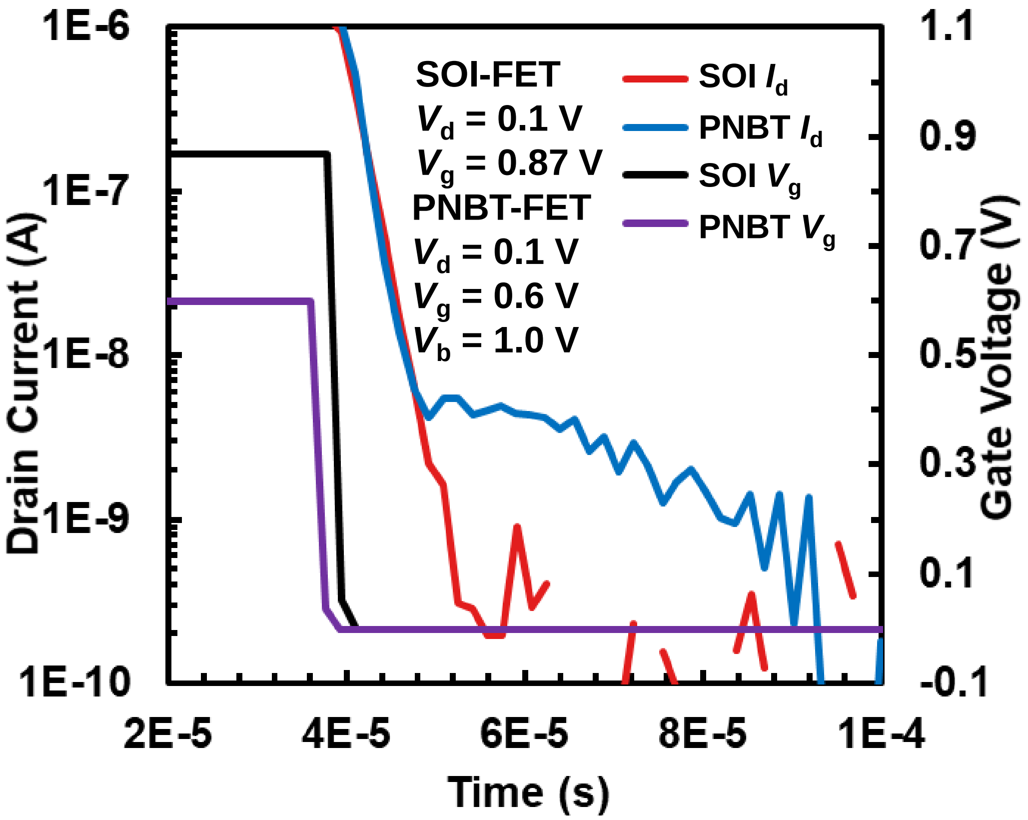


Holes accumulate on **Box** side and electrons flow on **gate** side.

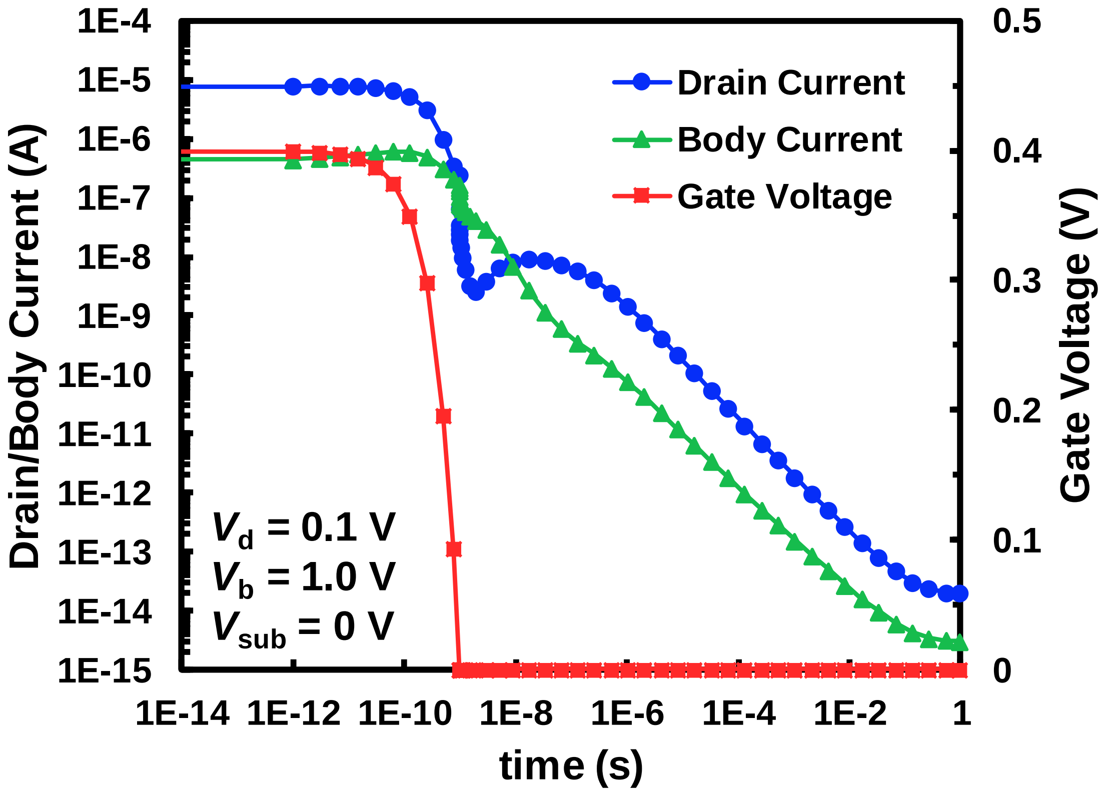
Holes accumulate on **Gate** side and electrons flow on **Box** side.

Transient characteristics of PNBT SOI-FET

Turn-off (Measurement)



Turn-off (Simulation)



T. Mori, J. Ida, *et al.*, *IEICE Trans. on Elec.*, Oct. 2020.

Device shows long-term leakage current upon turn-off because of accumulation carriers.

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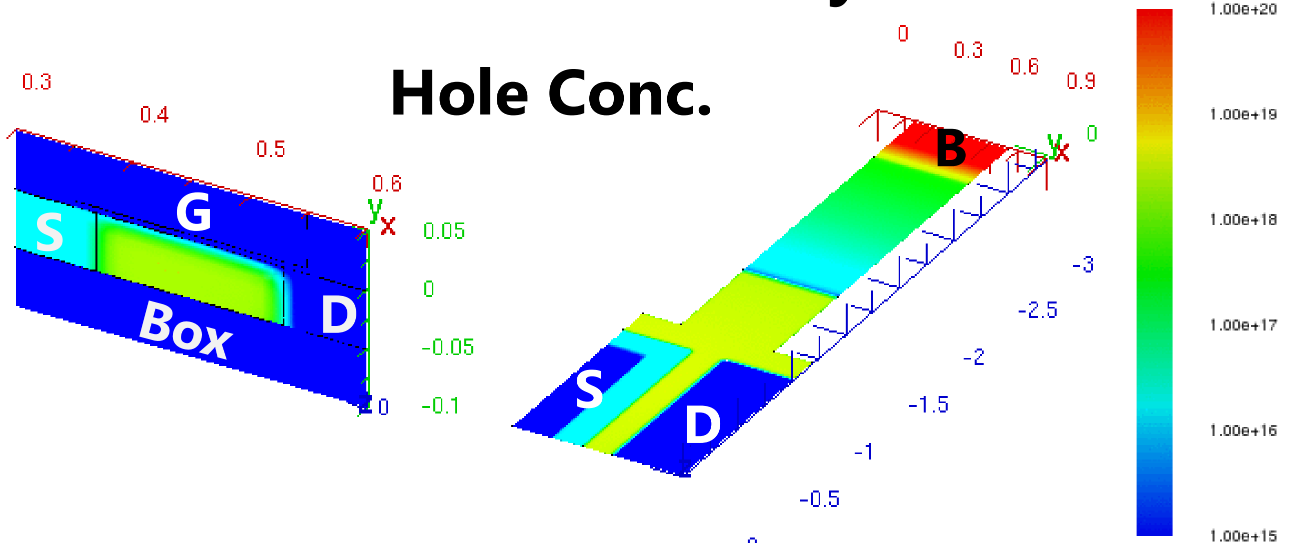
Transient characteristics of PNBT SOI-FET

T. Mori, J. Ida, *et al.*, *SISPAD* 2019

Animation of Carrier Dynamics

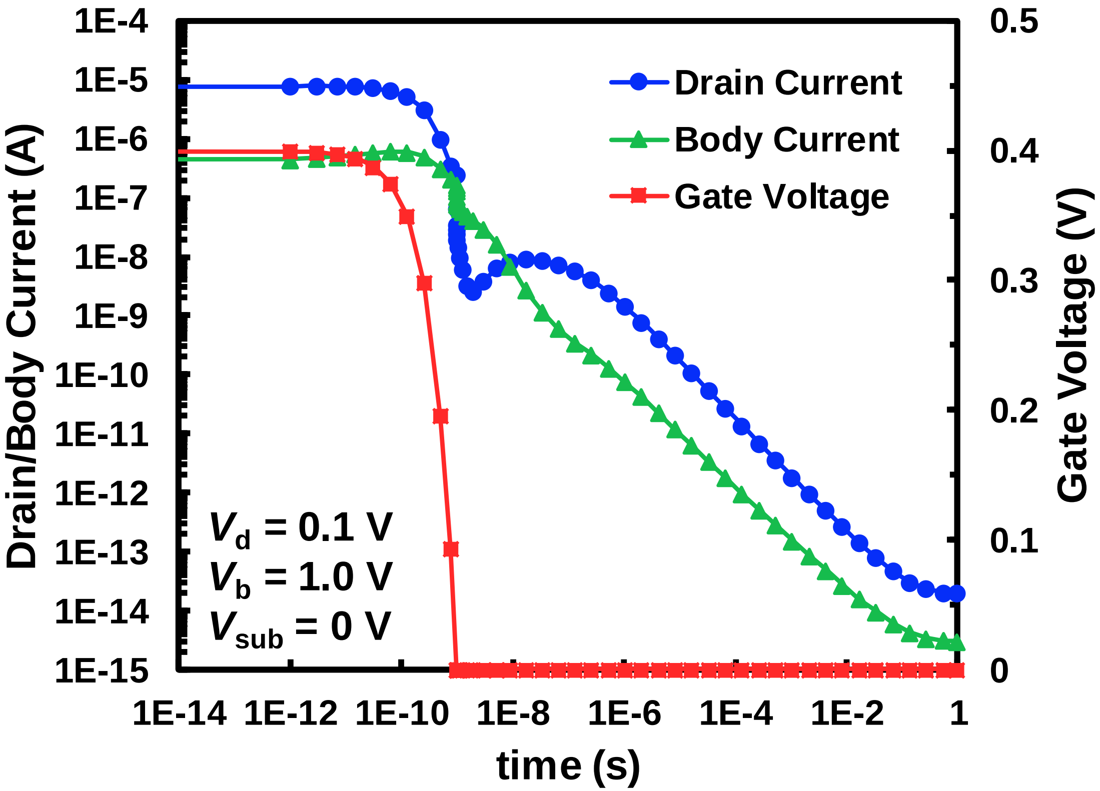


Flont

Center of SOI

(1) V_g ON state (2) V_g OFF state (3) Turn-off state

Turn-off (Simulation)



Device shows long-term leakage current upon turn-off because of accumulation carriers.

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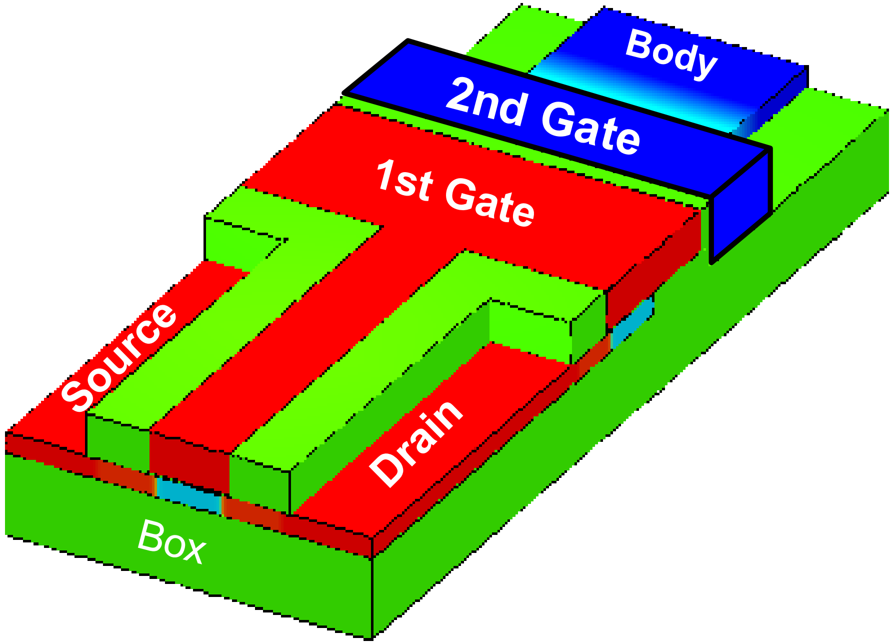
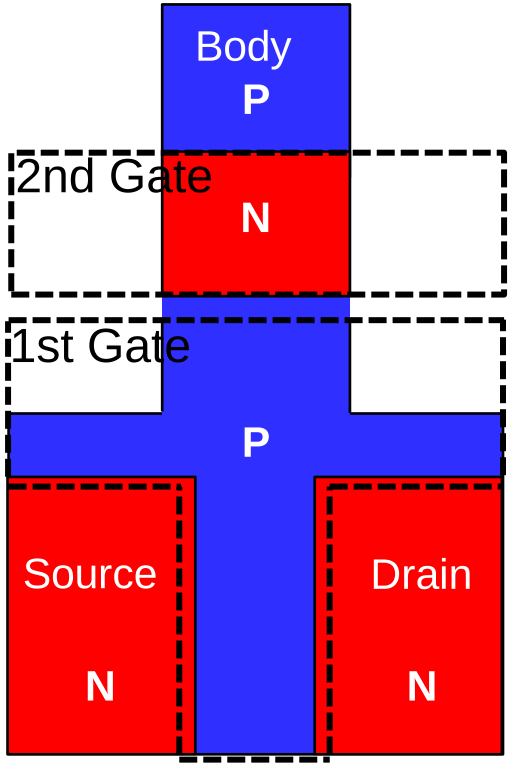
Dual Gate (DG) PNBT SOI-FET

To reduce the leakage current upon a turn-off

→ High-speed carrier ejection way is needed



Bird's eye view



Top view

We propose
Dual Gate (DG) PNBT SOI-FET

To control carrier ejection by using second gate

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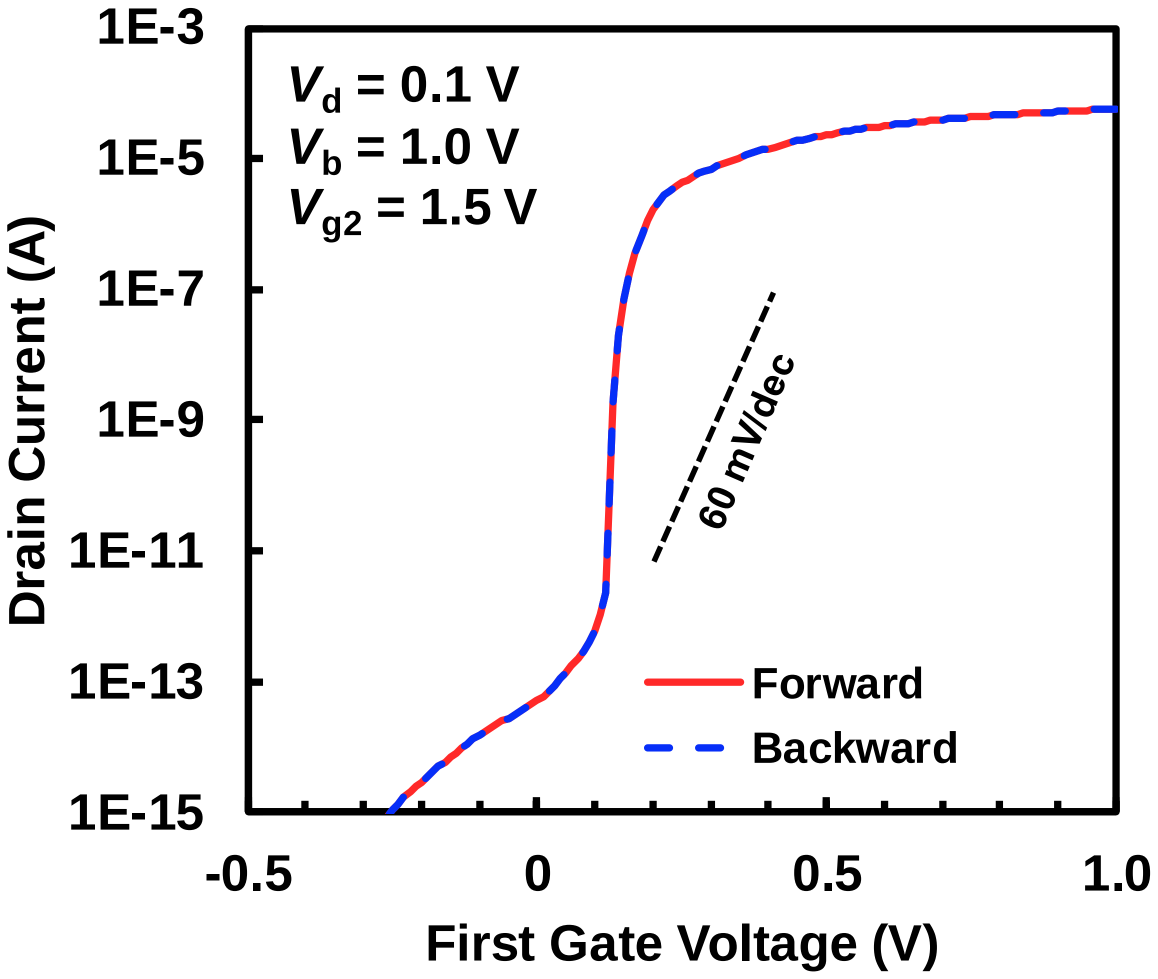
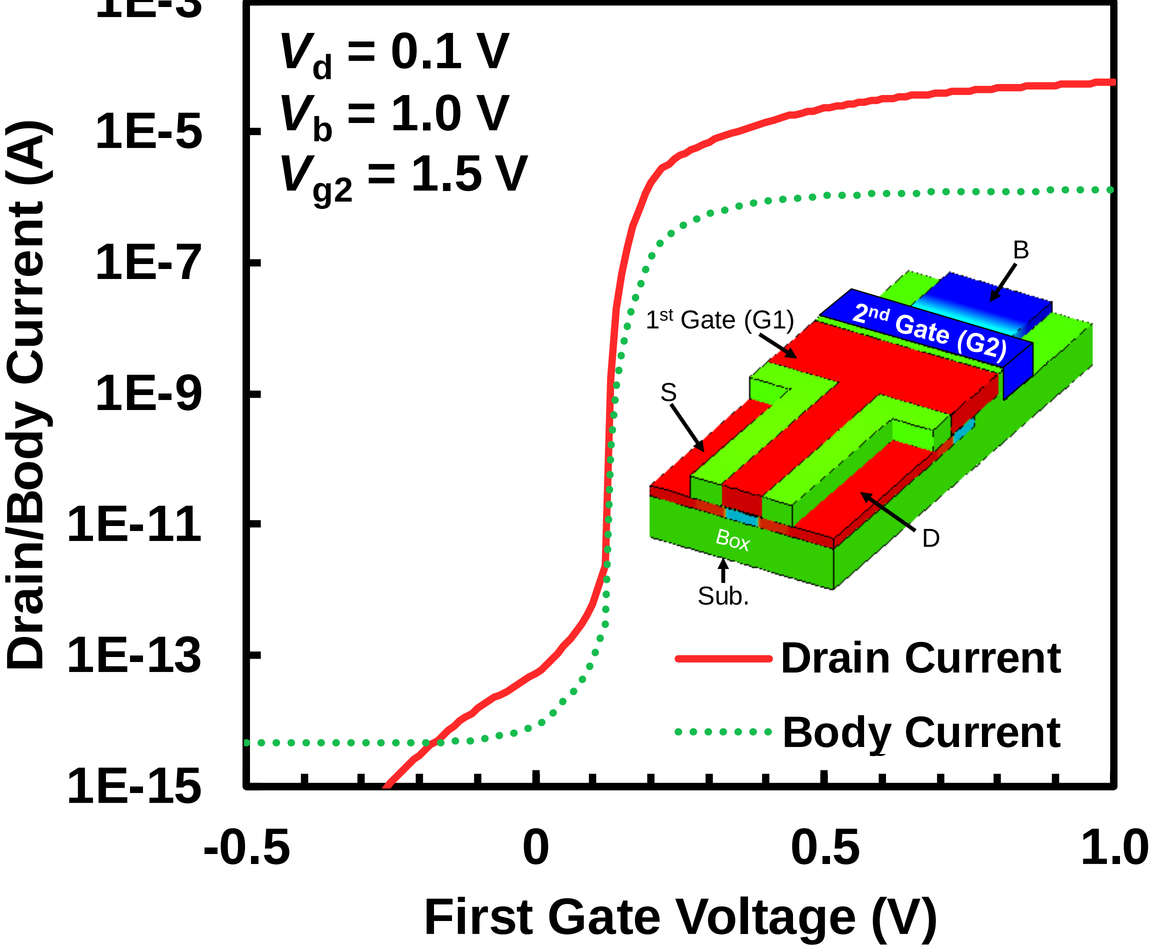
DC Characteristics of DG PNBT SOI-FET

T. Mori, J. Ida, *et al.*, *SISPAD* 2019





DG PNBT SOI-FET also has steep SS characteristics.
Additionally, the body current is smaller than drain current.

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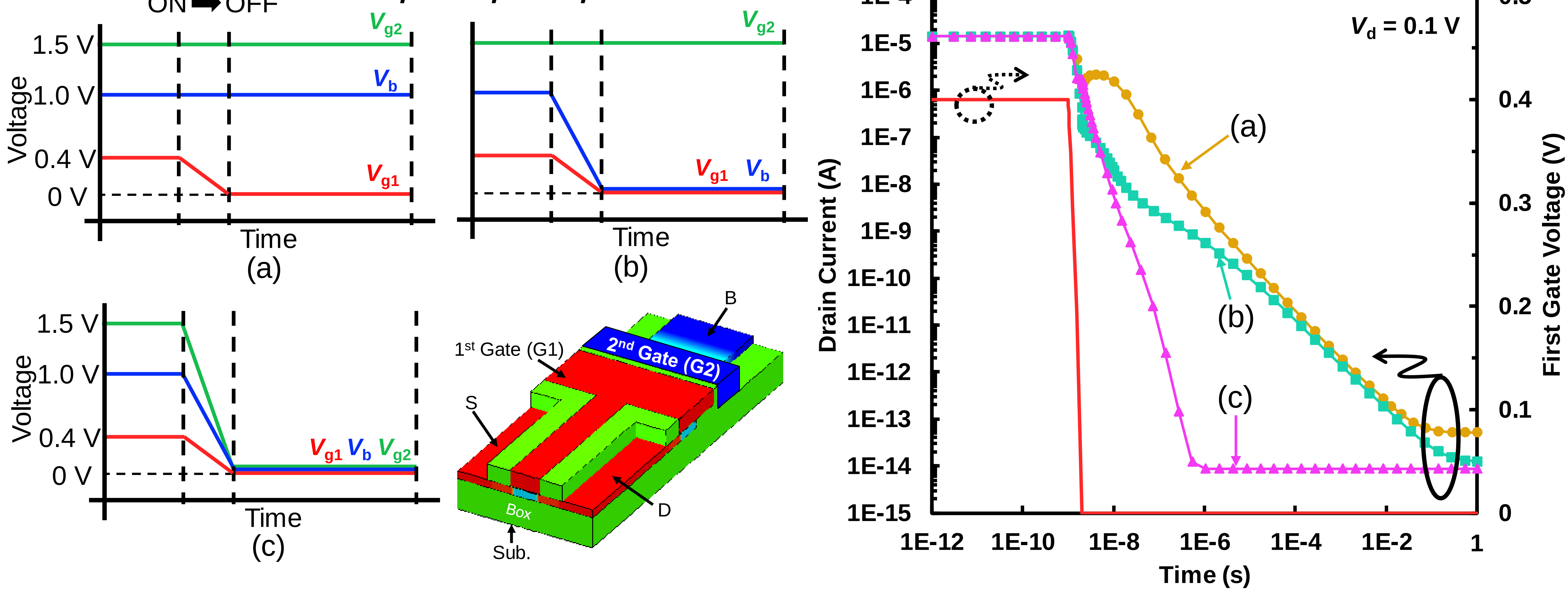
Turn-off Characteristics of DG PNBT SOI-FET

T. Mori, J. Ida, *et al.*, *SISPAD* 2019



V_{g1}, V_b, and V_{g2} turn off under same timing, leakage current decreases faster

Switching second gate means the operation mode changes from PNBT mode to a common body-tied mode

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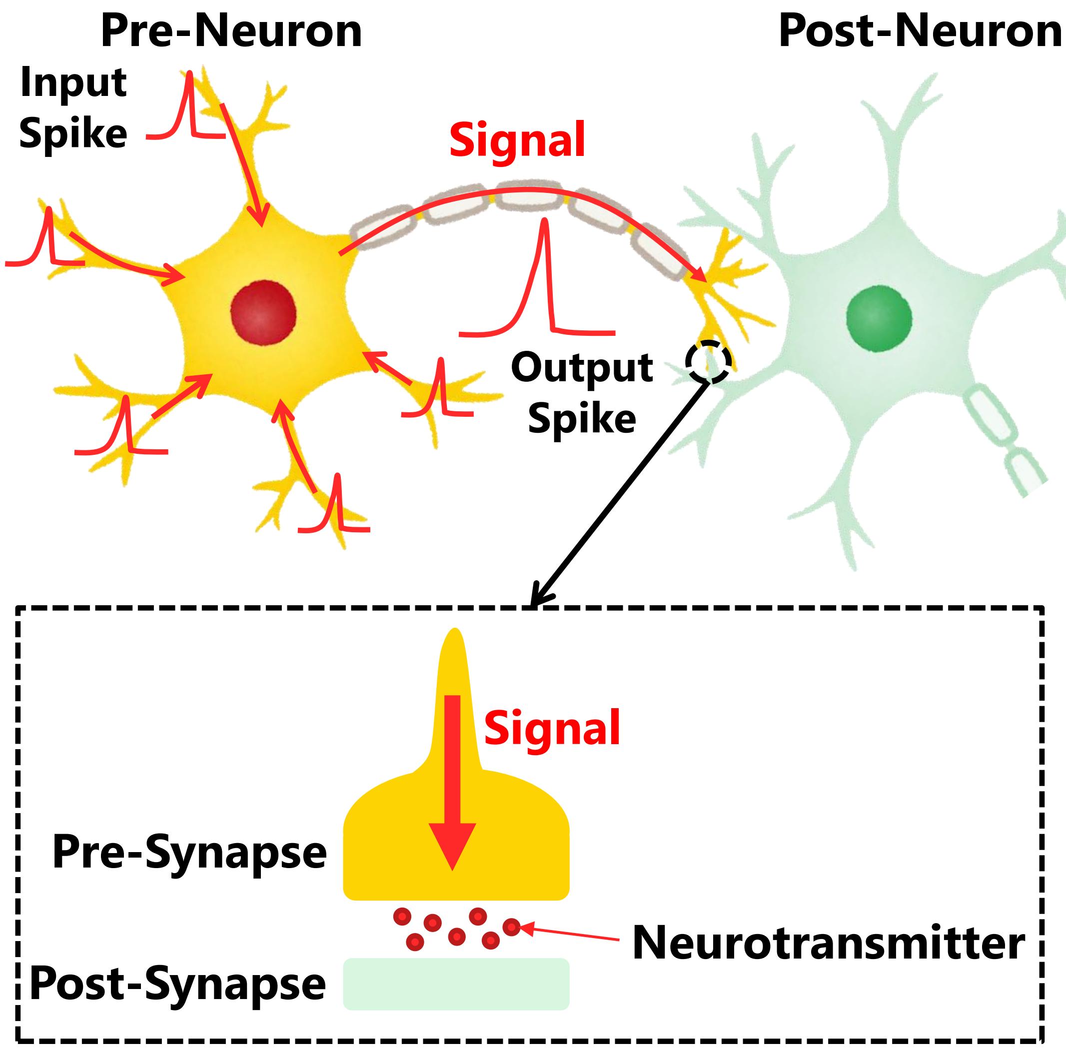
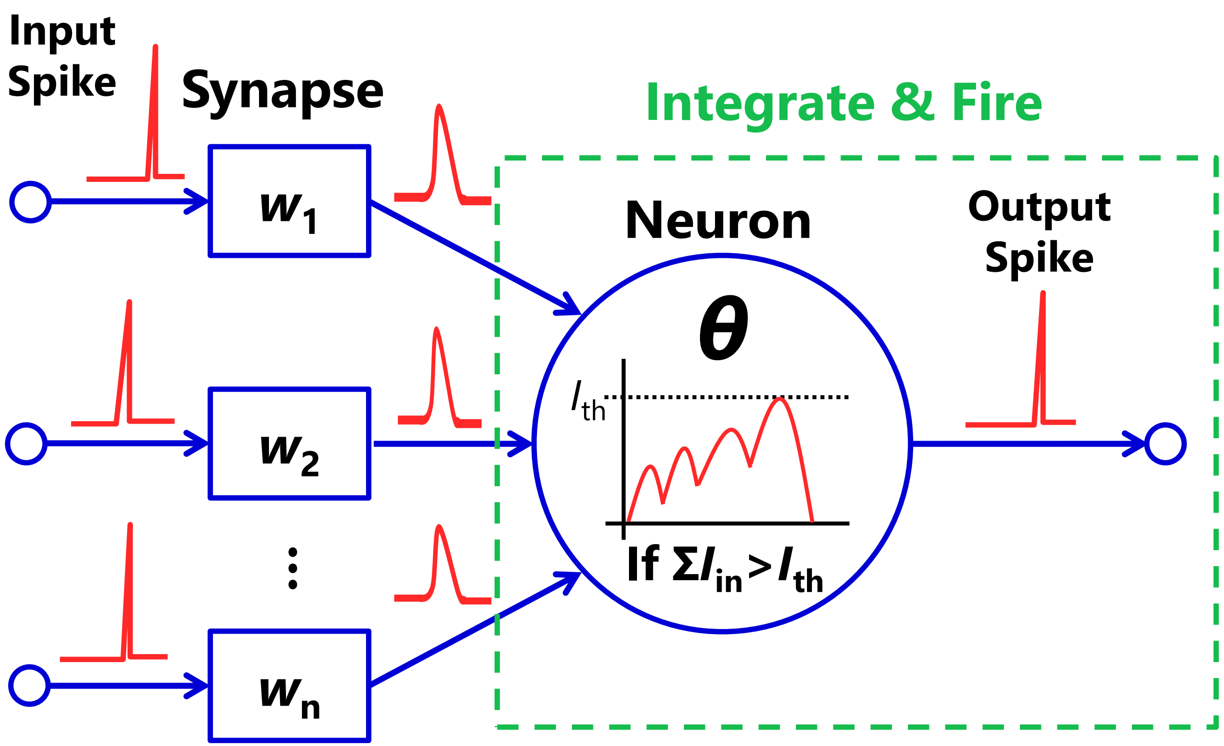
Application to neuromorphic chip | Spiking neural network

<Actual brain>



<Conceptual diagram>

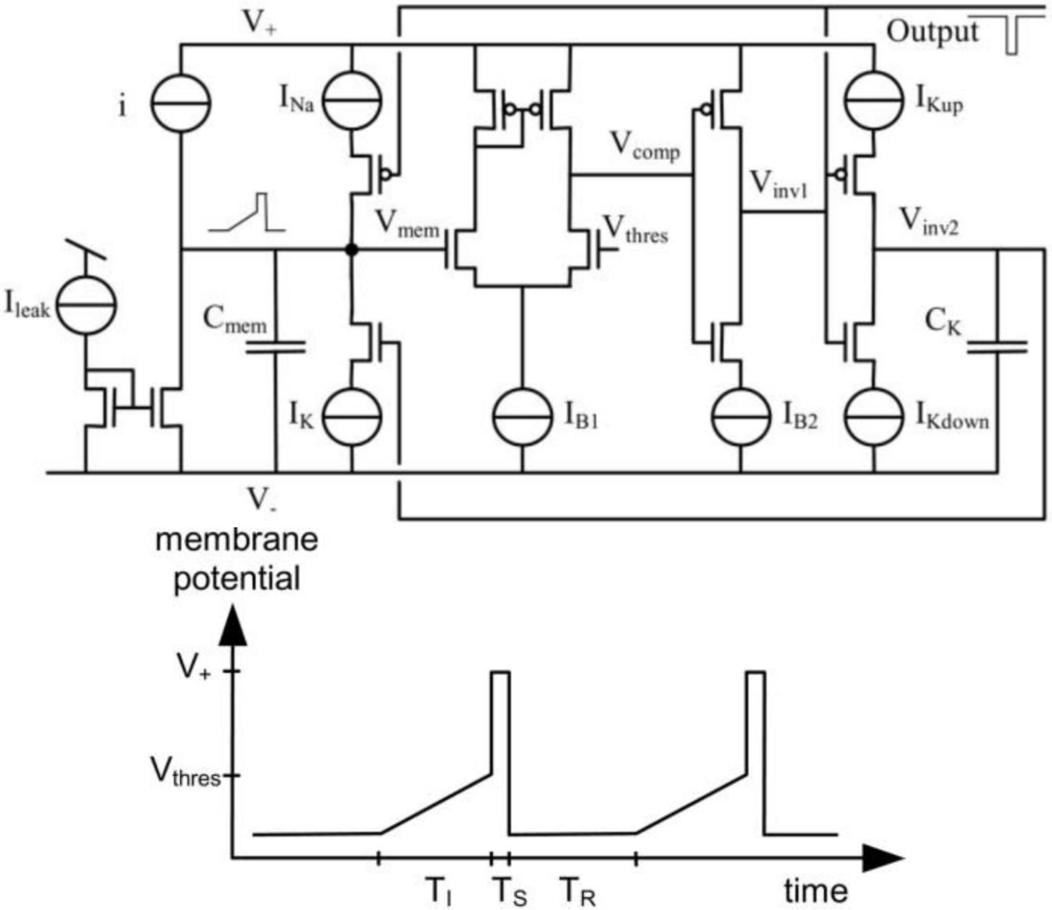


<Spiking Neural Network (SNN)>

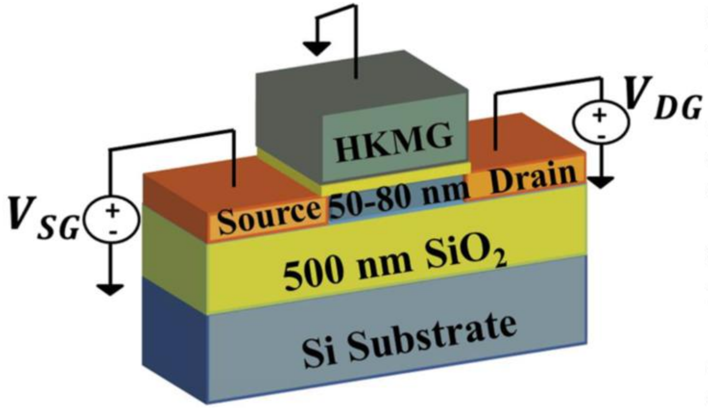
- **Low power**
  - -Spike input, Event-driven
- **High noise immunity** etc.

SNN has been studied for the next generation ANNs.

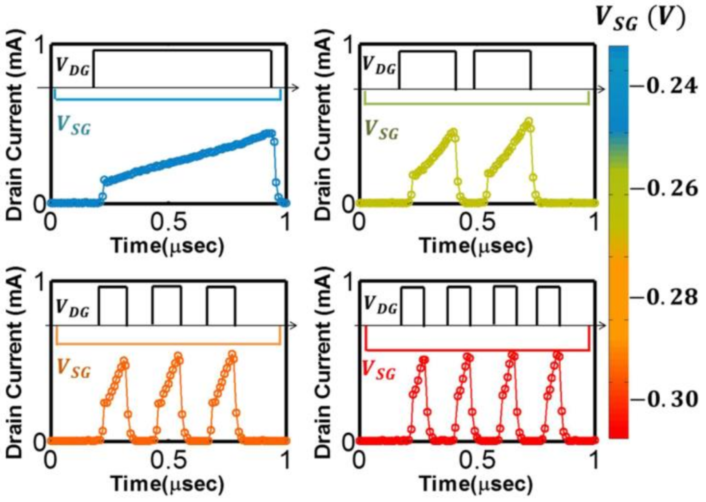
Application to neuromorphic chip | Previous study

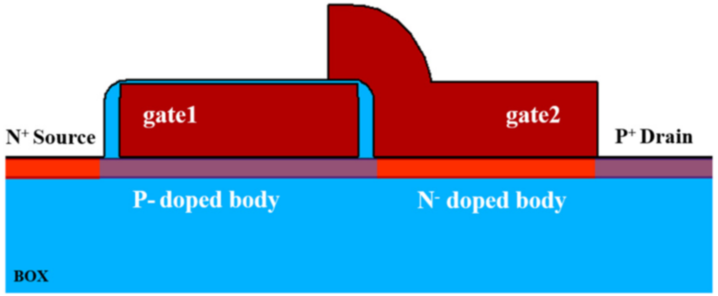


A. van Schaik, Neural Networks, 14, 2001.

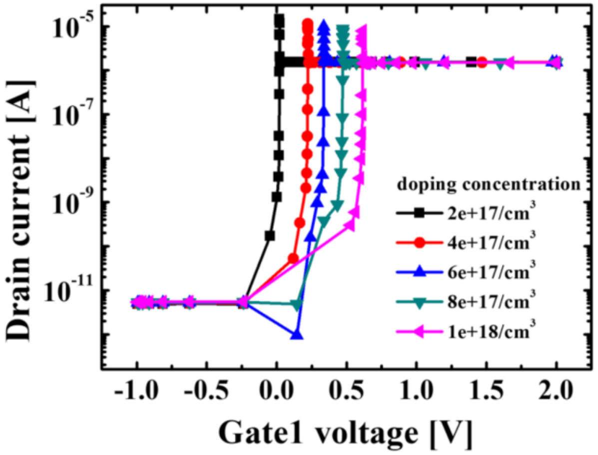


S. Dutta *et al.*, *Sci. Rep.*, 2017.



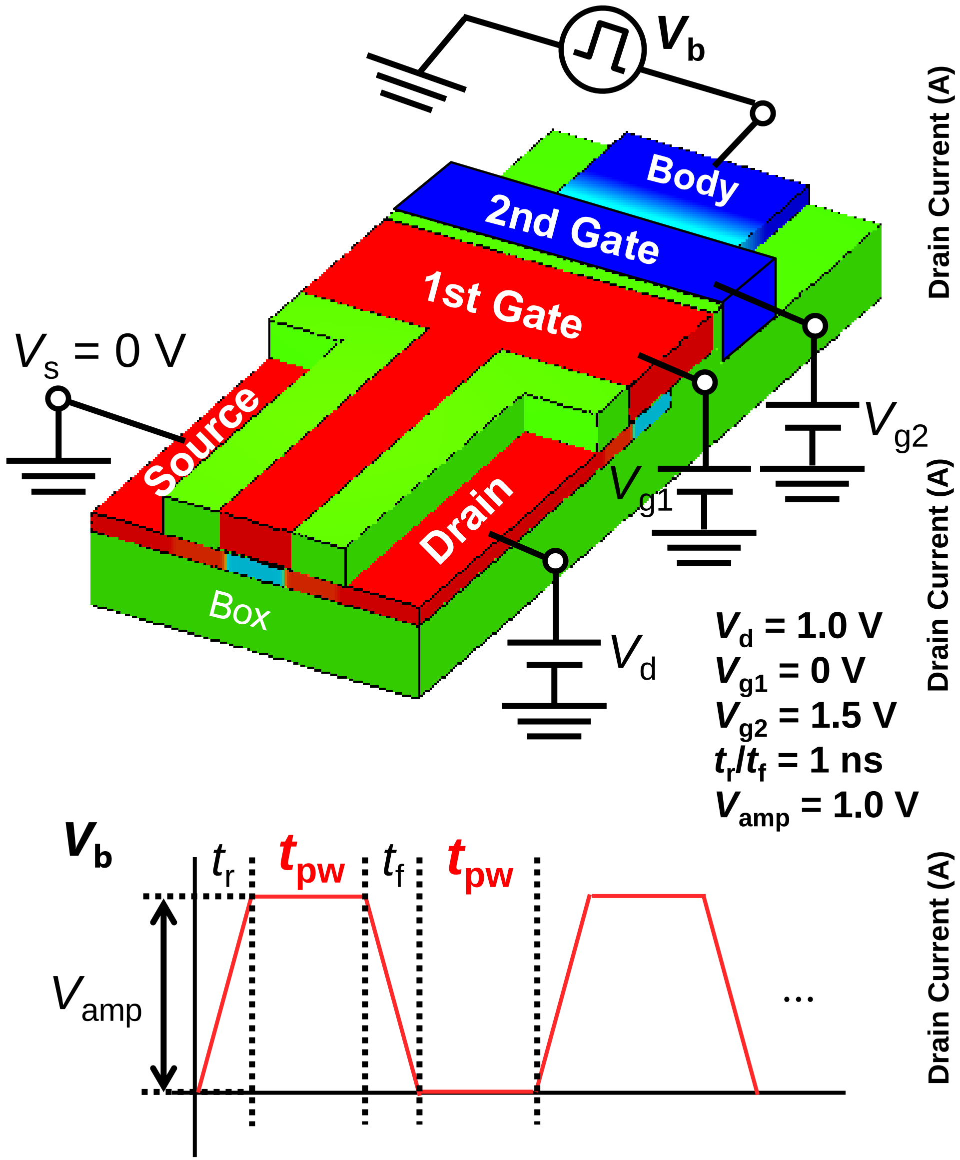


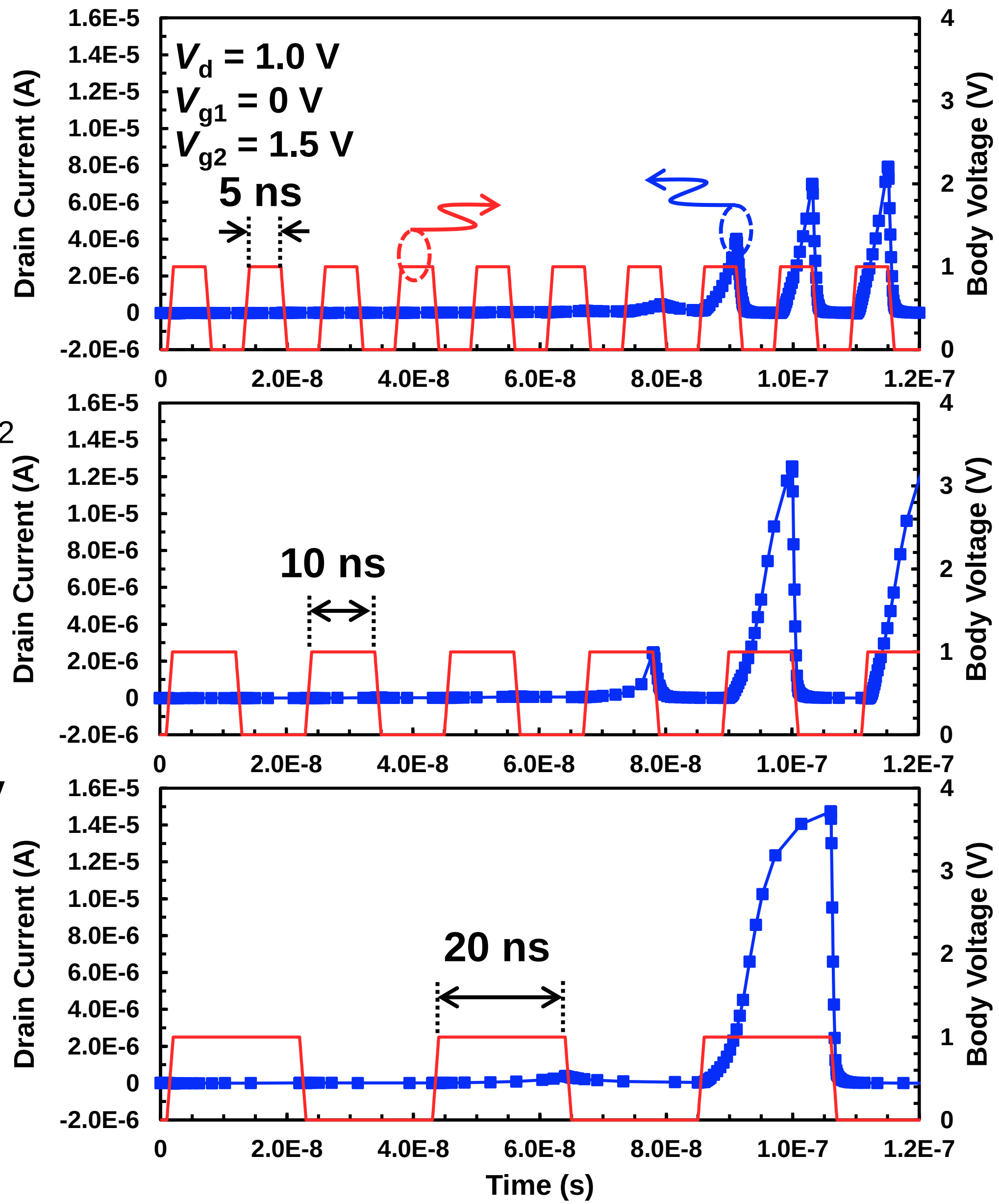
M.-W. Kwon *et al.*, *J. Appl. Phys.*, 2018.



The neuron circuit with floating body effects of a SOI-FET is possible to decrease the spike generation power and the foot-print of the circuit.

Integrate and Fire neuron by Using DG PNBT SOI-FET





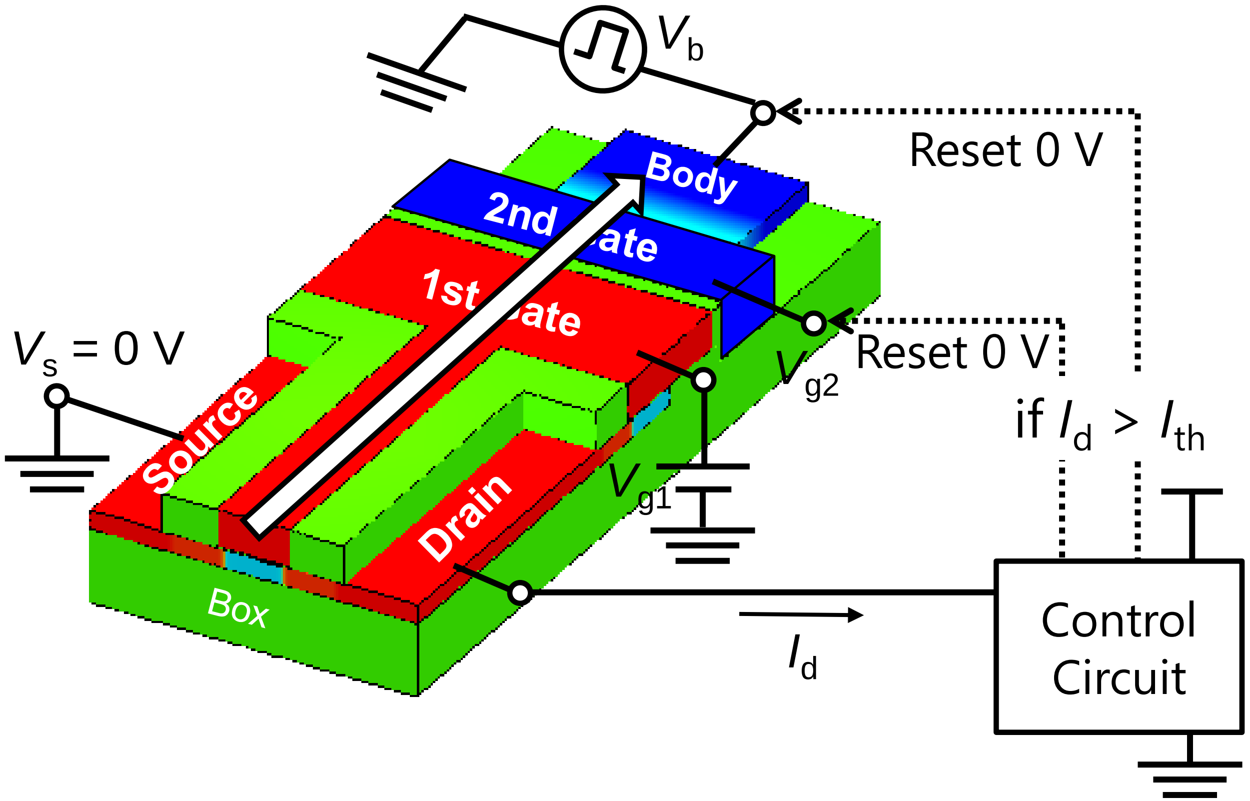
Pulse input
→Mimic spike

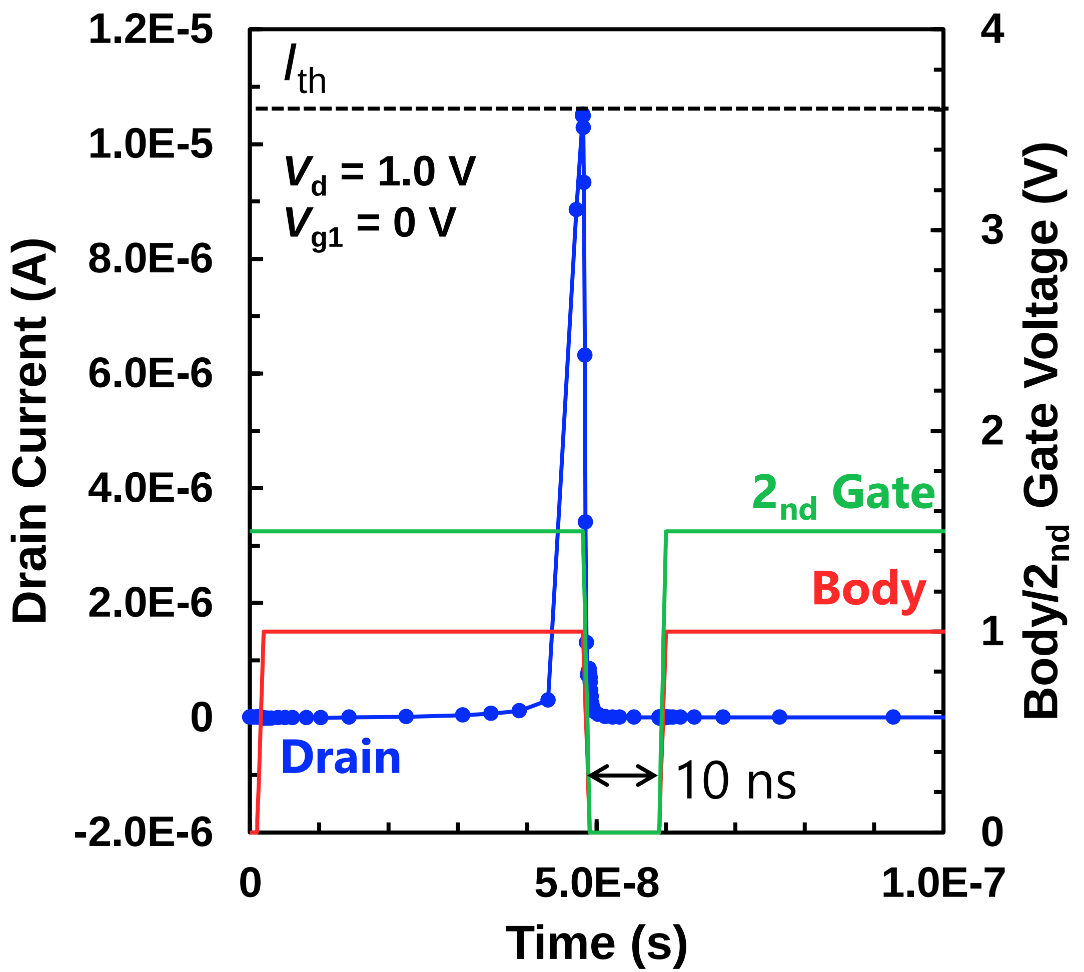
DG PNBT SOI-FET can turn-on even though intermittent inputs.

T. Mori and J. Ida, *SSDM* 2020

Spike generation with reset action

T. Mori and J. Ida, *SSDM* 2020





The accumulation carriers eject to the body and the base conditions are reset.

I_d does not turn on continuously after the reset.

The DG PNBT SOI-FET can make the single spike signal with reset action.

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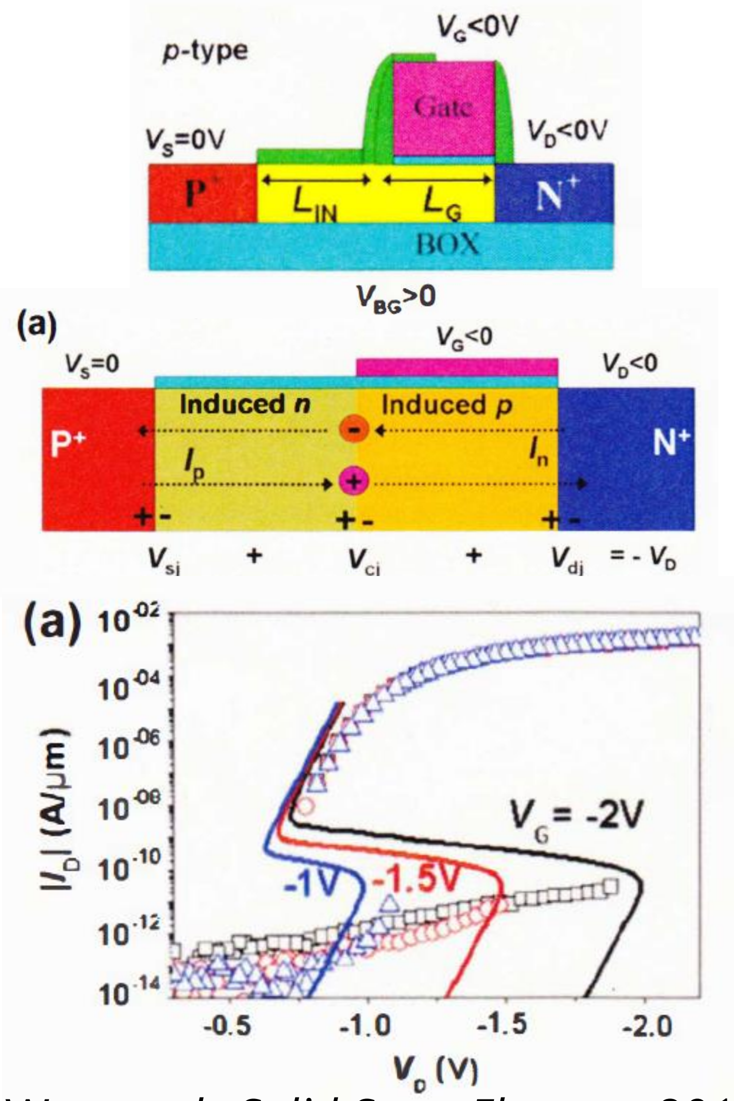
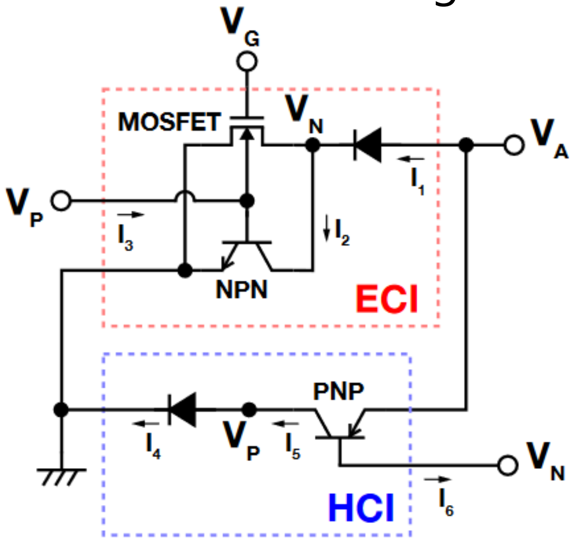
Modeling of PNBT SOI-FET (& thyristor-like devices)

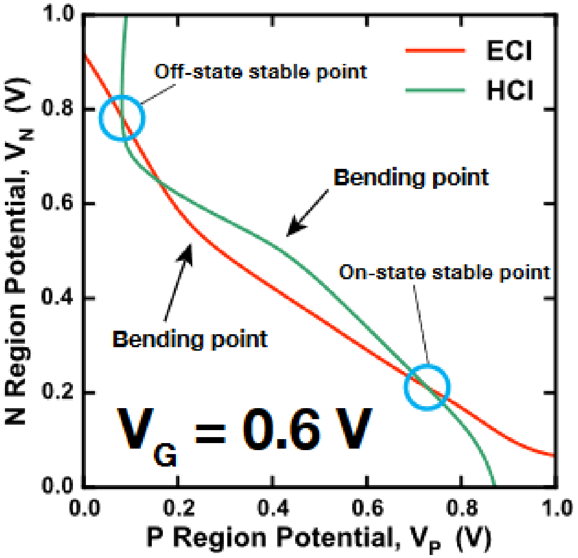
DC model of Z²-FET

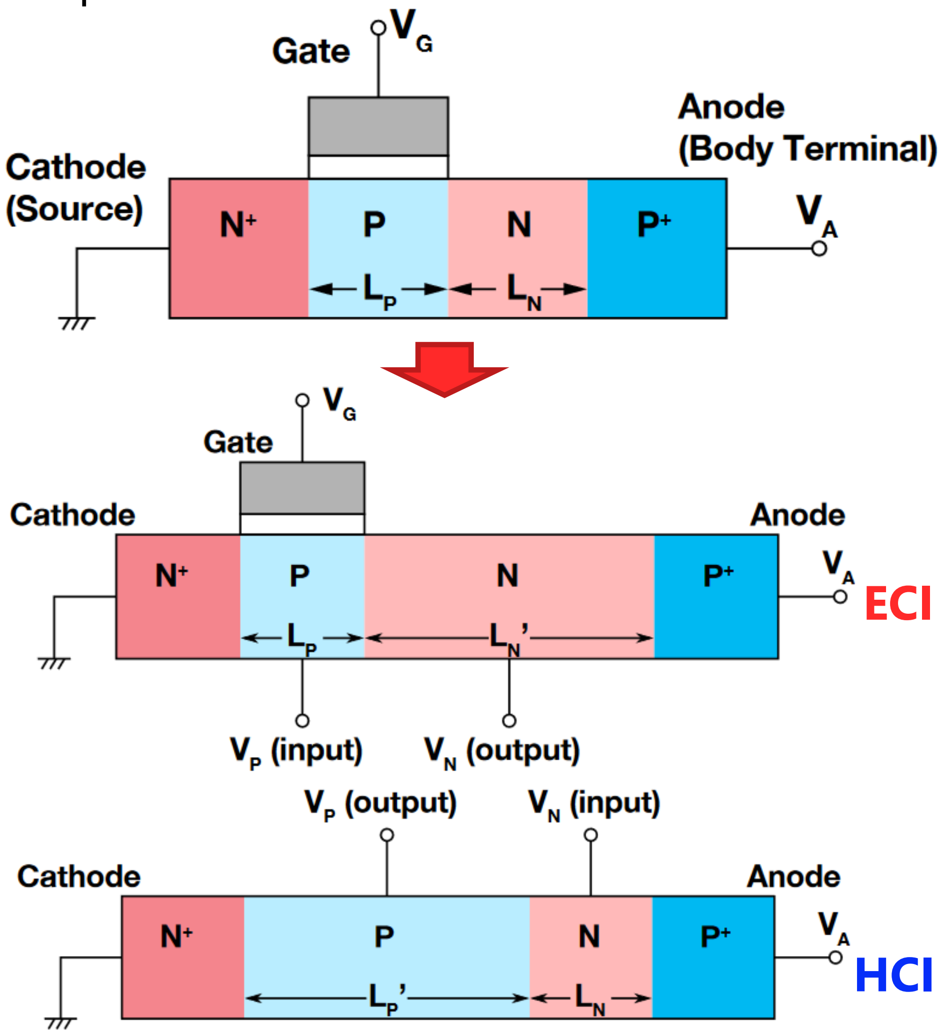


J. Wan *et al.*, *Solid State Electron.* 2013.

Voltage-based equivalent circuit model







D. Ueda *et al. Jpn. J. Appl. Phys.*, 2018.

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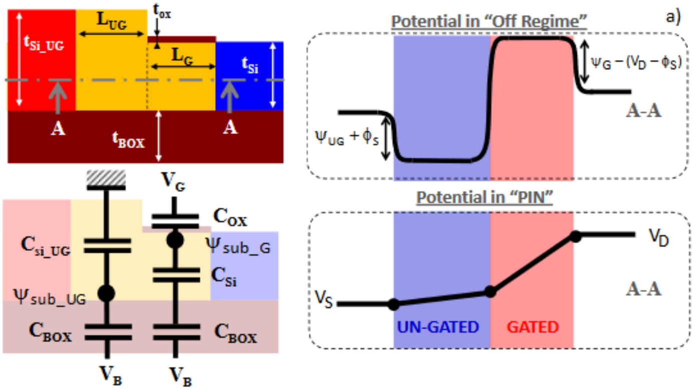
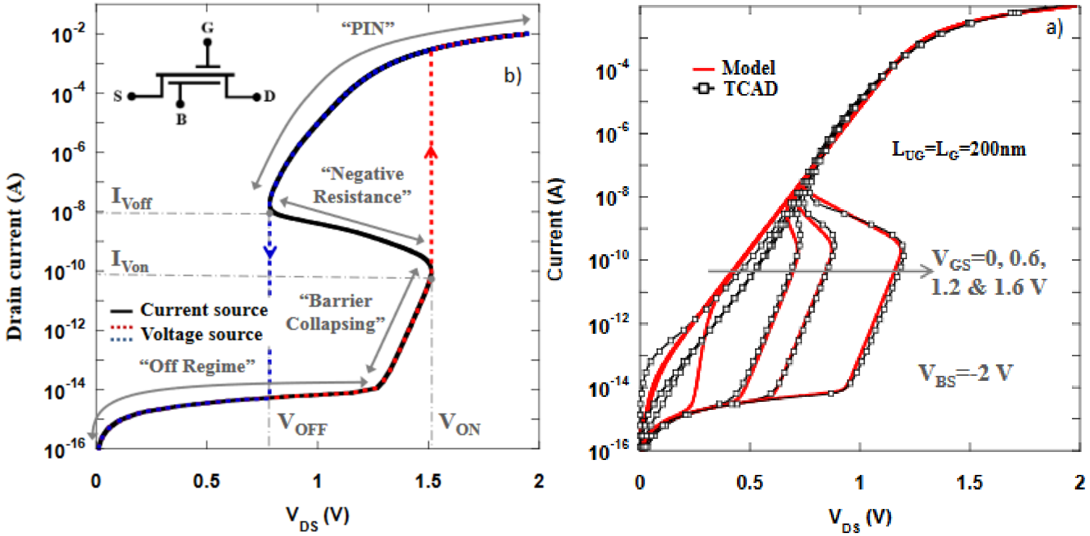
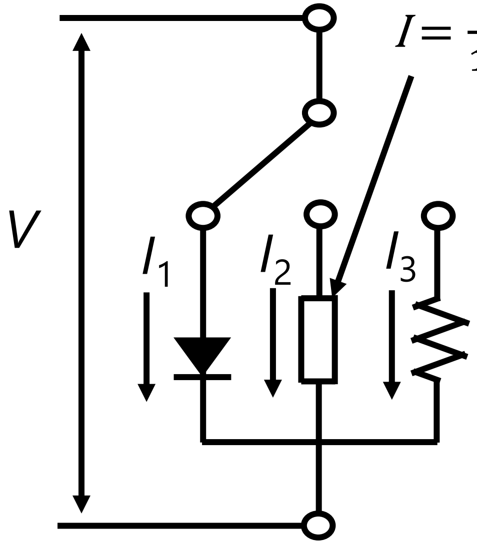
SPICE model of PNBT SOI-FET (& thyristor-like devices)



Z²-FET
SPICE model

S. Martinie *et al.*,
SISPAD 2017.



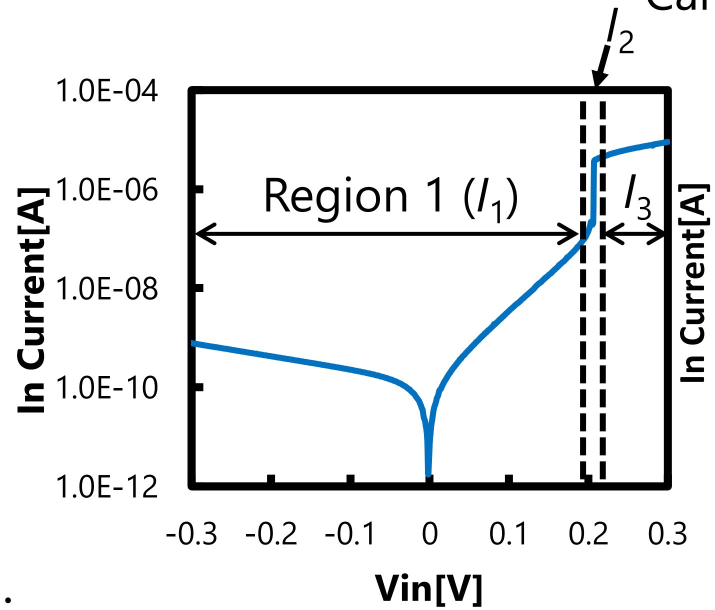


$$I = \frac{1}{1+\exp(-aV)}$$

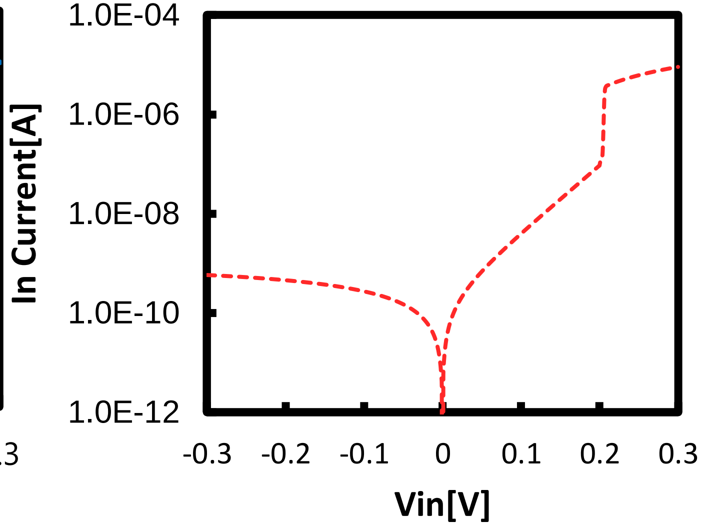
Diode connected PNBT SOI-FET
SPICE model (w/o transient effect)

Steep region is fitted by using
sigmoid function

Carrier charge & discharge effect
are needed...



Measurement



SPICE Model

We need more study about compact models...

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Summary

We introduce PN-body tied (PNBT) SOI-FET developed by our group.

PNBT SOI-FET has super-steep subthreshold slope (<1 mV/dec).

➡ Ultralow power LSI, High sensitivity sensor

DG PNBT SOI-FET has the function to integrate and fire neuron without comparator and capacitors.

Development of compact model

➡ It is important to reproduce carrier charge & discharge effect.

<Acknowledgment>

This work is the result of collaborations with the High Energy Accelerator Research Organization (KEK) and LAPIS Semiconductor Co., Ltd.

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Corporation and Mentor Graphics Corporation.

This work was partially supported by JST-CREST Grant Number JPMJCR16Q1, Japan.

The research has been partly executed in response to support of KIOXIA Corporation.