A new compact model for short-channel symmetric DG MOSFET

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Introduction

Double-gate (DG) silicon-on-insulator (SOI) MOSFETs with undoped channels are considered the most promising structures for scaling CMOS devices down to gate lengths in the 50 nm to 10 nm range. The use of Symmetric DG (SDG) MOSFETs with ultra thin bodies and ultra thin gate oxides suppresses short-channel effects making the conventional use of high channel doping densities and gradients unnecessary. This absence of dopant atoms in the channel improves mobility due to reduced scattering and eliminates random dopant fluctuations.

Appropriate DG MOSFETs' compact models are necessary for integrated circuits simulations. We present a new compact model of drain current for a symmetrical, undoped DG MOSFET. The model reflects most of the significant short-channel effects and allows for the simulation of devices with channel lengths down to 20nm.

Double Gate MOSFET Structure

Assumptions:
- symmetrical structure
- undoped channel
- midgap gate

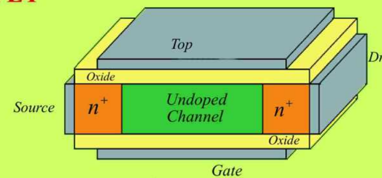

Fig.1. Double Gate nMOSFET

DG MOSFET Model

The new model is based on the long-channel charge-based model of Sallese et al.[1] and the explicit charge description presented in [2]. In order to extend the validity of the core model for short-channel devices we introduced several short-channel effects (dependence of threshold voltage on channel length[3], velocity saturation[4], channel-length modulation, drain induced barrier lowering [3] and drain-induced charge enhancement[5]). In[6] we investigated the impact of each correction on the device characteristics. Finally, we implemented the model equations in the hardware description language Verilog-A, and verified its accuracy by comparing calculated I-V, Gm-Id, and C-V characteristics with the results of 2D numerical simulations. We achieved good agreement with ATLAS simulations for a wide range of the device parameters (oxide thickness: 1-3nm, silicon film thickness:10-20nm, channel length: 20-500nm). We also performed some of the tests recommended by CMC [7], which proved a good overal behavior of the new model in all regions of operation.

Transfer and output characteristics of a short channel DGMOSFET (L=50 nm) are shown in Figs. 2 and 3, respectively. We compared the characteristics calculated according to the new model with the characteristics calculated according to the long-channel core model and the results of ATLAS simulations to justify the necessity of introducing short-channel corrections.

One of the most important parameters of a MOSFET, namely the transconductance-to-current ratio, is illustrated in Fig. 4 as a function of gate voltage with drain voltage as a parameter.

DG MOSFET charges and selected internal capacitances are shown in Figs. 5 and 6, respectively. The modeled characteristics are in good agreement with numerical calculations.

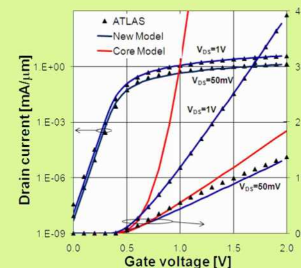

Fig.2. Comparison of transfer characteristics calculated according to the new model with the characteristics calculated according to the long-channel core model and the results of ATLAS simulations.

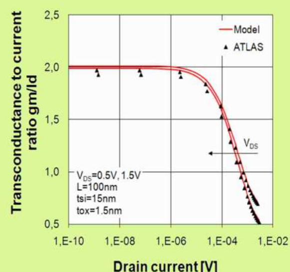

Fig.4. Transconductance gm normalized to the drain current as a function of drain current, for L=100nm. Solid line - compact model, symbols - ATLAS simulation.

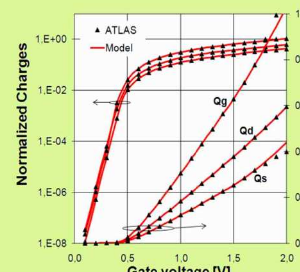

Fig.5. Normalized charges as a function of gate voltage, for Vds=1V, L=100nm. Solid line - compact model, symbols - ATLAS simulation.

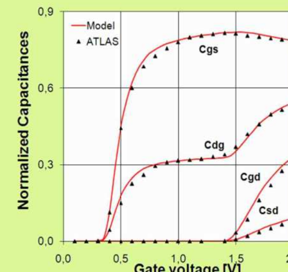

Fig.6. Normalized capacitances Cgs, Cdg, Cgd, Csg as a function of gate voltage, for Vds=1V, L=100nm. Solid line - compact model. Symbol line - numerical simulation.

Fig.3. Comparison of output characteristics calculated according to the new model with the characteristics calculated according to the long-channel core model and the results of ATLAS simulations.

Circuit simulation

Circuit simulation is the reason of compact modelling, therefore, in order to demonstrate the usefulness of our model we performed a few Spice simulations using our model.

One of the most commonly used circuits for basic validation of a MOSFET model is the NMOS inverter. The switching characteristics of NMOS inverters built of DG nMOSFETs with different channel lengths are shown in Fig. 7.The achieved agreement with ATLAS numerical simulations is very good.

MOSFET current dividers are useful analog circuits and can also be used to test the validity of compact models. We investigated the current divider shown in Fig.9., using (a) the core DG MOSFET model, (b) the new short-channel model. The results of the Spice simulations shown in Fig.10. Present the large impact of proper device model selection on circuit simulations.

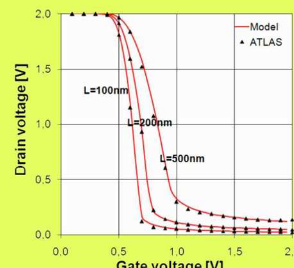

Fig.8. DG NMOS inverter switching characteristics for different transistor channel lengths L= 100nm, 200nm, 500nm.

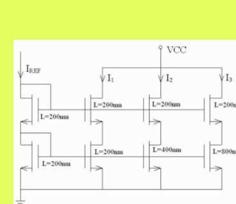

Fig.9. Current divider schematic

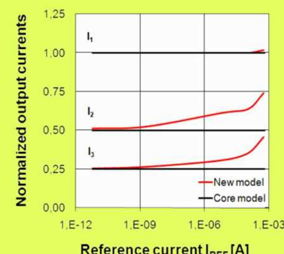

Fig.10. Current divider output currents normalized to the reference current I_{REF} as a function of I_{REF}.

Summary

We modified the drain-current model of Sallese et al. for undoped symmetric DG MOSFET, considering the most important 2D effects: velocity saturation, channel length modulation, DICE, DIBL and threshold voltage roll-off. In [6] we compared our model with already existing compact short-channel DG MOSFET models ([3,4]). Our new model introduces more short channel effects and so, presents better agreement with 2D numerical simulations (ATLAS). Moreover our corrections add only one fitting parameter to the core model. The drain-current model is still simple and useful for circuit device simulations of both long-channel and short-channel DG MOSFETs, which we proved by implementing the model in the Verilog-A hardware description language and performing Spice circuits simulations.

In the next step we intend to extend the model on asymmetric DG MOSFETs and introduce quantum-mechanical and hot-carrier effects. We also plan to develop a parameter extraction method.

References

[1] J.-M. Sallese et al., Solid-State Electron., vol. 49, pp. 485-489, 2005.
[2] O. Moldovan et al., IEEE Trans. Electron Devices, vol. 57, no. 7, pp. 17181724, Jul. 2007.
[3] B. Diagne et al., Solid-State Electron., vol. 52, pp. 9099-106, 2008.
[4] F. Lime et al., IEEE Trans. Electron Dev.Transactions on elektron devices, vol. 55, no. 6, 2008.
[5] S. Chouksey et al., IEEE Trans. Electron Dev., vol. 55, pp. 796-802, 2008.
[6] A. Sawicka Msc. Thesis Warsaw University of Technology, 2009.
[7] Compact Modeling Concil (http://www.eigroup.org/cmc/)

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