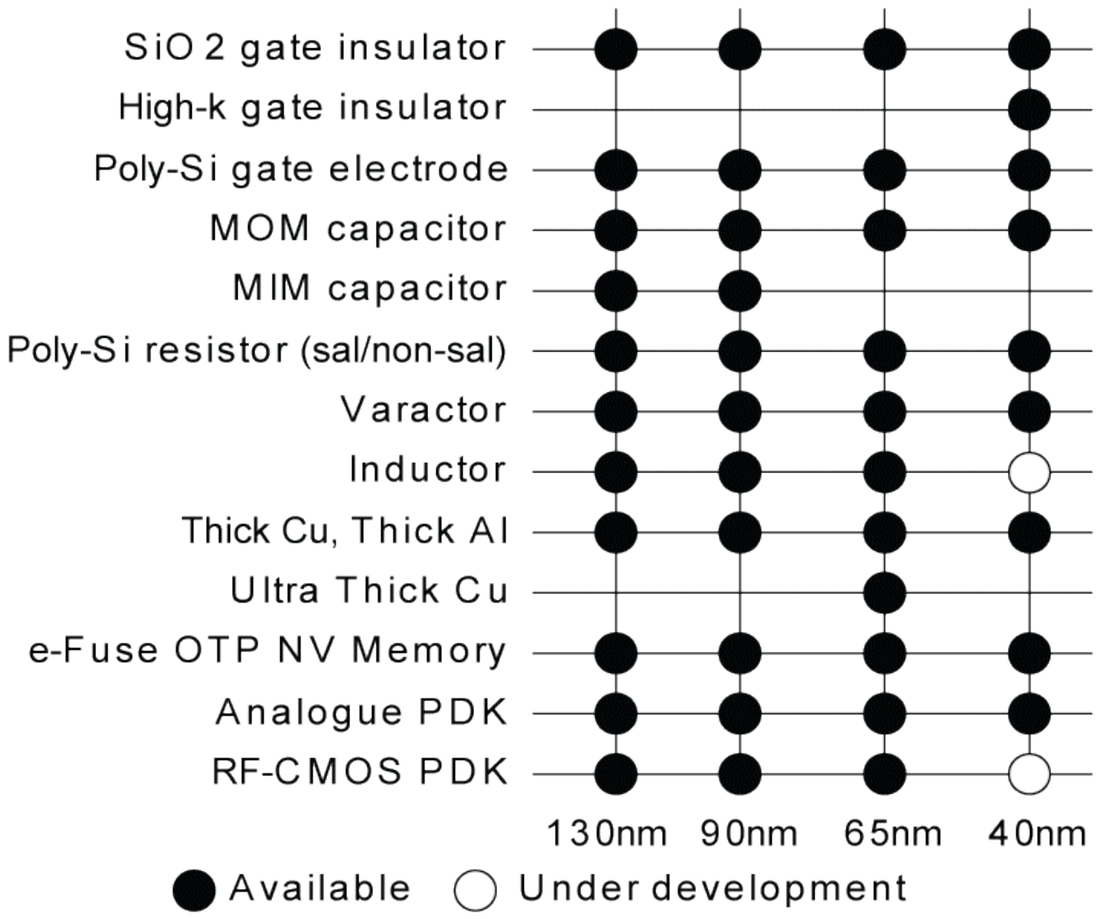
TOSHIBA

Leading Innovation »»

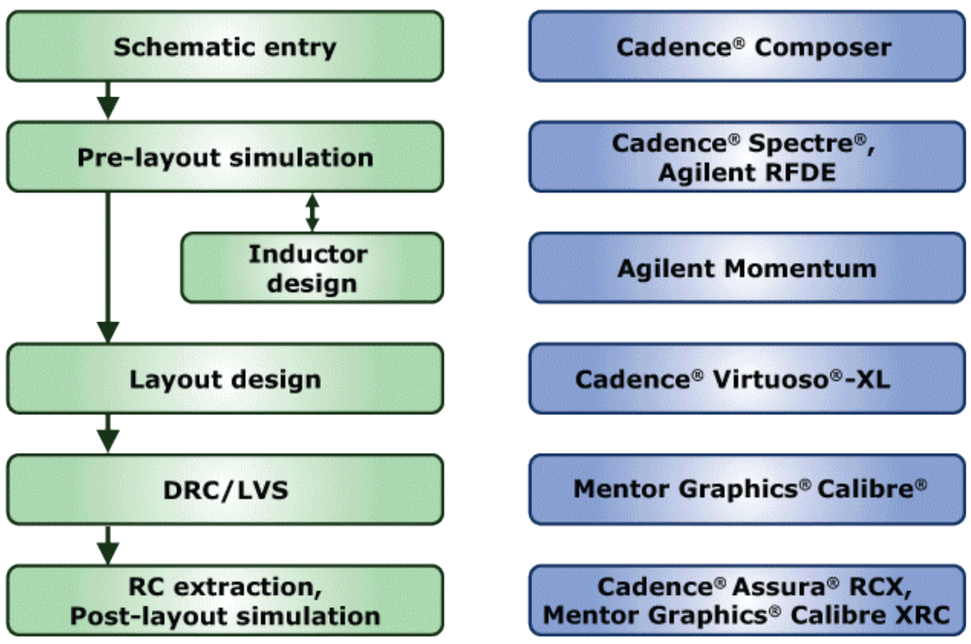
RFCMOS FOR HYBRID-COT AND FOUNDRY (ADVANCED AND OPEN IDM MODEL)



RFCMOS TECHNOLOGY OVERVIEW

Technology Node	130nm	90nm	65nm	40nm
Vdd[V]	1.5 1.2	1.2 1.0	1.2 1.0	1.1 1.0 0.9
Ft[GHz]	90	140	180	~250
Random Logic Density [kgates/sqmm]	206	403	800	2100
6 - tr SRAM Cell Density [squm/bit]	2,5	1,25	0,495	0,24

- Using standard CMOS Process
- Selective mixed-signal options
- Multi Vth, deep-N-well, High/Low-resistive Poly-Silicon, thick metal layers, MIM.cap., ..

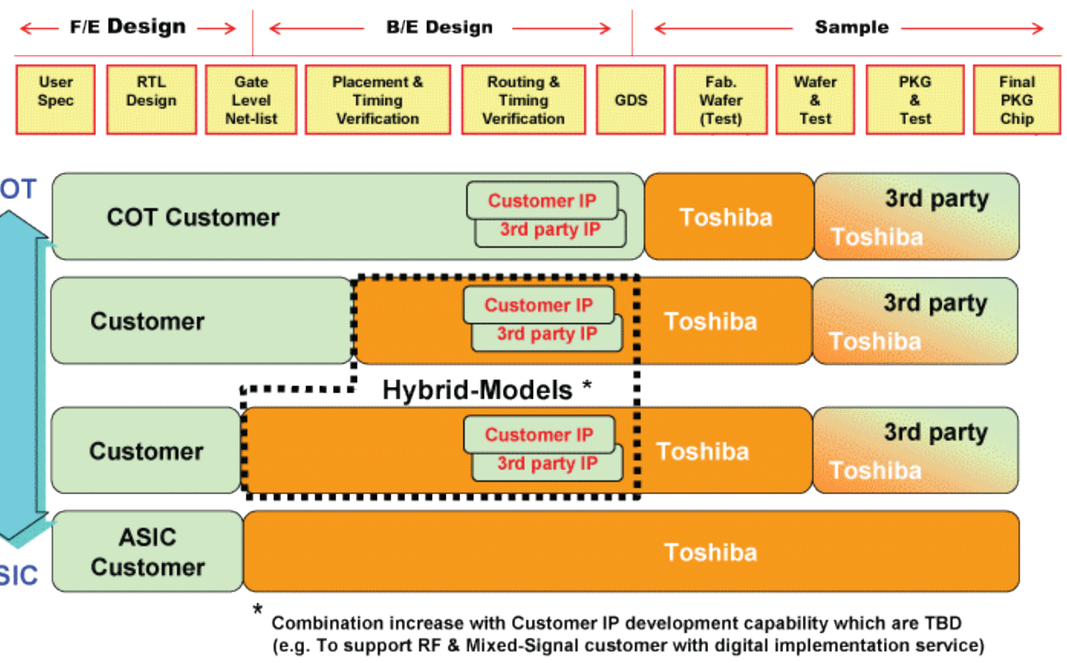


RF-PDK (PROCESS DESIGN KIT)

- MS- and RF- models are based on the same devices
- RF models additionally consider RF behaviour
- RF-PDK contains additional RF components Inductor (scalable pcell and model)
- Fully verified on silicon

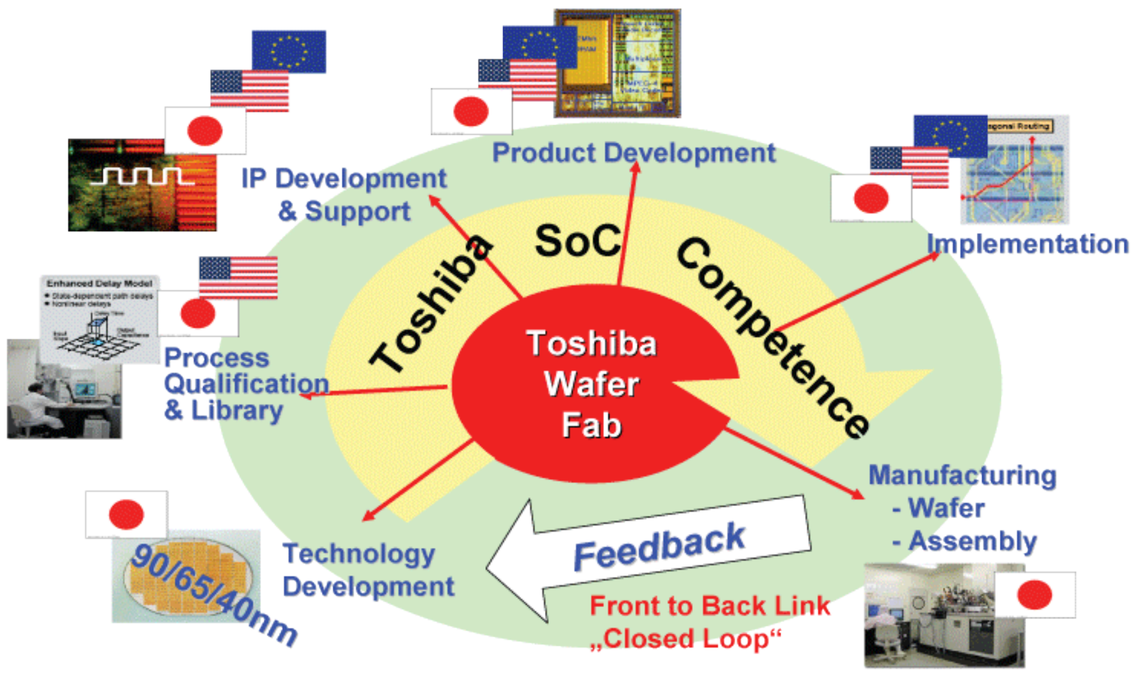
SUPPORTED EDA ENVIRONMENT

- Industry standard tools from leading vendors like Cadence, Mentor and Agilent are supported by Toshiba's RF-CMOS PDKs
- Support for other tools is available on request



HYBRID ASIC/COT MODELS

- Flexible I/F's
- Flexible Design-in
- Flexible Product-out
- Cost model tbd. ASIC or foundry



ADVANCED OPEN IDM MODEL

(BUSINESS STRATEGY FOR ASIC & FOUNDRY)

- All in One Hand
- All from One Source
- One Partner
- Road-map to 28/20nm