Characterization and Modeling of Single Event Transients in LDMOS-SOI technology

J. Alvarado, V. Kilchytska and D. Flandre

Microelectronics Laboratory, Université catholique de Louvain, B-1348 Louvain-la-Neuve, Belgium

Introduction

In this paper, we investigate single event transient (SET) phenomena in LDMOS-SOI devices. Three-dimensional simulations and a modified compact model are coupled in order to reproduce the current pulse generated by an ion strike, at different locations, through the LDMOS-SOI device, compared to a Partially Depleted (PD) SOI MOSFET. A qualitative result obtained by the compact model allows for explaining the effects to be taken into account during the transient. Lower transient drain current amplitude is observed in LDMOS device, whereas larger recovery time results in higher collected charge. In this work, we study the SET at off-state ($V_G = 0V$ and $V_D = 1V$) using three dimensional simulations of the LDMOS-SOI and PD SOI MOSFET. The off-state represents the worst case at low biases, since SET might turn on the transistor during a transient time.

Simulations

1. Comparison between experimental I-V curves and 3D simulations were performed in order to get good matching.
2. Several physical aspects were consider such as: doping, mobility, self-heating, impact ionization, recombination, etc.

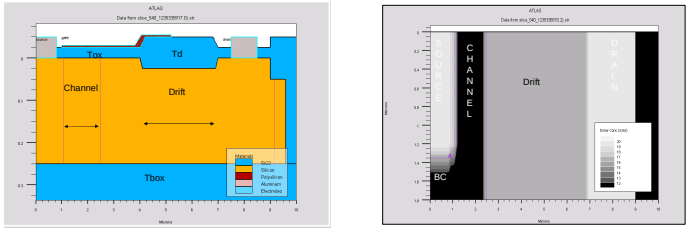

Fig.1 Schematic view of the simulated LDMOS transistor (left) cross-section, (right) top view of the body contact transistor

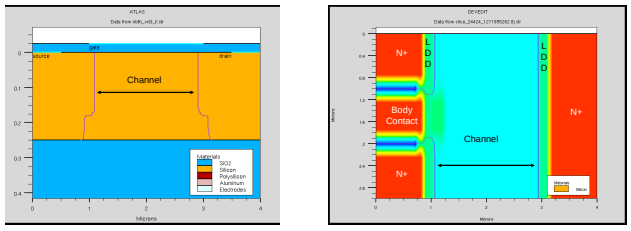

Fig.2 Schematic view of the simulated PD transistor (left) cross-section, (right) top view of the body contact transistor

Model

SET current

The drain current which includes the off-current I_{Doff} and the current generated by an ion-track can be given as:

$$I_D = I_S \cdot \left[q_S^2 - q_D^2 + q_S - q_D\right] + I_{Doff} + W \cdot L \cdot \left(J_n + J_p\right)$$

where $I_S = 2\,Ut\,\mu_{eff}\,\eta\,C_{ox}\,(W/L)$, Ut is the thermal potential, W is the channel width, L is the channel length, C_{ox} is the oxide capacitance per unit area and J_n and J_p are the current densities of electrons and holes, respectively which are given as [1]:

$$J_n = qD_n\nabla\rho_n(r,y,t) + q\mu_n nE \qquad J_p = -qD_p\nabla\rho_p(r,y,t) + q\mu_p(N_A + n)E$$

where N_A is the p-type doping concentration, n is the number of electrons generated by the ion-track and $\nabla\rho_{n,p}(r,y,t)$ represents the gradient of the function which includes the electron-holes pairs generated by an ion-track as [2]:

$$\nabla\rho_{n,p}(r,y,t) = \frac{2\rho_0}{\pi R_{n,p}^3}\cdot\sum_k \frac{\exp\left[-\dfrac{\lambda_{n,p}^2(2k-1)^2\pi}{4} - \dfrac{r^2}{t_{Si}^2\lambda_{n,p}^2}\right]}{\lambda_{n,p}^2} \qquad \lambda_{n,p} = \sqrt{\frac{4D_{n,p}t}{R_{n,p}^2}}$$

$$R_{n,p} = W/L\sqrt{k_{x1}\cdot X_{n,p}^{k_{x2}}}$$

where $\rho_0 = LET\ Z_\rho / E_w$ is the electron-hole pair density generated by an ion track, Z_ρ is the density of the target material (i.e. for Silicon 2.33 g/cm^2), E_w is the energy necessary to produce one electron-hole pair (i.e. for Silicon 3.6 e-h/eV).

X_n is the distance between the ion-track position and the drain terminal whereas X_p is the distance between the ion-track position and the source terminal with k_{x1} and k_{x2} are fitting parameters.

The lateral electric field in the channel can be given as:

$$E = \frac{2\cdot Ut\cdot v_{sat}}{L\cdot\mu_{eff}}\left[q_S - q_D\right]$$

where v_{sat} is the carrier velocity saturation and the normalized charges related with the drain and source, q_D and q_S, respectively, can be calculated by using the threshold voltage V_T and the Lambert W function LWF as[3]:

$$q_{S(D)} = \frac{\eta}{\alpha}LWF\left[\exp\left(V_G - V_T - \eta V_{S(D)}/\eta Ut\right)\right]$$

The effective mobility μ_{eff} used in this model considers the effect of the velocity saturation, both electric fields, transversal (scattering) and longitudinal (CLM) as well as the series resistances (R_D, R_S) as:

$$\mu_S = \frac{\mu_0}{1+\left(\theta_{ph}E_\perp\right)^{1/3}+\left(\theta_{SR}E_\perp\right)^2} \qquad \mu_{eff} = \frac{\mu_S\left[1+\left(\dfrac{\mu_S V_{Def}}{v_{sat}L}\right)^2\right]^{-1/2}\left[1-\dfrac{\Delta L}{L}\right]^{-1}}{\left[1+2C_{ox}\dfrac{W}{L}\left(R_S+R_D\right)\mu_S\left(V_G - V_T - \dfrac{n}{2}V_{Def}\right)\right]}$$

Considering the off-state condition, the drift resistance presented in the LDMOS can be modeled by [4]:

$$R_{Drift} = \frac{\rho_{Drift}L_{Drift}}{t_s W(1+\theta_1 V_G + \theta_2 V_G^2)} = R_D$$

Results

Good agreement between simulated, modeled and experimental data is obtained.

Also, good qualitative agreement of currents transients caused by the ion track at different positions is observed in the PD SOI MOSFET.

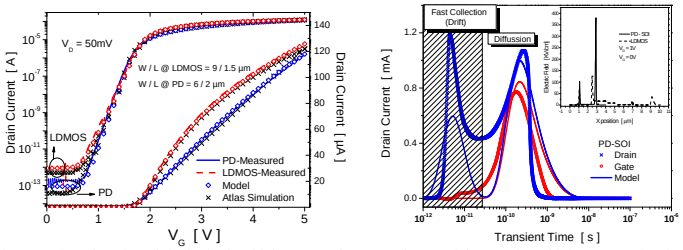

Fig.3 Comparison of experimental, simulated and modeled I-V curves of LDMOS and PD SOI (left), comparison of drain current transients between simulated and modeled at different positions (right). Inset: Longitudinal Electric Field versus position at off state in PD MOSFET and LDMOS.

Three peaks are observed in LDMOS current transients due to the asymmetry. Also, reduced current peaks are obtained since LDMOS presents smaller electric field than PD SOI whereas longer transient duration is observed in LDMOS.

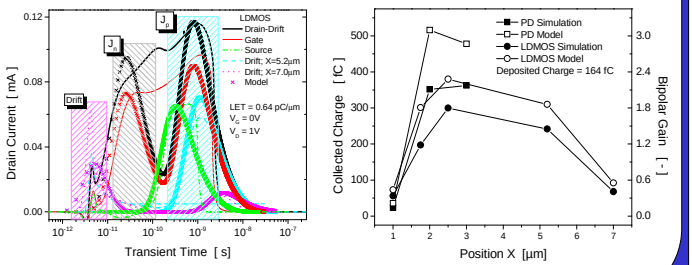

Fig.4 Comparison of drain current transients between simulations and model with different ion track positions (left), collected charge and bipolar gain comparison between simulations and model for PD MOSFET and LDMOS (right).

Conclusions

Comparison between simulations and model proves that a simple model provides good description of the single event effects in both kind of transistors.

Smaller and longer transient is observed in LDMOS transistor compared with PD MOSFET at off-state condition.

Comparable charge collection and bipolar gain is observed in the PD SOI and the LDMOS, because while PD SOI possessed higher current peaks due to the higher electric field, the LDMOS exhibits longer transient durations thanks to the asymmetry.

REFERENCES

1. J. P. McKelvey, Solid State and Semiconductor Physics, Harper and Row, 1980.
2. S. Kirkpatrick, "Modeling Diffusion and Collection of Charge from Ionizing Radiation in Silicon Devices", IEEE Trans. Electron Devices, vol. ED-26, No. 11, November 1979.
3. J. Alvarado, et. al., "Harmonic distortion analysis using and improved charge sheet model for PD SOI MOSFETs," Microelectronics Journal 38 (2007) 321-326.
4. Y.S. Chauhan, et.al.,"An EKV-based high voltage MOSFET model with improved mobility and drift model," Solid State Electronics 51 (2007) 1581-1588.