Simulation study of digital circuits based on nanometric Surrounding Gate Transistors: the role of quantum and velocity overshoot effects

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Introduction

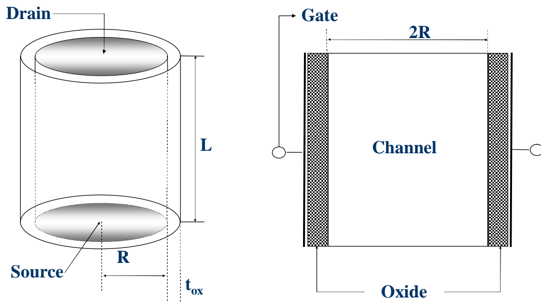
A Verilog-A compact model for Surrounding Gate Transistors (SGTs) has been implemented to study basic digital circuits.

A classical drain current model was used as starting point. The model has been enhanced to account for quantum mechanical (QME), velocity overshoot (VOE), short channel SCE and velocity saturation (VSE) effects.

Both the electron and hole layers are known to be highly confined in these structures due to structural as well as electrical confinement.

The influence of confinement effects in several circuits based on these quantum nanowires are characterized in depth. In particular, CMOS inverter gate delays, CMOS inverter ring oscillator frequencies, etc., have been obtained in order explore the relationships between the most representative technological parameters of the transistors and circuit performance.

Classical charge and current model for SGTs [1]



$$V_T = V_0 + 2V_{th}\ln\left(1+\frac{Q'}{Q_0}\right) + \Delta V_{TQM}$$

$$Q_0 = \frac{4e_{Si}}{R}\frac{kT}{q}$$

$$C_{Oxide} = \frac{e_{ox}}{R\cdot\ln\left(1+\frac{t_{ox}}{R}\right)}$$

$$\Delta V_T = \frac{\left(\frac{2C_{TOTAL}V_{th}^2}{Q_0}\right)Q'}{(Q_0+Q')}$$

$$V_0 = f_{MS} + \frac{kT}{q}\ln\left(\frac{8}{dR^2}\right) \qquad d = \frac{q^2 n_i}{kT e_{Si}}$$

$$I_{ds} = \frac{2pR}{(L-\Delta L)}\left[\frac{m_{eff}}{\left(1+d_0\frac{m_{eff}V_{DSx}}{v_{sat}(L-\Delta L)}\right)} + \frac{l_a}{(L-\Delta L)}\right]\left[\frac{2kT}{q}(Q_s-Q_d) + \frac{Q_s^2-Q_d^2}{2C_{ox}} + \frac{kTQ_0}{q}\ln\left(\frac{Q_d+Q_0}{Q_s+Q_0}\right)\right]$$

$$V_{DSx} = F(V_{DS},V_{DSsat})\cdot V_{DSsat} \quad \text{where} \quad F(V_{DS},V_{DSsat}) = 1 - \frac{\ln\left[1+e^{A\cdot\left(1-\frac{V_{DS}}{V_{DSsat}}\right)}\right]}{\ln\left[1+e^{A}\right]}$$

$$\Delta L = L_C\cdot \text{arcsinh}\left(\frac{V_{DS}-V_{DSsat}}{E_{sat}L_C}\right)$$

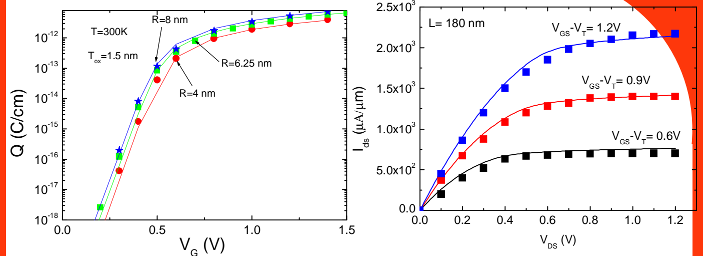
The capacitances of the structure are obtained following reference [2].
Finally, the models for both N-type and P-type SGTs are implemented in Verilog-A [3].

Quantum effects in SGTs

The inversion charge centroid $\mathbf{z_I}$ is modelled to account for the realistic charge distribution [4]. A new gate-channel capacitance model is used, corresponding to a higher oxide thickness, which is corrected to include the inversion charge centroid in the channel.

$$\frac{1}{z_I} = \frac{1}{a+b\times 2\times R} + \frac{1}{z_{I0}}\left(\frac{N_I}{8.26x10^{12}cm^{-2} - 4.9\times10^{18}cm^{-3}\cdot R(cm)}\right)^n$$

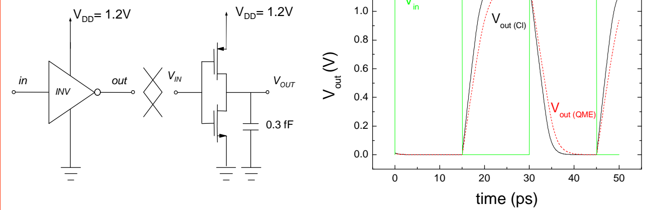
$$C_{Semiconductor} = \frac{e_{Si}}{(R-z_I)\ln\left(1+\frac{z_I}{R-z_I}\right)} \qquad \frac{1}{C_{TOTAL}} = \frac{1}{C_{Oxide}} + \frac{1}{C_{Semiconductor}}$$



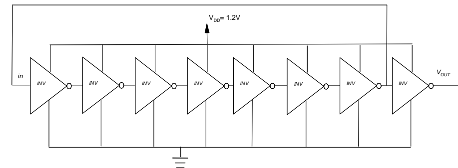
Channel charge at the source for SGTs at room temperature (R=4, 6.25, 8 nm). Simulation results, obtained taking quantum effects into account, (solid lines), modeled data (symbols).

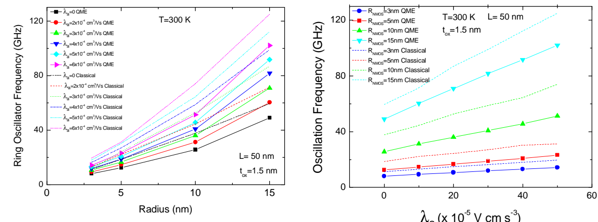
Output curves (normalized to the wire diameter) for a NMOS SGT with R=2.5nm, t_{ox}=9nm, L=180nm and V_T=0.05V. Experimental data reported in reference [5] are plotted in symbols and the drain current results obtained with our model are shown in solid lines.

CMOS inverters and Oscillator rings



Output voltage for a SGT CMOS inverter. The main device parameters are the following: L=50nm, R=3 nm and tox=1.5 nm.





Ring oscillator frequency versus (a) radius and (b) VO parameters, accounting and neglecting quantum mechanical effects. The technological parameters of the SGTs used in the circuit are the following: L=50 nm, tox=1.5 nm.

CONCLUSIONS

A a new model for SGTs was implemented (using Verilog-A) in a circuit simulator (ELDO, Mentor Graphics). The sizing of the transistors has been done by equating the transconductance parameter adapted to the particular geometry of the SGTs.

The influence of QME on the oscillation frequency of a seven stage SGT based oscillator ring has been studied. It can be seen that the inclusion of QME is essential to accurately calculate the oscillation frequency. This is due to the great structural inversion charge confinement produced by the geometrical configuration of these devices.

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