Advances in SOI Compact Modeling

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Rovira i Virgili University (URV), Tarragona, Spain

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Funded by the European project COMON (Compact Modeling Network)

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Outline

Presentation of the COMON project

1. Introduction
2. Charge based compact models
3. Conformal mapping
4. Fourier’s series
5. Conclusions
Outline

Presentation of the COMON project
- Who are we?
- Goals
1. Introduction
2. Charge based compact models
3. Conformal mapping
4. Others techniques
5. Conclusions
EU COMON Project – Who are we?

COMON: COmpact MOdeling Network

🇺🇸 “Marie-Curie”
Industry-Academia Partnership and Pathways project (IAPP FP7, ref. pro. 218255)

✔ Duration:
4 years, started from Dec. 2008.

✔ Coordinator:
Prof. B. Iñiguez
(URV Tarragona)
benjamin.iniguez@urv.cat

More information available on our website: http://www.compactmodelling.eu
EU COMON Project – Goals

- To address the full development chain of Compact Modeling, to develop complete compact models of Multi-Gate MOSFETs (Foundry: Infineon), HV MOSFETs (Foundry: Austriamicrosystems) and III-V FETs (RFMD (UK)).

- Development of complete compact models of these types of advanced semiconductor devices.

- Development of suitable parameter extraction techniques for the new compact models.

- Implementation of the compact models and parameter extraction algorithms in automatic circuit design tools.

- Demonstration of the implemented compact models by means of their utilization in the design of test circuits.

- Validation and benchmarking: compact model evaluation for analog, digital and RF circuit design: convergence, CPU time, statistic circuit simulation.

+ facilitate the mobility of young researchers, secondments of knowledge, organisation of training courses, ...
Presentation of the COMON project

1. Introduction
   - SOI technology
   - Why several gates?
   - Multi-gate SOI structures benchmark

2. Charge based compact models

3. Conformal mapping

4. Others techniques

5. Conclusions
1.1 SOI technology

- Necessity to reduce the gate length while maintaining a good electrostatic control and controlling the leakages
1.1 SOI technology

- Necessity to control the gate length while maintaining a good electrostatic control and controlling the leakages

![Diagram showing SOI technology with labels: Gate, Junction leakages, isolation]
1.1 SOI technology

- Necessity to control the gate length while maintaining a good electrostatic control and controlling the leakages

![Diagram of SOI Technology]

- Junction leakages
- High field effects in the drain
1.1 SOI technology

- Necessity to control the gate length while maintaining a good electrostatic control and controlling the leakages.
1.1 SOI technology

- Necessity to control the gate length while maintaining a good electrostatic control and controlling the leakages
- Isolate the electrically active layer from the bulk
- SOI (Silicon On Insulator) concept

with SOI:
- Reduced parasitic effects – reduction of source/channel and drain/channel capacitances
- Better electrostatic control

SOI allows to continue further the downscaling

Junction leakages
High field effects
In the drain
Subthreshold leakages
1.2 Why several gates?

- Double-gate transistor
- Two conduction channels
  - good $I_{ON}$
- Excellent electrostatic coupling:
  - Short Channel Effects (SCEs) reduction
  - Leakage currents reduction

- But self-alignment of the gates required to maintain Double-gate advantages

  - Idea of vertical gates: FinFET type transistors
1.2 FinFET-like transistors

- **FinFET**: vertical Double-gate
- **Triple-gate** (plus avatars ΠFET and ΩFET)
- **Quadruple-gate** (or GAA), plus Surrounding-Gate FET

Better electrostatic control
## 1.3 (non exhaustive) SOI Benchmark

<table>
<thead>
<tr>
<th>Technology</th>
<th>State of the art</th>
<th>Main advantages</th>
<th>Main drawbacks</th>
<th>Potential for sub 30 nm nodes</th>
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<tbody>
<tr>
<td>Bulk Single-gate</td>
<td>Production</td>
<td>Well known process</td>
<td>Short Channel Effects Control</td>
<td>NO / MAYBE</td>
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<tr>
<td>Strained Single-gate</td>
<td>Development</td>
<td>Increased mobility</td>
<td>Relaxation of strained layers for small dimensions</td>
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<tr>
<td>Partially Depleted SOI</td>
<td>Development</td>
<td>Pragmatic technology</td>
<td>Floating body effects</td>
<td>MAYBE</td>
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<tr>
<td>Fully Depleted SOI</td>
<td>Development</td>
<td>No Floating body effects</td>
<td>Thin and well-controlled thicknesses mandatory, Fringing fields in the BOX</td>
<td>YES</td>
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<tr>
<td>Double-gate SOI</td>
<td>Research</td>
<td>Two channels conduction, Good electrostatic control</td>
<td>Gate self-alignment, Thin channel thickness mandatory.</td>
<td>YES</td>
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<tr>
<td>FinFET SOI</td>
<td>Research</td>
<td>Self aligned technology, Relatively CMOS compatible</td>
<td>Lithographic pitch, Source/Drain Doping, Access resistances</td>
<td>YES</td>
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<tr>
<td>Triple-gate SOI</td>
<td>Research</td>
<td>Three conduction channels, Self aligned technology</td>
<td>Lithographic pitch, Source/Drain Doping, Access resistances</td>
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<tr>
<td>Gate All Around SOI</td>
<td>Research</td>
<td>Good electrostatic control</td>
<td>Not a very pragmatic technology, Source/Drain Doping, Access resistances</td>
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<td>Multichannels</td>
<td>Research</td>
<td>Integration density, Good electrostatic control</td>
<td>Difficult process, Source/Drain Doping, Access resistances</td>
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Presentation of the COMON project

1. Introduction
2. SOI Charge based compact models
   - Surrounding-gate FETs
   - Double-gate transistors
   - FinFETs
3. Conformal mapping
4. Others techniques
5. Conclusions
2.1 Surrounding-gate FETs

➢ 1D Poisson’s equation (no SCEs):
\[ \frac{d^2 \psi}{dr^2} + \frac{1}{r} \frac{d \psi}{dr} = \frac{kT}{q} \delta \cdot e^{-\frac{q(V-V')}}{kT} \]

➢ Solving the 1D Poisson’s equation [Jimenez’04], charge control model obtained:
\[ (V_{GS} - V_0 - V) = \frac{Q}{C_{ox}} + \frac{kT}{q} \log \left( \frac{Q}{Q_0} \right) + \frac{kT}{q} \log \left( \frac{Q+Q_0}{Q_0} \right) \]

➢ Drain current calculation:
\[ I_{DS} = \mu \frac{2\pi R^{\nu_{DS}}}{L} \int_0^{V_{DS}} Q(V)dV \]

2.1 SGFETs- Capacitance modeling

- Analytical expressions [Moldovan’09] of the total electrode charges obtained by integrating the mobile charge density over the channel length. Ward-Dutton partitioning is assumed. Capacitances are obtained by differentiation of total charges.

![Normalized $C_{GD}$ (a, b) and $C_{GS}$ capacitance (c, d) with respect to the gate voltage, for SG MOSFET $V_{DS}=0.05V$ (b,c) and $V_{DS}=1V$ (a,d). Solid line: DESSIS-ISE simulations; Symbol: analytical model. $L=1 \mu m$, $t_{Si}=20 \ nm$, $t_{ox}=2 \ nm$](image1)

![Normalized $C_{DG}$ (a, c) and $C_{SG}$ (b, d) with respect to the gate voltage, for SG MOSFET with $V_{GS}=0$, $V_{DS}=1V$ (a, d) and $V_{DS}=0.05V$ (c, d); $t_{Si}=31\ nm$, $L=1 \mu m$. Solid line: analytical model; Symbols: DESSIS-ISE simulation](image2)

2.1 SGFETs, short channels effects

- Inclusion of SCEs [AbdElHamid’07]:
  \[ \phi(x, y) = \phi_1(y) + \phi_2(x, y) \]
  - \( \phi_1(y) \) Solution of the 1D Poisson’s equation
  - \( \phi_2(x, y) \) Solution of the remaining 2D equation

- Minimum of potential giving threshold voltage \( V_{TH} \) and subthreshold slope SS

DIBL vs. channel length \( L_G \) (radius = 5 and 10 nm).
Comparison between model (lines) and numerical simulations (circles, diamonds)

Subthreshold slope SS vs. channel length \( L_G \)
(radius = 5 and 10 nm). Comparison between model (lines) and numerical simulations (circles, diamonds)

2.3 Symmetrical Double-gate FETs

- Transistor in saturation [Lime’08]:

\[ \phi(x, y) = a + b(x)y + c(x)y^n \]

\[ \frac{\partial^2 \phi}{\partial x^2} - \frac{\phi}{\lambda^2} = 0 \]

with

\[ \lambda = \sqrt{\frac{\varepsilon_{it}t_{it} + \varepsilon_{ox}}{\varepsilon_{ox}}} \]

\[ \frac{1}{2} \left( 1 - \frac{2}{n(n+1)} \right) \]

\[ \frac{1}{2} \left( 1 + \frac{1}{2r} - \frac{1}{n(n+1)} \right) \]

\[ \phi(x = -\Delta L) = \phi_S + V_{\text{deff}} = \phi_{\text{sat}} \]

\[ \frac{d\phi}{dx} \bigg|_{x=-\Delta L} = \frac{k v_{\text{sat}}}{\mu} \]

NMOS: \( k=2 \)
PMOS: \( k=1 \)

Electrostatic potential derived from 2D Poisson’s equation:

\[ \phi(x, y) = \phi_1(y) + \phi_2(x, y) \]

\( \phi_1(y) \) Solution of the 1D Poisson’s equation
\( \phi_2(x, y) \) Solution of the remaining 2D equation

\[ \phi(x, y) = \varphi_{\text{sat}} \cosh \left( \frac{\Delta L + x}{\lambda} \right) + \frac{k v_{\text{sat}}}{\mu} \varphi_{\text{sat}} \sinh \left( \frac{\Delta L + x}{\lambda} \right) \]

Determination of saturated length \( \Delta L \)
2.3 Symmetrical Double-gate FETs

(a) Saturation region length $\Delta L$ vs. drain current $V_{DS}$. ($V_{GS} - V_{TH} = 0.25$ and $0.5V$; $L = 50$nm)

(b) Output conductance $G_D$ vs. drain current $V_{DS}$. $V_{GS} = 0.4, 0.75, 1, and 1.5 V$; $t_{ox} = 2$nm, $t_{Si} = 15$ nm and $L = 50$ nm.

Modeling of the saturation for Symmetrical Double-gate FETs
2.4 FinFETs compact modelling

- Relationship between the charge density and the potentials [Sallese’05][Tang’09]:
  \[ v_g^* - v_{ch} - v_{to} = 4 \cdot q_g + \ln(q_g) + \ln[1 + \alpha \cdot q_g] \]
  with \( \alpha = \frac{C_{ox}}{C_{Si}} \)
  
  *This equation is solved by an explicit algorithm [Prégaldiny’06].

- Drain current expression:
  \[ i = -q_m^2 + 2 \cdot q_m + \frac{2}{\alpha} \ln\left(1 - \alpha \cdot \frac{q_m}{2}\right) \]
  with \( q_m = f(v_g^* - v_{to} - v_{ch}) \)

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Outline

Presentation of the COMON project

1. Introduction
2. Charge based compact models
3. Conformal mapping
   - Application to Fully Depleted single-gate FETs: effect of the Drain through the BOX
   - Symmetrical Double-gate FETs
4. Others techniques
5. Conclusions
3.1 What is conformal mapping?

- **Conformal transformation**: transformation of an analytical function in a complex space:

$$V(x+iy) = W(F^{-1}(x+iy))$$

- Conservation of the Laplace’s equation in the two spaces

  → **Simplification of the geometry possible**

- Application to FDSOI structures:
3.1 FDSOI: effect of the Drain through the BOX

- Penetration of the electric field from the drain into the BOX and the substrate
  - Electrostatic potential at the body-BOX interface modified
  - Because of coupling between back and front channels (Lim & Fossum model), front channel properties degraded

'Drain Induced Virtual Substrate Biasing' (DIVSB) effect [Ernst'99]

3.1 Conformal mapping in the BOX for FDSOI

- **Bidimensionnal case: fully depleted transistor**

\[
\psi_{\text{TOT}}(x, y, V_S, V_D, V_B, V_{G2}) = \psi_{G2}(y, V_B, V_{G2}) + \psi_S(x, y, V_S, V_B) + \psi_D(x, y, V_D, V_B)
\]

- **Superposition theorem:**

\[
\psi_D(x, y) = \text{Re} \left\{ \frac{V_D - V_B}{i\pi} \ln \left[ 1 + \exp \left( \frac{\pi}{t_{\text{BOX}}} \frac{L}{2} \right) \right] \right\} = \frac{V_D - V_B}{\pi} \arctan \left( \frac{\sin \left( \frac{\pi}{t_{\text{BOX}}} \frac{y}{2} \right) \exp \left( \frac{\pi}{t_{\text{BOX}}} \frac{L}{2} \right)}{1 + \cos \left( \frac{\pi}{t_{\text{BOX}}} \frac{y}{2} \right) \exp \left( \frac{\pi}{t_{\text{BOX}}} \frac{L}{2} \right)} \right)
\]

Electrostatic potential modelling in the BOX
3.1 Conformal mapping in the BOX for FDSOI

- Comparing with numerical simulations (using ISE/Synopsis) [Ernst’07]:

![Graph showing electrostatic potential comparison between analytical model and numerical simulations.](image)

**Comparison model / numerical simulations (ISE DESSIS)**

3.2 Application to Symmetrical Double-gate FETs

- In the subthreshold regime (resolution of 2D Laplace’s equation) for Double-gate FETs [Børli’08] and Schottky Barriers DGFETs [Schwarz’09]:

\[ \varphi(u, v) = \frac{1}{\pi} \int_{-\infty}^{+\infty} \frac{v}{(u - \bar{u})^2 + \nu^2} \varphi(\bar{u}) d\bar{u} \]

- Scheme and core formula (‘Poisson’s integral’)

- 2D closed form
- No fitting parameters
- Intrinsically compact expression
- Excellent agreement with numerical simulations

Potential in the channel obtained for a step of gate bias $V_G$ with model (solid lines) and numerical simulations (points). Drain voltage $V_D = 0$ V (a) and 1 V (b). $L_G = 22$ nm, $t_{Si} = 10$ nm.

[Schwarz’09] M. Schwarz et al., to appear in ISDRS’09 proceedings, Dec.. 2009
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1. Introduction
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4. Fourier’s series development
   - Triple-gate FETs 2D interface coupling
   - Π-gate FETs 2D interface coupling
5. Conclusions
4.1 Triple-gate FETs 2D interface coupling

- Resolution of 2D Laplace’s equation using series’s development and Gauss’s theorem at the interfaces:

![Resolution of 2D Laplace’s equation using series’s development and Gauss’s theorem at the interfaces.](image)

- Comparison front-gate threshold voltage $V_{TH1}$ vs. back-gate bias $V_{G2}$ with model (lines) and numerical simulations (squares)
4.2 Π-gate FETs 2D interface coupling

Tranversal cross-section for Triple- and Pi-gate FETs

The process-induced gate overetch in the BOX is improving the device scalability

Subthreshold slope SS vs. gate length $L_G$ for TG and Pi-FETs (from [Park’01])


4.2 Π-gate FETs 2D interface coupling

Comparison front-gate threshold voltage $V_{TH1}$ vs. back-gate bias $V_{G2}$ with model (lines) and experimental measurements (squares) [Ritzenthaler’09]

Perfect agreement analytical model/experimental measurements

4.2 Π-gate FETs 2D interface coupling

- **Coupling coeff.** : slope of $V_{TH1}(V_{G2})$ when the back-gate is depleted.
- **Good agreement** between experimental measurements and model.
- Triple-gate FETs are slightly more sensitive to back-gate influence than Pi-gate FETs.

**Comparison coupling coefficient vs. gate width W using model (lines) and experimental measurements (squares)**

**Comparison front-gate threshold voltage $V_{TH1}$ vs. back-gate bias $V_{G2}$ with model (lines), compact model (dashed lines) and experimental measurements (squares)**

**Compact model of the threshold voltage taking into account the effect of the overetch**
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5. Conclusions

- Recent developments in compact/analytical modeling from COMON partners presented:
  
  ✓ **Compact charge based models** in Multiple-Gate MOSFETs (DG MOSFETs, GAA MOSFETs, FinFETs):
    - A **core model**, developed from a unified charge control model obtained from the 1D Poisson’s equation (using some approximations in the case of DG MOSFETs).
    - **2D or 3D scalable models** of the short-channel effects (threshold voltage roll-off, DIBL, subthreshold swing degradation and channel length modulation), developed by solving the 2D or 3D Poisson’s equation using appropriate techniques.

  ✓ **Conformal mapping** technique presented, with applications to the case of fringing fields in FDSOI, and Schottky Barriers DGFETs.

  ✓ **Series’s development** used to develop compact threshold voltage models for 2D interface coupling in Triple-gate and Pi-FETs architectures.
Thank you for your attention!

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✓ **Tyndall Cork** (Ireland): Prof. J.-P. Colinge
Back-up slides
Triple-gate FETs short channel effects

- Inclusion of SCEs [AbdElHamid’07-2]:
  \[ \phi(x,y) = \phi_1(y) + \phi_2(x,y) \]
  - \( \phi_1(y) \) Solution of the 1D Poisson’s equation
  - \( \phi_2(x,y) \) Solution of the remaining 3D equation

- Conduction path approach and virtual cathode position calculation.

Subthreshold slope SS vs. channel length L<sub>G</sub>. Comparison between model (lines) and numerical simulations (markers)
