MOS-AK Workshop (Baltimore 2009)

Recent Achievements in Verilog-A Compact Modeling

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Outline

- Case study: BSIMSOI
  - Issues
  - Validation
  - Benchmarking
- General Benchmarks
- Verilog-A Guidelines
- Conclusion

BSIMSOI

- **Silicon-on-insulator (SOI) MOSFET model**
  - **Developed by UC Berkeley**
  - **Standardized by Compact Model Council**
  - **28,832 lines (*.c, *.h in 4.2 distribution)**
  - **Numerous bugs**
    - In parameter handling, source/drain swapping, derivatives
    - > 50 found while converting to Verilog-A of which about half were new (not previously reported by EDA vendors)

bsimsoi.va

- **Verilog-A definition of BSIMSOI 4.2+**
  - **Approx. 7100 lines of code (¼ of C code)**
  - **Never any derivative errors**
  - **Approx. 1 month to develop from C code**
    - Perl script to extract and convert
    - Much hand-coding
    - Assistance from Tiburon to find “superfluous assignments” (derivatives)
    - Some compiler improvements
    - Includes time addressing bugs in C code
    - Still faster than typical C model implementation time

bsimsoi.va

- CMC agreed (Sept. 2009) that next release of BSIMSOI would be in Verilog-A
  - Some CMC models were originally in Verilog-A
  - This will be the first to change from Spice C
- Code sent to Berkeley and EDA vendors for validation
  - Thanks to Simucad, Ansoft, IBM for feedback

Compiler Issues

- **`$port_connected`**
  - **BSIMSOI has 3 optional terminals: P, B, T**
  - **Most Spice simulators require all ports of Verilog-A models to be connected**
  - **Compiler must interpret `$port_connected(b)` to mean `b` is an optional terminal**

Compiler Issues, p.2

- Collapsible nodes (switch branches)
  - RGATEMOD allows 0, 1, 2 internal gate nodes
  - RBODYMOD allows 0 or 2 internal body nodes
  - RD/RS can give 2 additional nodes

Other Issues

- **$limit**
  - **Spice C code uses node-based limiting:**

```
vg = B4SOIlimit(*(ckt->CKTrhsOld + here->B4SOIgNode),
                *(ckt->CKTstate0 + here->B4SOIvg), 3.0,
  &Chk)
```

  - **Limiting algorithms typically proprietary**

- **Self-heating parameter update issues**
  - **Rds < 0 because of linear tempco PRT**
  - **Vsat < 0 because of linear tempco AT**

Validation Challenges

- C code is a moving target
  - IBM's "4.2 Production Plus" effort
  - Approx. 30 additional bugfixes beyond 4.2
  - Bug in spice3f5 noise code means reference results are bad
- Reference results must be regenerated for latest C code

Validation: 4.2PP versus 4.1

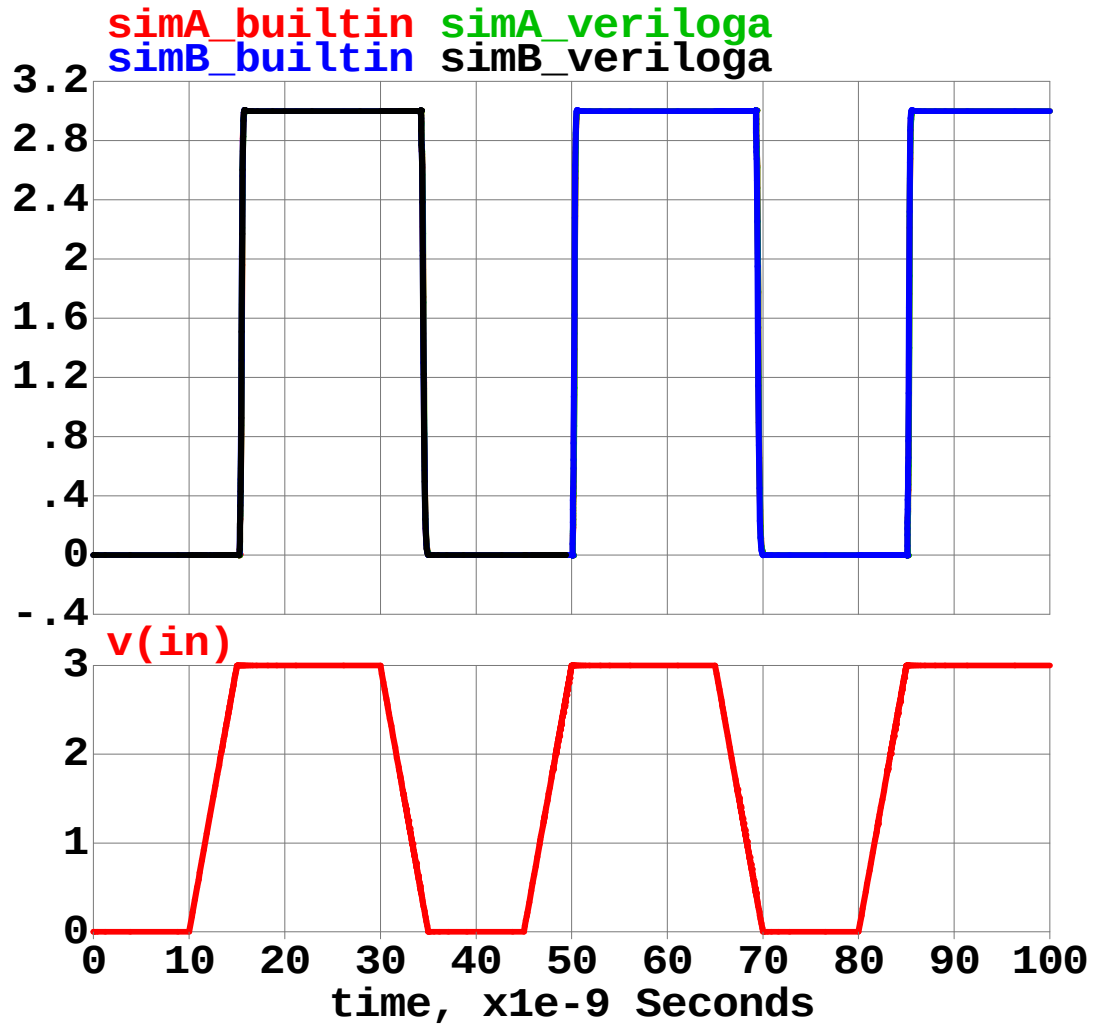
Test	Paramchk=0	Paramchk=1	Why?
dcSweep01	< 0.1%	9%	Rds0<0 at -50℃
dcSweep02	< 0.1%	17%	
dcSweep03	< 0.1%	9%	
acVd01	0.5%	0.5%	
acVd02	0.5%	0.5%	
acFreq01	0.3%	0.3%	
acFreq02	0.5%	0.5%	
noise01	100%	100%	spice3f5 noise bug
noise02	100%	100%	
noise03	100%	100%	

Validation: VA versus 4.2PP

Test	Adice	SimA	SimB
dcSweep01	< 0.001%	< 0.1%	< 0.005%
dcSweep01	< 0.001%	< 0.1%	< 0.005%
dcSweep01	< 0.001%	< 0.1%	< 0.005%
acVd01	< 0.001%	< 0.4%	< 0.001%
acVd02	< 0.001%	< 0.4%	< 0.001%
acFreq01	< 0.001%	< 0.03%	< 0.005%
acFreq02	< 0.001%	< 0.02%	< 0.005%
noise01	< 0.001%	~ 1%	13%
noise02	< 0.001%	~ 1%	13%
noise03	< 0.001%	~ 1%	13%

Benchmarking

- Delay chain similar to circuit from Gilles Depeyrot, MOS-AK Athens 2009
- Using models from CMC QA suite
- SimA, SimB are commercial simulators



Benchmarking, p.2

Circuit	SimA w/ self-heat		SimA w/o SH	
	CPU	Memory	CPU	Memory
400 bsimsoi				
Built-in	78s	39.2MB		
Verilog-A	153s	56.5MB		
Ratio	**1.96x**	**1.44x**		
4000 bsimsoi				
Built-in				
Verilog-A				
Ratio				

Benchmarking, p.2'

Circuit	SimA w/ self-heat		SimA w/o SH	
	CPU	Memory	CPU	Memory
400 bsimsoi				
Built-in	78s	39.2MB	46s	38.5MB
Verilog-A	153s	56.5MB	149s	60.7MB
Ratio	**1.96x**	**1.44x**	**3.24x**	**1.58x**
4000 bsimsoi				
Built-in	539s	74.4MB	541s	74.5MB
Verilog-A	2161s	305MB	2318s	305 MB
Ratio	**4.01x**	**4.10x**	**4.28x**	**4.09x**

Benchmarking, p.3

- Depeyrot, MOS-AK Athens 2009
  - Analyzed Verilog-A to SPICE (built-in hand-coded C) in SMASH and “simulator B”
  - Showed 6x to 40x performance hit!
- Test circuit provided to ADI and re-run in “simulator A”

Benchmarking, p.4

Circuit	Depeyrot		SimA
	CPU time		
400 MOS	7.7x		1.6x
4k MOS	6.1x		1.5x
40k MOS	13.8x		1.7x
	Memory		
400 MOS	1.2x		1.08x
4k MOS	1.7x		1.10x
40k MOS	4.1x		1.13x

Benchmarking, p.5

- ADI has its own Verilog-A compiler
  - Independently developed, not based on ADMS nor Tiburon
  - Generates C code for ADICE
  - Creates dependency tree for model initialization, “static” vs “dynamic” load, noise
- Used for several models, including PSP, MOS20, BSIMSOI
- Benchmarked against hand-coded C for BSIM3

Benchmarking, p.6

Circuit	# BSIM3	Transient CPU		Ratio
		C	VA	VA/C
Simple amp	8	26.3s	25.8s	0.98
PLL	412	566s	540s	0.95
Switch-cap comparator	436	2.40ks	2.44ks	1.02
Sigma-delta modulator	1340	506s	505s	1
ADC front-end	1680	359s	378s	1.05
DCO	4281	1.40ks	1.56ks	1.11

Benchmarking, p.7

- CPU penalty of < 2x is commercially available
- Performance parity is possible
- MCAST (Prof. CJ Richard Shi)
  http://www.ee.washington.edu/research/msca d/shi/mcast.html
  - Automatic compiler beats hand-coded C
  - Reported circa 2004
- No one hand-codes assembly language!

Verilog-A Guidelines

- **Original guidelines: Coram, BMAS 2004**
  - **avoid `analysis()` and `initial_step`**
  - **take care with `ln(x)` `abs(x)` `if()`**
- **Perraud, MOS-AK Strasbourg 2005**
  - **ADMS limitations: no `idt()`, `V(x) <+`**
- **Coram & McAndrew, CMRF 2005**
  - **watch out for `sqrt(x)` near `x=0`**
  - **watch out for integer division: `1/2 = 0`**

Verilog-A Guidelines, p.2

- **Mierzwinski, MOS-AK San Fran 2008**
  - **Tips based on Modified Nodal Analysis**
  - **Suggests using**

```
if (R > 0)
        I(br) <+ V(br) / R;
else
        V(br) <+ 0;
```

(so we assume it's supported by TDA!)

  - **Memory states are almost certainly programming errors in compact models**
  - **Do not use**

```
        I(br) <+ x * ddt(y);
```

(note that `ddt(Q) != V * ddt(C)`)

Verilog-A Guidelines, p.3

- **Depeyrot, MOS-AK Athens 2009**
  - **Focus on Spice integration**
  - **Good points about including P-type equations, operating-point values, noise names**
  - **However: several guidelines violated by BSIMSOI!**

Verilog-A Guidelines, p.4

Depeyrot guideline	**bsimsoi.va**
Limit to the use of `electrical` discipline	Uses `thermal` for self-heating
Avoid collapsing two ports, or one port and the ground	Collapses `t` terminal to ground when RTH=0; May collapse optional terminals `b` and `p`
Do not use system tasks … except `$mfactor`	Uses `$temperature`, `$port_connected`, `$param_given`

Verilog-A Guidelines, p.5

- Some restrictions are critical
- Others are current simulator limitations
- If a feature is necessary for a model, then simulator vendors must address the limitation
  - Thermal discipline in Spice netlist
  - `$port_connected`
  - Collapsing multiple internal nodes to one port

Conclusion

- Verilog-A is increasing its “market share”
- Writing a good compact model still requires care and rigor
- Simulator vendors have work to do
  - 1x has been demonstrated

More Information

- Verilog-A model library at http://www.designers-guide.org/VerilogAMS/
  - VBIC, MOS11, JFET, etc.
  - Also, forum for asking questions
- PSP http://pspmodel.asu.edu
- Mextram http://mextram.ewi.tudelft.nl/
- bsimsoi.va available from Berkeley
- Silvaco/Simucad has models available "for non-commercial use"