COMPACT MODELING OF PLANAR AND VERTICAL TUNNEL TRANSISTORS

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OVERVIEW

• SECTION-1: DEVICE STRUCTURE AND OPERATION

• SECTION-2: PERFORMANCE ANALYSIS

• SECTION-3: MODELING IN VERILOG-A FOR LOGIC AND MEMORY APPLICATION
MOSFET

MOSFET Energy Band Diagram
TFET

TFET Energy Band Diagram
Vertical Interlayer Tunneling FET

Vertical iTFET

Vertical iFET Energy Band Diagram
Existing Vertical Interlayer Tunnel Transistors

- Fallahazad et al. *Nanolett.*, 15, 2014
Pros and Cons of Vertical Interlayer TFETs

Pros:
• Atomically thin vertical heterostructures.
• Flexible and transparent
• THz operating frequency

Cons:
• Strong negative differential resistance (NDR) observed
• Resonant tunneling occurs
• Very low drain current (pA or nA)
• Good for high frequency operation but questionable for logic applications
Alternative Current Transport Technique


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Alternative Current Transport Technique

Interlayer Tunneling Based Channel Barrier Control

Current Transport Model

Performance Estimation

- Britnell et al. Science, 335, 2012
- Roy et al. Microelec. Rel. 109, 2013
- Roy et al. APL, 104, 2014

Graphs illustrating the performance of transistors with various parameters and equations.
Logic Application
MoS$_2$ in place of graphene

Performance Estimation of MoS$_2$-hBN-MoS$_2$ Vertical iTFET

- Drain Current $I_D$ vs. Drain Bias $V_{DS}$
- Capacitance vs. Gate Bias $V_G$
- Cut-off Frequency $f_T$ vs. Gate Bias $V_G$

Diagrams showing various parameters and characteristics of the MoS$_2$-hBN-MoS$_2$ Vertical iTFET, including temperature effects and device performance metrics.
Compact Modeling in Verilog-A through Mentor Graphics Tanner Tool

1. New Devices
2. Mathematical Equations
3. SPICE Code
4. New Simulators
5. New Simulators Installation
6. Design Kits and Model Libraries for Designers
7. Physics Based Compact Equations
8. Compile the equations in Verilog-A through S-Edit
9. Generate a symbol for that device through S-Edit
10. Use that symbol to draw circuit schematic through S-Edit
11. Simulate the circuit schematic in T-Spice
12. Waveform generated in W-Edit for analysis
13. The cell of the new device ready for any circuit analysis
Case study: GNR TFET Logic Inverter

- Physics based compact model:

\[
I_D = \frac{\mu_c C_m (V_{GS} - V_{TH})}{l_{ox}} V_I T_{WKB} \left[ -\ln \left(1 + \exp \left(\frac{V_{GS} - V_{TH} - V_{DS}}{V_T} \right) \right) \right] + \ln \left(1 + \exp \left(\frac{V_{GS} - V_{TH}}{V_T} \right) \right) + \ln \left(1 + \exp \left(\frac{V_{DS}}{V_T} \right) \right) - \ln(2) + \frac{q^2}{\pi h} V_T \exp(-\frac{\phi_{BL}}{V_T}) \left( V_{DS} - V_{TH} \right) \]

- Numerical simulation: using open source simulation tool NanoTCAD ViDES

Model Integration into Verilog-A

• Symbol generated for each of this GNR TFET Verilog-A codes.
Model Integration into Verilog-A

- Spice netlist generated and simulated in Mentor Graphics T-Spice.
Model Integration into Verilog-A

- Transfer characteristics of both n-type and p-type GNR TFET are plotted
Model Integration into Verilog-A

• Output characteristics of both n-type and p-type GNR TFET are plotted
Comparison with Verilog-A

- Physics based analytical model matches with Verilog-A simulation.
- The Verilog-A device becomes suitable for circuit design.
Performance of GNR TFET Logic Inverter

- Power dissipation 2.09μW at 0.1V and 1GHz
- At 0.1V, the delay is still less than 100ps
- The delay is only 12.5ps for load capacitance of 1pF

Fahad et al., IEEE iNIS, Gwalior, India, 2016
GNR TFET 6T-SRAM DESIGN

![GNR TFET 6T-SRAM Diagram](image)

**GNR TFET 6T-SRAM READ SNM**
- $V_Q [V]$: 0.372 mV

**GNR TFET 6T-SRAM WRITE SNM**
- $V_Q [V]$: 1.237 mV
Graphene iTFET NAND2 Design

\[ V_{DD} = 0.5V \]

Rise and Fall Time = 1ps
Delay = 20ps
Graphene iTFET 6T-SRAM Bitcell Design

Graphene iTFET 6T-SRAM Read SNM

Graphene iTFET 6T-SRAM Write SNM

251mV

490mV
Summary

• Promise of alternative current transport mechanism in MOSFET has been explored named as iTFET.

• Verilog-A serves as extremely useful tool for circuit level exploration of these new devices.

• Though “i” refers for “interlayer”, we conclude “i” for “intelligent” since more than Moore era would only recognize “intelligent” transistors!
THANK YOU