The Robuspic Project – An Overview

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- on behalf of all partners -
The Robuspic Project – An Overview

- Motivation
- Organization
- Work Packages
- Results
- Conclusion
Robuspic - Motivation

Smart Power circuits...

... typically combine:

- Highly accurate analog circuitry
- Digital signal processing
- Driving heavy loads

... operate in an uncontrolled environment

- Extended Temp. range
- E-M disturbances

... should have good, predictable reliability in harsh environment

... should have competitive cost
ROBUSPIC: Robust Mixed Signal Design Methodologies for Smart Power ICs

- An Information Society Technologies Project Funded by the European Commission in Framework 6
- Duration: December 2003 until November 2006
Robuspic - Organization

→ Partners:

- AMI Semiconductor (Belgium, Project Leader)
- Cadence (France)
- Cambridge Semiconductors (UK)
- EPFL (Switzerland)
- University of Cambridge (UK)
- IMEC (Belgium)
- KU Leuven (Belgium)
- University of Zagreb (Croatia)
- Robert Bosch GmbH (Germany)
ROBUSPIC – Work Packages

→ WP1: Compact Models
  - Development of L- and VDMOS models based on the EKV approach for the channel region
  - Development of LIGBT models
→ WP2: Reliability
  - Investigation of degradation mechanisms at DMOS and LIGBTs
  - Development of aging models
→ WP3: Sensitivity Modeling
  - Model extensions for matching, process and layout sensitivities
→ WP4: System Level Aspects
  - Methods for fast simulation on system level
  - Electro thermal simulation
  - Simulation of EMC
→ WP5: Validation
  - Assessment of gain in simulation accuracy & speed
VDMOS Transistor - Schematic Cross Section

- Source = Body
- Gate
- Drain
- Substrate
LDMOS Transistor - Schematic Cross Section

Source = Body
Gate
Drain
Substrate
LIGBT - Schematic Cross Section

Cathode

Gate

Anode

p+

Pwell

n-Drift

Drain MOS = Base Bipo

n+

p+
DMOS Model Approach

- Base: EKV V2.6 for Channel Region Modeling
- Drift Region modeled by voltage dependent resistor
  - Correct modeling of « quasi-saturation »
- EKV formulation modified for charge calculation
  - Correct modeling of bias-dependent capacitances
- Self heating effects included
- Different geometry scaling for L- and VDMOS devices
DMOS Model Approach

- 8 EKV model parameters (channel region)
- 12 Drift region parameters ($R_D$, $C_{GD}$)
- 4 thermal parameters
- 3 self heating parameters
- 4 impact ionisation parameters
- 8 (+x) parameters for parasitics
Work Package 1: Modeling

Transfer ($I_D-V_G$ and $g_m-V_G$)
$N_F=2$, $T=30\,^\circ C$, $\#W$

- Correct $W$ scaling for transfer and output characteristics, including $g_{m\_max}$ and Self Heating
Work Package 1: Modeling

LDMOS Capacitances: Model (red) vs Measurement (black)

$C_{GD}$ vs. $V_D$ for $V_G=0V$

$C_{GG}$ vs. $V_G$ for $V_D=0V$
LIGBT Model

- Based on Hefner model for vertical IGBTs
- Modifications for lateral IGBTs to account for differences in
  - Carrier dynamics
  - Terminal capacitances
  - Substrate effects
  - Parasitic effects (resistor, JFET)
- Development by use of TCAD simulations & measurements at devices fabricated at CamSemi (SOI & junction isolated)
- Implementation in Pspice and Verilog-A
LIGBT – Equivalent Circuit
Work Package 2: Reliability

- Investigations of devices under static and dynamic stress conditions
  - Temperature range -40 to 200°C
  - Consideration of process deviations
  - Identification of main stress mechanisms, also by use of TCAD

- Development of degradation models for DMOS and LIGBT device parameters (HCl)

- Implementation into the circuit models developed in WP1

- Development of supplementary circuits for life condition monitoring
Work Package 2: Reliability

Circuit Simulation (typical application)

Age Model:
Age = f(Operating Conditions, Time)

Degradation Model:
Model Parameter Drift = f(Age)

Simulation of aged Circuit (by adapted model Parameters)
Topics addressed in this work package:

- Investigation of process parameter variations on on-state performance
- Extension to statistical model
- Matching (Mismatch models for L- and VDMOS)
- Scaling: Investigation of several scaling options (e.g. fingers or cells) for both DMOS and LIGBT
Work Package 4: System Level Aspects

- Investigation of Methods to speed up simulation of smart power circuits
  - Automatically generated “Black Box Models” for circuit blocks
  - Transistor Level Simulation using Fast Spice Simulators
- Development of Methods for Electro-Thermal Simulation
  - Package modeling
  - Scalable thermal impedances of power devices
  - Coupled electro thermal simulation
- Development of models and methods for EMC simulation
Work Package 4: System Level Aspects

f=10KHz, $V_{ac}=1.0\, V$, $V_{dc}=1.0\, V$
$R_F=100\, \Omega$, $R_I=1300\, \Omega$

“Black Box” Model Approach:
Model Generation by training of artificial neural networks

ANN model

Output from ANN model (♦)  Output from compact model (■)
IC level EMC

EME and EMI HTVD measurement system

EMC test chip

Comparison of the EM emission before and after the optimization

Interface for EMC simulations in Cadence environment

EMC aware circuit optimizations

Automotive Electronics
Derivation of Scalable Model for Thermal Device Impedance

Thermal Simulation Result:
Thermal Impedance vs time for 3 device mounting conditions
Work Package 5: Validation

- Implementation of DMOS and LIGBT models into design environments
- Selection of demonstrator circuits
- Implementation of methods into the industrial design flows
- Assessment of new models and methods regarding accuracy and performance
Work Package 5: Validation

DMOS model implementation

Verilog-A
Simulator: Eldo
EPFL

Direct transfer

Verilog-A
Simulator: Spectre/UltraSim
AMIS/Cadence

C
AHDLCMI

Translation

C-Core
MAST-Shell
Simulator: Saber
Bosch

Automotive Electronics

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Robuspic - Highlights

- Scalable models for LDMOS, VDMOS, SOI LIGBT available
- Self heating effect included
- Extension with parasitic bipolars implemented
- DMOS Degradation investigated, analytical aging formulation and parameter degradation models available
Robuspic Workshops:

June 2005 at ISIE Dubrovnik
Planned: June 4th, 2006 at ISPSD Naples
Planned: September 22nd, 2006 at ESSDERC Montreux

Robuspic Website:
http://www-g.eng.cam.ac.uk/robuspic/