Lumped Element
High Voltage
MOS Model

presented by
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The Devices:
  Types and Construction

DC Model:
  Mathematical considerations, types

AC Model:
  Non diode variable "gate" capacitance

Ring Oscillator Test Bench:
  A challenge for the simulator

Outlook
The goal is to show an extension to the BSIM3v3 model which can be simulated by a standard Spice simulator.

At the time of development a VerilogA formulation was not intended.

The model shows a more accurate description of the so-called quasi saturation effect.

A better description of the LDDMOS drain overlap capacitance is considered.
High Voltage Drain Extension MOS Cross Section

- BULK
- SOURCE
- GATE
- DRAIN

Si depth / µm

Position / µm

Net Doping (/cm³)
- 1E20
- 1E18
- 1E16
- 1E14
- 1E12

watch the scaling
Two Types of Drain Extension MOS

Extension region at drain
Circuit with drain resistance and parasitic elements (BJT, substrate resistance)

Name: Extended Drain MOS
XDMOS

N-Well as drain extension
Two Types of Lateral Diffused Drain MOS

Diffused drain with lateral drain connection

Name: LDDMOS or LDMOS

Diffused drain with vertical drain connection

XD_10 with up to 650 V LDMOS transistors
Agenda (2)

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> Outlook
First Generation HV MOS Model

> MOS transistor with serial resistor

The model does not take into account the quasi saturation effect.

- good model accuracy for low gate voltages
- drain current saturation effect at high VGS and VDS not included
- fast simulation speed and good convergence
Second Generation Behavioural HV MOS

- MOS transistor with serial resistor and voltage controlled voltage source

The quasi saturation is modeled with acceptable accuracy (green).

- Core devices MOS and Rds identical to HV model
- Several parameters for VCVS added
- Good model accuracy, error less than 10%
- Higher simulation time
- Simulation convergence problems more likely
Function Requirement for the Voltage Source

Demands on the behavioral current function:
- The function should be monotone (not necessarily).
- The first and second derivative must be continuous.

Function needed for the voltage source:

\[ F(V_1, V_2, \ldots) \]

\[ \frac{\partial^2 F}{\partial V^2} \text{ should not have a kink} \]

The voltage source acts

Maximum voltage to avoid reverse current

Voltage drop @ resistor.
> Improved accuracy has its price:
  3 auxiliary networks, 7 parameters, several additional elements

\[ \text{evd} = \max(\text{sgn}(v(d,s)),0) \times \max(\text{sgn}(v(g,s)),0) \times \min(v(7),v(6),v(d,s)) \]

> Auxiliary Networks:

- **TC network**
  - \( R = 1k \)
  - \( tc1 = 5.5E-3 \)
  - \( tc2 = 1.2E-5 \)

- **Main formula**
  \[ ev = (kpv(5)^3 + kp4v(5)^4 + kp5v(5)^5) \times f(v(g,s),k1h,kgs) \times f_{\text{limit}}(v(d,s),kds) \]

- **ev5**
  \[ ev5 = \frac{v(d,9)}{(v(7) + 1E-6)} \]
MOS transistor with serial resistor and voltage controlled current source

- core devices MOS and Rds identical to HV model
- added fly back diode due to device construction
- improved accuracy compared to the voltage source model
- shorter simulation time
- capacitance modeling difficult in case of LDDMOS
Function Requirements for the Current Source

The function for the current in the drain extension region

Variations ...

Resulting resistance

\[ F(V_1, V_2, \ldots) \]

\[ \frac{\partial^2 F}{\partial V_i^2} \] must not have a kink
Behavioural Current Source Model

- Less auxiliary sources, improved TC modeling.
- More compact model, all effects in a few equations.
- Improved convergence, fewer parameters (5).

\[ I(g_{11}) = \frac{v(11,12)}{v(102) \times 1 + \sqrt{1 + \frac{v(11,12)^2}{v(101)^2}}} \]

Gate Voltage influence:
\[ I = f(v(2,3), a, b, c) \times v(102) \]

\[ I = R_{02} \]

R = 1
\[ tc_1', tc_2' \]

\[ 1G \]
\[ 1f \]
Gm and Transconductance Example

Plot nd25c_x1/x0y3/idvg_40/

Id [1E-3]

red: measured
green: simulated
Gds and Ron accuracy

Plot nd25c_x1/x0y3/idvd_40/Ron (Off)
The below plot shows clear self heating: a "falling" current trace in the saturation region.

To include this effect into the model, it needs a temperature node and additionally ...

A thermal resistance / capacitance network. It's not yet implemented in the model.
Introduction to Self Heating

> Simple thermal network added for self heating:
  - Voltage [V] ∆ Temperature [K]
  - Current [I] ∆ Thermal Current [J/s=W]
  - Resistance [Ω] ∆ Thermal Resistance [K/W]
  - Capacitance [C/V] ∆ Thermal Capacitance [J/K]
  - Charge [C] ∆ Energy [J=Ws]

> The thermal power equals the electrical power loss.
Agenda (3)

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A capacitance, which depends strongly from the drain voltage, develops if the gate overlaps the drain extension region.

This is true for the LDDMOS type MOS with Trench isolation.

Fortunately it does not occur in the standard CMOS technologies, e.g. xc06.
For the LDDMOS of the XD?10 technology a (variable) capacitance has to be added in the drain to gate path. It can not be decided by CV measurement which node has to be occupied to get a good fitting transient respond.
This model is not yet implemented in X-FAB's HV models, ongoing work.

This is the drain/gate overlap capacitance, which has a diode like CV trace.

This is the reverse diode, which is easily modeled.

constant cap @ drain (purple)

improved model (green)
The capacitance is modeled in an auxiliary circuit. The current is mirrored back into the current controlled current source between the drain and gate node. This is fine for stand alone AC simulation but proved as not converging in the ring oscillator test.

An alternative model is in development. It uses function controlled sources instead of diodes to modulate the CV characteristic.
> The Devices: Types and Construction

> DC Model: Mathematical considerations, types

> AC Model: Non diode variable "gate" capacitance

> Ring Oscillator Test Bench: A challenge for the simulator

> Outlook
The Model is tested regarding convergence.
DC check with extended voltages.
Transient analysis with ring oscillator as benchmark.

Simulation health check with high gate and drain voltages:

I will show two bad examples from the time of model development on the next slides ...
Adverse effect of high drain voltage on the effective gate voltage: The model is not physical.

Initially the model was extracted at low gate / drain voltages. ➔ It was not sanity checked.
Non physical convergence found by the simulator:

Negative drain current in the simulation due to a reversed voltage in the drain voltage source. This can occur if the mathematical formulation is not monotone or no cautions are taken against nonphysical results.

The simulator finds convergence even with the impossible ...
Ring oscillator with 25 stages

In this case NMOS and PMOS HV model.

Alternative if only NMOS (PMOS respective):
The transient analysis simulation time is considerably longer compared to the simple resistor model.

<table>
<thead>
<tr>
<th>Model Type</th>
<th>CPU time [s]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple resistor @ drain</td>
<td>2.52</td>
</tr>
<tr>
<td>Resistor with behavioural voltage source</td>
<td>36.41</td>
</tr>
<tr>
<td>First Current Source Model</td>
<td>133.35</td>
</tr>
<tr>
<td>Improved Model, changed maths</td>
<td>47.94</td>
</tr>
<tr>
<td>Final Behavioural Current Source Model</td>
<td>40.24</td>
</tr>
<tr>
<td>Model with CV modelling (diodes)</td>
<td>not converg.</td>
</tr>
</tbody>
</table>

Factor 15 to >50 depending on the mathematics behind the model.

The challenge is the transient analysis.

AC and DC analyses are more robust regarding convergence.
### Agenda (5)

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- **Ring Oscillator Test Bench:**
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- **Outlook**
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<td><strong>Plans for Enhancement of the HV Model</strong></td>
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> Improvement of the Capacitance Model.

> Test of Capacitance and Reverse Diode Model with transient measurement and simulation. (TT problem)

> Further simplification of the mathematical description for better convergence.

> Consideration of self heating effects.

> Why not VerilogA?  
Most of the Simulators cope with it nowadays.  
It would made the formulation much simpler.
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and ...

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http://www.xfab.com