Scalable Electrical Model for a SOI-RF-LDMOS Including Drain Drift Region Resistance Self-Heating Effects

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Outlines

- Introduction
  - Work background
    - application, technology etc.
- Modeling self-heating effects
  - Choice of electrical and thermal model
  - Thermal parameters relationships, principles and assumptions
- Model description
- Results
- Conclusions
Introduction

Purpose
- An electrical model which includes thermal behaviors of intrinsic MOS and its drift region, and represents the best compromise among accuracy, simulation time and difficulty of extraction.

Device and Process
- $n$-channel RF-LDMOS
- SOI-C-RF LDMOS 8 Technology

Application
- Power amplifier for cellular phones

Advantages and Drawbacks for SOI Technologies
- Advantages: no parasitic effects through the substrate thanks to buried oxide (BOX). More performing devices.
Modeling Self Heating Effect

- Model for Intrinsic MOS w/ thermal node
  - Berkeley BSIMSOI

- Heat spreading model
  - 3D distributed thermal network
    - Best of Accuracy
    - Physical simulation (not our case)
  - Vertical distributed thermal network
45° heat spreading Distributed Model

\[ \Sigma = \frac{R_{1,2} R_{1} R_{2}}{R_{1} + R_{2}} \]

\[ C_{1,3} = \frac{1}{6} c_{TH} \cdot h \cdot \Sigma \]

\[ C_{2} = \frac{2}{3} c_{TH} \cdot h \cdot \Sigma \]

- \( C_{th} \) well defined
- Good accuracy in transient
- Big simulation time

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FTM-SP&HV-Device Char. & Model.
MOS-AK Workshop
Modeling Self Heating Effect/2

For RF application (GHz), $C_{th}$ is insensitive

A simple thermal RC seems to be convenient:

- Advantages: Simulation time
- Drawbacks: Lower accuracy in transient simulation, not needed in RF simulation
- $R_{th}$ can be easily calculated
  \[ R_{th} = R_{th_{Si}} + R_{th_{ox}} + R_{th_{Sub}} \]
**Thermal Capacitance Extraction**

- Based on simulations
  - Transient analysis on a power step response of a RC circuit.

![Diagram of RC circuit](image)

\[ V(t) = P \cdot R_{th} \cdot (1 - e^{-t/\tau}) \ \ [°C] \]

\[ \tau = R_{th} \cdot C_{th} \ \ [s] \]

- Power generated by DMOS model:
  - \( I_{PR} \) [W]: Total dissipated power on drain/source series resistances
  - Assumption: 90%ΔT of Distributed RC is equivalent of single RC
Power Step response for a distributed thermal network

\[ \Delta T = P \cdot R_{th} \]

\[ tr : 90\% \Delta T \]

T_{cx}=1\mu m, T_{si}=3\mu m

90\% \Delta T

Steady state

Device temperature [\degree C]

Time [\mu s]

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**Cth Extraction/ formulae**

- **Injected power**
  \[ I_{PR} = I_D(V_D - V_{CH}) + R_{SMET} \cdot I_S^2 \]

- **Temperature @ node T**
  \[ V(t) = P \cdot Rth \cdot (1 - e^{-t/\tau}) \]  \[ \Delta T = P \cdot Rth \]

- **tr calculation**
  \[ 0.9 \cdot \Delta T = \Delta T \cdot (1 - e^{-tr/\tau}) \]  \[ \tau = Rth \cdot Cth \]  \[ tr: 90\% \Delta T \]

- **Cth calculation**
  \[ Cth = \frac{tr}{Rth} \cdot \ln 10 \]
Model Scalability

Sub circuit is composed by

- Intrinsic MOS
  - BSIMSOI -> scalable
- Drain drift resistor $f(w)$
- Metal resistors $f(w, area)$
- $R_{th} f(w, area)$
- $C_{th}$ expression is extracted from $tr$ vs. $w$ fitting

\[
tr = T_{w_1} \cdot w + T_{w_2} \cdot \left[ 1 - \frac{T_{w_3}}{w^{xtp}} + T_{w_3} \right]
\]

Fitting parameters: $T_{w_1}, T_{w_2}, T_{w_3}, xtp$
(square device)
SOI-C-RF LDMOS

- M1: Berkeley BSIMSOI
- GNL: VCCS
  \( f(V(T), V(7-CH), V_{GS}) \)
- \( R_{Conv} \): convergence Resistor
- \( R_{D_{lim}} \): \( n^+ \)-layer resistance
  \( f(V(T)) \)
- \( R_{D_{Smet}} \): metal pattern resistance
  \( f(\text{layout parameters}) \)
- \( R_{Ge} \): Poly-Gate resistance
- \( D_{BD} \): Body-Drain diode
SHE Effects simulation comparison

$V_{GS\ min} = 0.8\text{V}$

$V_{GS\ max} = 3.3\text{V}$

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All SHE ON

All SHE OFF

Exp.

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DRAIN-SOURCE VOLTAGE (V)

DRAIN CURRENT (mA)
Drain Rdrift w/ and w/o SHE

- Rdrift w/o SHE
- All SHE ON
- Exp.

Graph showing the relationship between drain current (mA) and drain-source voltage (V) with different gate voltages (V_{GS}) ranging from 0.8V to 3.3V, for a channel width (w) of 27µm.
SHE on RF simulation performances
Model Scalability Accuracy

\[ w(\mu m) \quad 7 \quad 14 \quad 52 \quad 105 \]
Conclusions

- A fully scalable electrical model which takes into account self heating effects of a LDMOS has been extracted.
- The thermal effects of the resistance of drain drift region have been modeled and successfully included in the model.
- The presented approach on extracting an electrical model which take into account SHE by mean of a simple RC is very satisfying thanks to the results obtained in terms of accuracy and scalability.
References


On line documentation:
- www-device.eecs.berkeley.edu/~bsimsoi/