Recent Enhancements in BSIM-IMG

BSIM-IMG: Industry Standard Model with Fast and Extended Range Core Including Improved Mobility and Noise models

Chetan Kumar Dabhi*, Pragya Kushwaha, Harshit Agarwal, Juan Pablo Duarte, Yen-Kai Lin, Yogesh Singh Chauhan*, Chenming Hu

*IIT Kanpur, India
University of California, Berkeley

MOS-AK, Chengdu
Difficult to suppress leakage in Scaled MOSFET

- Need a thinner Oxide to suppress the leakage
- Gate Leakage is the Issue!

Solution:
Leakage is suppressed by multi-gates

Scale body thickness instead of Oxide thickness

**Examples of Multi-Gate**

- Thin channel for (fully depleted) better gate control and Short channel effect (SCE)
- Better gate control $\rightarrow$ Better transistor scaling

*Fully Depleted Silicon-on Insulator (FDSOI)*

**UC Berkeley - MOS-AK, Chengdu**
Scaling: CMOS Solution

- **2003**: 1.2 V (Ghani, IEDM 03) Strain Eng.
- **2005**: 1 V (Tyagi, IEDM 05) Contact resistance
- **2007**: 1 V (Mistry, IEDM 07) High K metal gate
- **2009**: 1 V (Packan, IEDM 09) RSD
- **2011**: 0.9 V (Q. Liu VLSI 2011) RSD-FDSOI
- **2012**: 0.7 V (UC Berkeley) ETSOI Si

**2003 - 2012**

- **90 nm**
- **65 nm**
- **45 nm**
- **32 nm**
- **22 nm**

**Multi-Gate**

- **2014**: 0.7 V (2nd Gen. FinFET) [14 nm - FinFET, IEDM-14] Fin doping and profile opt.
- **2014**: 1.2 V
- **2014**: 1 V
- **2014**: 0.9 V

**BSIM-IMG Developed for FDSOI Multi-gate MOSFET**
Outline

- BSIM-IMG: Independent Multi-gate MOSFET Model
  - Fast core Model
  - Extended Range Core Model

- Channel current, Charge and Capacitance Model
- Dual Mobility Model: $g_m$ Double Hump Behavior
- Developed Noise Models in BSIM-IMG
BSIM-IMG: Independent Multi-gate MOSFET Model

- Separate front and back gates
- Asymmetrical gate stack: $T_{ox}$, Work-function etc.

Physical surface-potential-based core I-V and C-V model agrees with Numerical Solution without fitting parameters for surface potential
Fast Core Model

Solving Poison’s eq. in silicon body

\[
\left( C_{ox1} \frac{V_{fg} - \Delta \phi_1 - \psi_{s1}}{\varepsilon_{Si}} \right)^2 - \left( C_{ox2} \frac{V_{bg} - \Delta \phi_2 - \psi_{s2}}{\varepsilon_{Si}} \right)^2 = \frac{2qN_c V_{th}}{\varepsilon_{Si}} \left[ \exp \frac{\psi_{s1} - V_{ch}}{V_{th}} - \exp \frac{\psi_{s2} - V_{ch}}{V_{th}} \right].
\]  

\[ \psi_{s2} = \frac{C_{Si}}{C_{Si} + C_{ox2}} \psi_{s1} + \frac{C_{ox2}}{C_{Si} + C_{ox2}} (V_{bg} - \Delta \phi_2) \]  

Considering back gate in weak inversion

Solving (1) with proper initial guess, and using Helly’s algorithm: Analytical Surface potential

[S. Khandelwal et. al., TED, 2012]
Extended Range Core Model

Solving Poisson’s eq. for undoped silicon body
\[
\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho(\psi)}{\varepsilon_{ch}} = \frac{q n_i}{\varepsilon_{ch}} e^{\frac{\psi - V_{ch}}{\nu T}} \quad \tag{1}
\]

Integrating Poisson’s for front and back gate
\[
\alpha^2 = k_f (x_f - \varphi_f)^2 - A_0 e^{\varphi_f} \quad \tag{2}
\]
\[
\alpha^2 = k_b (x_b - \varphi_b)^2 - A_0 e^{\varphi_b} \quad \tag{2}
\]

Integrating electric field and using boundary cond.
\[
\alpha \coth(\alpha/2)(k_f (x_f - \varphi_f) + k_b (x_b - \varphi_b)) + k_f k_b (x_b - \varphi_b)(x_f - \varphi_f) + \alpha^2 = 0 \quad \tag{3}
\]

\[
f(\varphi_f) = (k_f (x_f - \varphi_f) + \alpha \coth(\alpha/2))(k_f (x_f - \varphi_f) + k_b (x_b - \varphi_b)) - A_0 e^{\varphi_f} = 0
\]

\[
\varphi_b = \varphi_f - \ln(k_f (x_f - \varphi_f) + \alpha \coth(\alpha/2)) + \alpha \coth(\alpha/2) + \ln \left( \frac{\alpha}{\sinh(\alpha/2)} \right)^2 \quad \tag{4}
\]
Extended Range Core Model: Analytical Solution

Maximun front surface potential $\varphi_{f,max}$ (28) → Physics based initial guess $\varphi_{f,guess}$ (29) → Iteration calculation for: $f(\varphi_f) = 0$ (30) → $\varphi_f$, $\varphi_b$

\[-4\pi^2 = k_f (x_f - \varphi_{f,max})^2 - A_0 e^{\varphi_{f,max}} \tag{5}\]

$\varphi_{f,guess} = \max_s \left( \frac{r \cdot EOT_f (x_f - x_b)}{T_{fin} + r(EOT_f + EOT_b)} + x_b, \varphi_{f,max} \right) \tag{6}\]

Solving (6) and using proper initial guess in Newton raption algorithm:

Analytical Surface potential of (4) is obtained
Channel current, Charge and Capacitance Model

Extended Range Core Model

Fast Core Model

I-V Validation

Terminal Capacitances

MOS-AK, Chengdu
Dual Mobility Model: $g_m$ Double Hump Behavior

\[ \mu_{t,\text{eff}} = w \cdot \mu_{\text{eff},fg} + (1 - w) \cdot \mu_{\text{eff},bg} \]

$W$ is the weighting function
The major sources of noise in a transistor are the thermal noise and the flicker noise.

Flicker Noise: Created by carrier trapping and de-trapping.

Thermal Noise: Created by random motion of carriers due to thermal excitation.
Thermal Noise Models in BSIM-IMG

Earlier models only uses front gate for thermal noise PSD calculation

\[ S_{id^2} = \frac{4K_BT}{I_D L_{vsat}^2} \int_0^{V_{DS}} g^2(V) \cdot dV \]

\[ g(V) = wC_{ox1}V_t(\mu_f q_f(v) + K\mu_b q_b(v)) \]

Performing integration

\[ S_{id^2} = \frac{4K_BT C_{ox1} V_t^3}{I_D L_{vsat}^2} \left( A_1 + B_1 + C_1 \right) \]

\[ A_1 = \mu_f^2 (q_{fs} - \beta q_{fd}) \left( \frac{q_{fs}^2 + q_{fs}q_{fd} + q_{fd}^2}{3} + \eta_f \frac{q_{fs} + q_{fd}}{2} \right) \]

\[ B_1 = K^2 \mu_b^2 (q_{bs} - \beta q_{bd}) \left( \frac{q_{bs}^2 + q_{bs}q_{bd} + q_{bd}^2}{3} + \eta_b \frac{q_{bs} + q_{bd}}{2} \right) \]

\[ C_1 = 2K \mu_f \mu_b q_{ba} (q_{fs} - \beta q_{fd}) \left( \frac{q_{fs} + q_{fd}}{2} + \eta_f \right) \]

Front gate contribution
back gate contribution
coupling contribution
More inversion charges as $V_{gs}$ increases, more scattering, thermal noise

- $+ V_{bg} \rightarrow V_t \rightarrow$ more carriers $\rightarrow$ noise
- $+ V_{bg} \rightarrow V_t \rightarrow$ more carriers $\rightarrow$ noise

Sid is maximum @ $V_{ds} = 0$ V, starts to decrease as operating point move towards saturation (charge decreases)

- $+ V_{bg} \rightarrow V_t \rightarrow$ more carriers $\rightarrow$ noise
- $+ V_{bg} \rightarrow V_t \rightarrow$ more carriers $\rightarrow$ noise

---

Flicker noise – FDSOI MOSFET Models

FDSOI transistor faces more carrier fluctuations due to the presence of the front and back interfaces (carrier trapping and de-trapping)

- Single Si-Sio2 interface
- Scaling issues

- Dual Si-Sio₂ interface
- Good Scaling solution

Flicker noise — BSIM-IMG Model

The charge fluctuations near both interfaces contribute to total inversion charge fluctuation ($dQ_{inv}$) in thin silicon film as

$$dQ_{inv} = \frac{\partial Q_{inv}}{\partial N_{t1}'} dN_{t1}' + \frac{\partial Q_{inv}}{\partial N_{t2}'} dN_{t2}'$$

Front Interface  Back Interface

$$dQ_{inv}$$ (1)

Fluctuation in the amount of trapped oxide charges at front/back interfaces will cause

- Correlated fluctuation in effective mobility
- Correlated fluctuation in carrier number

ultimately fluctuates the current

$$\frac{dI_{ds}}{I_{ds}} = dN_{t1}'\left(\frac{1}{N_{t1}'} \frac{\partial N'}{\partial N_{t1}'} + \frac{1}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial N_{t1}'}\right) + dN_{t2}'\left(\frac{1}{N_{t2}'} \frac{\partial N'}{\partial N_{t2}'} + \frac{1}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial N_{t2}'}\right)$$

$$R_{front} = \frac{\partial \Delta N}{\partial \Delta N_{t1}} = \frac{\partial Q_{inv norm}}{\partial V_{fg}} = C_{ox1} \left(\frac{\partial V_{fg,eff}}{\partial V_{bg}} - \frac{\partial \Psi_{s1}}{\partial V_{bg}}\right) + \frac{C_{si} \cdot C_{ox2}}{C_{si} + C_{ox2}} \left(1 - \frac{\partial \Psi_{s1}}{\partial V_{bg}}\right)$$

$$R_{back} = \frac{\partial \Delta N}{\partial \Delta N_{t2}} = \frac{\partial Q_{inv norm}}{\partial V_{bg}}$$

$$R_{front} = \frac{N}{C_{box} N + N_1^*}; N_1^* = \frac{KT}{q^2} (C_{ox} + C_{it})$$
Flicker noise – BSIM-IMG Model

From the number fluctuation theory and following assumptions
- Oxide trap have a uniform distribution near the interface
- Tunneling probability decreases exponentially in vertical direction

\[
S_{\Delta Ids}(x, f) = \left( \frac{I_{ds}}{W \cdot \Delta x} \right)^2 \left( \frac{R_{front}}{N} \pm \alpha_1 \mu_{eff} \right)^2 S_{\Delta N_{t1}}(x, f)
\]

\[
+ \left( \frac{I_{ds}}{W \cdot \Delta x} \right)^2 \left( \frac{R_{back}}{N} \pm \alpha_2 \mu_{eff} \right)^2 S_{\Delta N_{t2}}(x, f)
\]

\[
S_{\Delta N_{t1/2}}(x, f) = N_{t1/2}(x, f) \left( \frac{kT \cdot W \cdot \Delta x}{\gamma \cdot f} \right)
\]

\[
S_{Ids}(f) = \frac{1}{L^2} \int_0^L S_{\Delta Ids}(x, f) \cdot \Delta x \cdot dx
\]

\[
= \frac{kT \cdot q \cdot I_{ds} \cdot \mu_{eff}}{\gamma \cdot f \cdot L^2} \int_0^{V_{ds}} \left[ N_{t1}^*(E_{fn}) \frac{R_{front}^2}{N} + N_{t2}^*(E_{fn}) \frac{R_{back}^2}{N} \right] dV
\]

\[
N_{t1/2}^*(E_{fn}) = \text{Trap distribution around quasi Fermi level – Delta function}
\]
The threshold voltage shift due to different back gate biases is captured very well.

Model is following CNF model in weak inversion region.

Model is following CMF model in strong inversion region.

Model shows correct trends (1/f-like spectra) for all drain biases which implies model’s robustness from linear to saturation region.

Negligible effect of back-bias (CNF)

Mobility fluctuates with back-bias (CMF)
Gate induced noise – BSIM-IMG Model

Channel charge fluctuation cause a redistribution of the channel potential which results in a charge redistribution across the gate capacitor. This fluctuation is capacitively coupled to the gate charge at the RF frequency, and result in a noise current (rate of change of charge) at the gate terminal.

**KP equation**

\[
S_{ig}^2 = P_{S_{ig}} \int_{V_s}^{V_d} g_0(v) \left[ \int_{V_s}^{V_d} (Q(u) - Q(v))g_0(u)du \right]^2 dv
\]

\[
S_{ig, id} = P_{S_{ig, id}} \int_{V_s}^{V_d} g_0(v) \int_{V_s}^{V_d} g_0(u)(Q(u) - Q(v))dudv
\]

\[
PS_{ig}^2 = \frac{16\pi^2 kT f^2 W^2}{I_{ds}^5 L_{eff}^2} \quad \quad PS_{ig, id} = \frac{-j8\pi kT f W}{I_{ds}^3 L_{eff}^2}
\]

\[
Q = C_{ox1} V_t (q_f + Kq_b)
\]

\[
Q_f(b)_N = \frac{q_f^N}{N} - q_f^N + q_f^{N-1} - q_f^{N-1}
\]

Gate induced noise – BSIM-IMG Model

- Increase in semiconductor charge with increasing front gate voltage results in more scattering due to increase in the field and hence more noise.
- Increasing the back gate bias also leads to an increase in the total semiconductor charge, resulting in higher noise for higher back gate bias.

\[ S_{ig}^2 = \frac{16\pi^2 q_f^6 L_{\text{sat}}^3}{WC_{ox}^3 V_i^9 m_{id}^5} (T_I - U_I + X_I); \]
\[ S_{ig, id} = \frac{-j8\pi q_f L_{\text{sat}}}{C_{ox} V_i^3 m_{id}^3} \left( \frac{2T_I - U_I}{2P_I} \right) \]
\[ T_I = P_I^2 \left( \mu_f^2 Q_f3 + 2\mu_f \mu_b q_{av} Q_f2 + \mu_b^2 Q_b3 \right); \]
\[ P_I = WC_{ox} V_i^3 \left[ \mu_f Q_f3 + \mu_b Q_b3 + K q_{av} (\mu_f + \mu_b) Q_f2 \right] \]
\[ U_I = 2P_I WC_{ox} V_i^3 (\mu_f Q_f2 + \mu_b K Q_{b2}) \left[ \mu_f^2 Q_f4 + (\mu_f q_{av} Q_f3)(\mu_f K + 2\mu_b) + (\mu_b q_{av}^2 Q_f2)(2\mu_f K + \mu_b) + \mu_b^2 K q_{av}^3 Q_f1 + \eta_f \left( \log(q_{fa}) - \log(q_{fd}) \right) \right] \]
\[ X_I = \left[ WC_{ox} V_i^3 (\mu_f Q_f2 + \mu_b K Q_{b2}) \right]^2 \left[ \mu_f^2 Q_f5 + 2q_{av} \mu_f Q_f4 (\mu_b + \mu_f K) \right. \]
\[ + q_{av}^2 Q_f3 (\mu_b^2 + 4\mu_f K \mu_b + K^2 \mu_f^2) + 2\mu_f \mu_b K^2 q_{av} Q_f2 (1 + q_{av}) \right] \]
As the frequency increases, the impedance of the effective capacitance coupling between the gate and the channel brings in a frequency dependence.

- Increase in cross-correlation PSD at higher frequency due to capacitive coupling.
In cellular and Wi-Fi systems, the Radio Frequency (RF) Front-End Module is one of the most critical parts.

High performance system on chip (SOC), which includes mix signal, complex high power devices, trans-receiver, high resistivity (HR) silicon SOI substrates (RFSOI substrate) make it possible.
In MOS devices the effect of parasitic resistances and capacitances showed up at higher frequency.

When MOSFET is operated in gigahertz range, the extrinsic part of the transistor is of more concern than its intrinsic part.

The accurate modeling of the following are highly important.
1: Gate electrode resistance.
2: Source/Drain series resistance.
3: Parasitic capacitance.
4: Substrate resistance.
RF Modeling of FDSOI MOSFETs

Parameter extraction for DC characteristics

S-parameter measurement

Coaxial cable

Agilent E5071C ENA Network Analyzer

Probe Station

Gate capacitance

\[ C_{GS} (\text{pF}) = \text{Im}(\text{y}_{11}) \]

- N-channel
- \( V_{ds} = 0 \text{ V} \)
- \( V_{bg} = 0 \text{ V} \)

\[ C_{GS} \text{ (pF)} \]

- 0.84
- 0.91
- 0.98
- 1.05

\[ V_{fb} \text{ (V)} \]

- 0.0
- 0.2
- 0.4
- 0.6
- 0.8
- 1.0
- 1.2
- 1.4

Iso-thermal frequency

Output conductance (gds)

\[ \text{Real (y}_{22}, \text{ mS) } \]

- 2.4
- 2.6
- 2.8
- 3.0
- 3.2
- 3.4

\[ \Delta G_{SHE} \]

Substrate N/W:

Heat N/W:

DC value of g_{DS}

Gate resistance

\[ \text{Real (h}_{11}, \text{ Hz}^3) \]

- 0
- 3
- 6
- 9
- 12
- 15

\[ f \text{ (Hz)} \]

- 10^6
- 10^7
- 10^8
- 10^9
- 10^10

Symbols: Exp. Data

Lines: Model

Self-heating model

MOS-AK, Chengdu


UC Berkeley-24
Recently published BOOK on BSIM-IMG
- Core Modeling
- I-V & C-V Modeling
- Leakage Current Modeling
- RF and Noise Models in BSIM-IMG
Summary

- Core I-V and C-V models for independent multi-gate FETs are developed and verified with TCAD without using fitting parameters.
- BSIM-like short channel real device effects are implemented.
- Double hump $g_m$ behavior analysed and modelled.
- RF and Noise models in BSIM-IMG are developed.
THANK YOU!