AI Applications in Semiconductor
From Parametric Testing to Design Signoff

http://www.platform-da.com
11 years of support of MOS-AK

32nm

Stress Modeling (LDE)

Physics Driven

7nm/5nm

AI is hot

Algorithm Driven
AI vs. DA

Recent hot AI terms

- CNN
- RNN
- GAN
- DNN

Many Machine Learning terms...

- FFT
- PCA
- OLS
- Spline
- Bayesian...
- Genetic Algorithms
- Machine Learning
- NN

What used often in EDA

- Signal and Systems
- Stochastic process
- Numerical Analysis

DATE 2018 Best Paper on Speeding up Test with Learning Algorithms

TNS2012 paper on Soft Error Using ANN

AI and DA are related
What’s AI Application and Why do we need it?

- **Prediction** through different modeling approaches (RSM, NN, etc.), and discover the “real world”
  - Use less efforts to achieve similar accuracy and performance
  - Break Hardware boundries
- **Regression**: effectively construct the network between parameters and targets and reduce the labor of tweaking parameters to achieve targets

**Ultimate Goal**: Better Pay, Less Working Hours

TNS2012 paper on Soft Error Using ANN

DATE 2018 Best Paper on Speeding up Test with Learning Algorithms
AI Application: Consumer vs. Semiconductor
- Problem Scope, Algorithm, Expertise, Data
- Key FOM

AI Driven Modeling Eco-system
- Test – Faster and More Powerful Test
- Modeling – Automatic Extraction
- Design – tough mission requires long term efforts

Challenges down the road
- Challenges
- Applications

Conclusion

Concept & Key FOM

Daily Exercise in Semiconductor

Faster, Safer and More Powerful
Scope Matters

- **Narrow Scope**
- **Optimize Based on knowhow**

Narrowed scope, Less contamination, Higher accuracy requirement

A lot work repeatably done daily in Semiconductor have contained Scope
Rely on Expertise

- **Siri** gives definitive answers
- Poor accuracy leads to **low usage**
- **Search Engine** gives multiple answers
- Reply on expertise to filter, we use it **everyday**

If targets are difficult to define, give multiple answers
In engineering world, most of us are dealing with low data problems.

- Physics provides a shortcut.
- High quality data availability.

Low Data not necessarily a bad thing as long as it gives you enough information to extract features.

- PCA – more data doesn’t give you more value.

Consumer applications require big data, which are owned by the tech giants:

- Apple
- Google
- Amazon
- Facebook

Most semiconductor companies owe quality data.
Revisit Key FOM - DARK

Algorithms → We are optimization experts, daily exercises with different neural networks

Knowledge → Modeling background give us the best knowledge in device/IC behaviors

Data → Accumulated millions of curves from different foundry/process

Risk → We expect error in simulation or measurement

AI Has Potentials in Semi
**AI Application** : Consumer vs. Semiconductor

- Problem Scope, Algorithm, Expertise, Data
- Key FOM

**AI Driven Modeling Eco-system**

- Test – Faster and More Powerful Test
- Modeling – Automatic Extraction
- Design – tough mission requires long term efforts

**Challenges down the road**

- Challenges
- Applications

**Conclusion**
Why Device/IC Test Is a Good Machine Learning Application?

- **Time is $$$: Increasing Pain**
  - Volumes: Increasing wafer volumes, increasing variability, but reducing test time = Faster TTM
  - Emerging Technologies: Micro-LED, VCSEL, Optical Module reducing testing time = saving $

- **IC/Device Test: Confined Scope**
  - Self-driving cars are difficult with current algorithms/computing, but trains are easy
  - IC/Device behaviors are highly regulated, often by well-know physics, similar to “trains”, with very contained scopes

- **PDA's DARK**
  - Data: Owned a lot of data from many foundries
  - Algorithms: Optimization gurus, applied machine learning in EDA for years
  - Risk: Testing facility itself brings in error, as long as ML error < system errors, applying ML can also reduce these instabilities
  - Knowledge: Modeling/Simulation Folks own the best behavior knowledge
Learning Based Test Methodologies

Accelerating Hardware

Testing Behavior Prediction Algorithm
Use Time Series Analysis to reduce settling time of the hardware

Information Redundancy Removal Algorithm with Machine Learning

◆ Best Paper at DATE 2018

Process Variation Awareness Algorithm
Apply Deep Learning to extract data structure and pattern for some dies to know the behavior of other dies for smarter testing
Outcomes of Smart Test

**Much Faster**

Parametric Test system can achieve 10-100X acceleration compared to traditional IC/device while retaining same accuracy.

**Safer & Reliable**

Testing noise and testing structure drawbacks can be internally considered and removed by learning techniques.

**Powerful & Smarter**

With 5G and MMW, current hardware based testing will soon hit a wall, “AI-driven” is the only way to break the hardware boundary.

Revolutionary in test industry: Shift from labor & capital-intensive to knowledge & technology-intensive. Align with the strategic direction of “Made in China 2025”.
Test Methodologies

- Traditional Instruments are “Analog” heavy
- “Digital” heavy, apply similar methodologies from computer vision to extract features and recover data
  - Signal can be noisy
  - On board data processing and signal processing
- Like ASIC, test instruments are made to meet specific requirements
Binning Is More AI Friendly (Less Parameters)
- BSIM4 has around 200 parameters, Binning can reduce to 10-20 parameters
- TID Model Can Be Fully Automated (<10 Parameters, 1 or 2 targets)

Human Experts: 3 days, Local x86(i7)+expert: 1-day Pure Cloud: 10 days, ~¥30K

The Biggest Challenge is how to define targets
Case Study: Bi-Direction Network for Modeling

➢ Similar methods deployed

[Image of diagram showing network architecture with steps: Load pretrained network, Replace final layers, Train network, Predict and assess network accuracy, Deploy results.]

All BSIM4 Params
Skewed Params

$x = [x_1, x_2, ...]$
- 3 4 3
- 4 5 1
- 5 3 0
- 3 8 3
- 9 7 8

$y = f(x; w)$
- 10
- 10
- 8
- 14
- 24

Circuit Design

- Front end design automation: possible
- Physical layout: very difficult

Whole System

Verilog-A

Pareto Front Modeling

Circuits

- Blocks (e.g., LNA)
- Analog Frontend
- Whole System

Circuit Specs
RO delays in consideration of LPE

IV/CV Specs

Model/Process Params

Construct Correlations of System, Circuit, Device and Process
Challenges Down The Road

◆ Measurement Expensive
  ◆ New technologies such as Micro-LED
  ◆ 5G

◆ Simulation Costly
  ◆ Memory and Logic ICs are already simulation costly
  ◆ More corners
AI-Driven Parametric Test Applications I

- AI Application: IV and 1/f Noise Combined Test
  - WAT level flicker noise test is in increasing need
  - Proven by leading semiconductor companies and top tier research

**Nature Nano and EDL Papers**

The only solution for production level 1/f Noise Test

**IV,CV,1/f Noise All-in-One**
Only 8.2 Kg

**Modular Architect Flexible**
High speed, high density, accurate capacitance tester

UPH = 40,000 devices (32 channel system)

0.1pF accuracy

Modular

Up to 64 channels
Conclusion

- AI in Semi is not just AI Chips, AI applications have a lot of potential.
- Design and Manufacture should invest more on Algorithms
- AI is the answer for future challenges in Test and Simulation
PDA At A Glance

◆ PDA: Unique Integration of All the Critical Elements that connect Process Technology with Product Design

EDA  Test  EDU

Engineering Center

Scale by designs  Scale by wafers  Scale by people

Embrace Data

Faster Test and Faster Simulation

Technology Driven, Innovation is our Key Competence
MQRF – Complete CMOS RF Modeling Platform

MQ-RF – Integrate BB modeling, QA and RF to a single platform

- Unique integration of the whole RF Flow
  - DC, AC, LDE, Statistical, 1/f noise, RF and Thermal noise

- Comprehensive Model Support
  - BSIM3, BSIM4, BSIM6, BSIM-CMG, BSIMSOI, PSP
  - RF Model Extraction Technology up to 110GHz
  - Internal QA
  - Built-in RF data QA, de-embedding, extraction and model QA
High precision IV, and 1/f noise test in one box w/o cabling change (e.g. 5X CP than competition)

1/f noise Production test ready (down to 2s/bias)
Support WAT 1/f noise test

Built-in MeQLab to form a complete modeling system

10fF CV Accuracy
0.1fA sensitivity

200V, 3A
5X Faster

Compact 8.2Kg

As many channels as desired

1/f noise integrated (all channels)