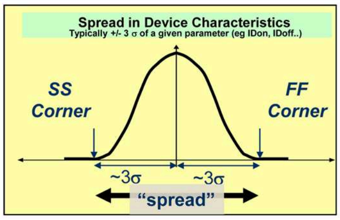
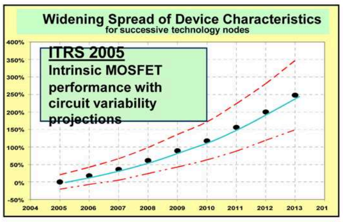
PQA Variable-Aware Verification Platform for the sub-45nm PDK

Layout Effect Variability at Sub 45nm

- Spread in Device Characteristics
  - Typically encompassing +/- 3 σ of a distribution of key parameters
  - Extreme points define FF & SS Corners
- Widening Spread for Successive Nodes
- Caused from Litho and Stress Effects
  - Rounding
  - Gate spacing/Contact positioning
  - Well Proximity

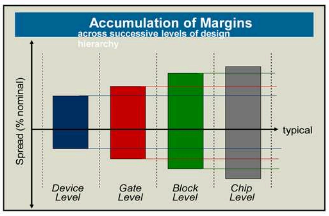




Leads to overly pessimistic design??

Traditional Methodology – Excessive Margins

- Accumulate Margins for Successive Levels of Design Hierarchy
- Standard Corner-based Analysis
- Margin Definition is a Trade Off
  - Widening Spread in Device Corners propagates to excess margin at MSM and System level



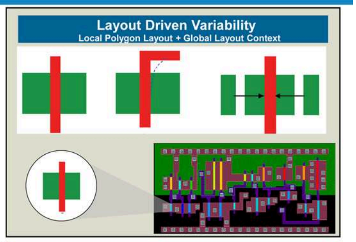
Gate Density is compromised

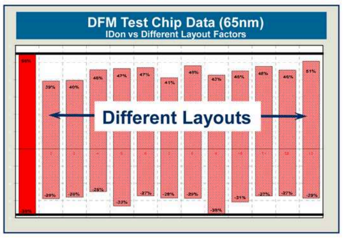
PQA Variability-Aware PDK Analysis

- Automates the SPICE analysis of Layout Effect Variability
- Easy assessment of variability impact from different sources
  - Foundry DFM Models
- Accurately predict design margin due to process/design variability before tape-out.
  - Remove "uncertainty" before tape-out
- Increase gate density, performance

Foundry Solution – Model-based DFM

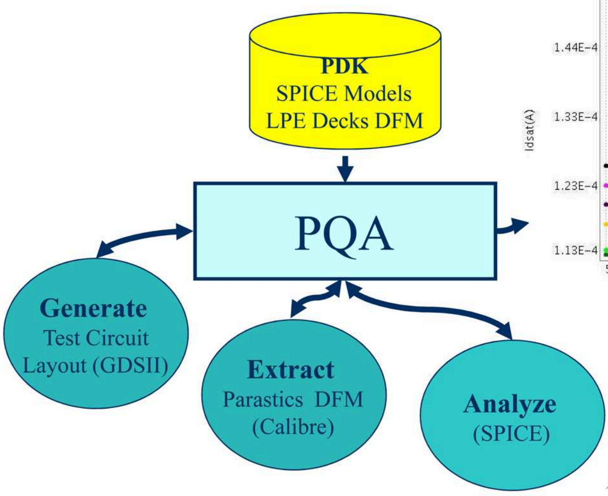
- Layout effect variability can be mitigated through analysis
- Incorporate litho/stress effects into compact model/LPE decks
- E.g. TSMC DDK @ 32nm
  - Litho pattern check
  - CMP analysis
  - Critical area analysis
  - DFM optimization results
- Analyze layouts with SPICE
- But how:
  - Do the models make sense?
  - Can the designer assess impact of variability?

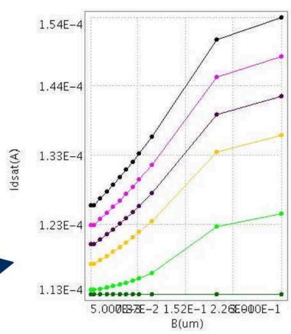




Requires new automated solutions

PQA





Results:

Characterize
Compare
Document

Accelicon