

ASYMMETRICAL DOUBLE GATE (ADG) MOSFETs COMPACT MODELING

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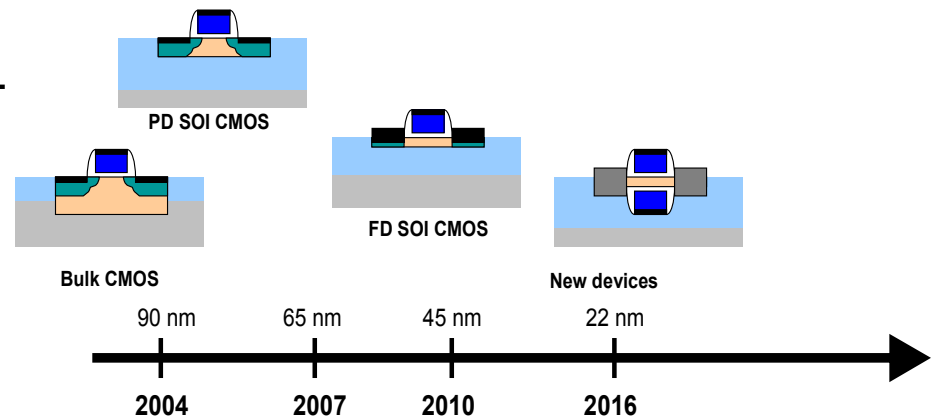
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WHY ARE WE INTERESTED IN MODELING ADG MOSFETs?

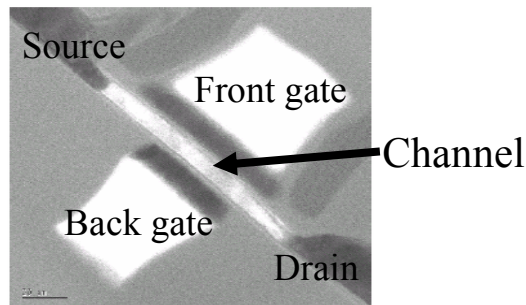
- New Devices
 - classical CMOS technologies + forecasts of the ROADMAP = ??
 - New devices: GAA, FinFET, SON & planar DG



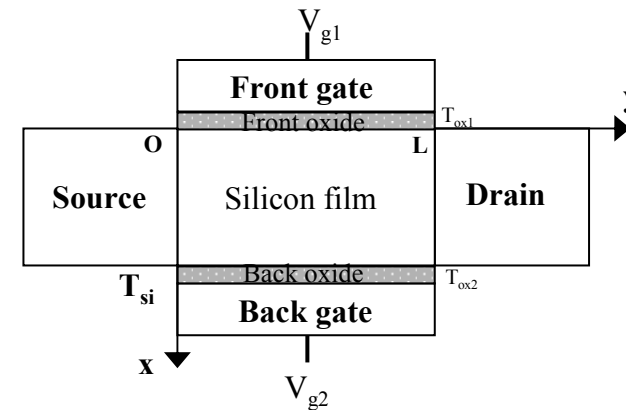
- ADG MOSFET
 - Excellent channel control
 - Design flexibility with a second gate independently driven
- Model: to take advantage of this new device designers need a model
- Compact Model: to design new circuits

ADG ARCHITECTURE

DIFFERENCES BETWEEN SYMMETRICAL (SDG) AND ASYMMETRICAL (ADG) DG MOSFETs



PICTURE: ADG MOSFET
M.Vinet et al, SSDM 2004
22nm node



SCHEMATIC: DG MOSFET

The asymmetry of the structure:

- gate oxide thicknesses
- gate voltages
- or/and gate work functions

MODELING DIFFICULTIES

BASIC EQUATIONS OF ADG

DRAIN CURRENT

$$I_{ds} = \mu \frac{W}{L} \int_{V_s}^{V_d} Q_{inv} d\phi_{imref}$$

GAUSS THEOREM

$$Q_{inv} = \epsilon_{si} (E_{s1} - E_{s2})$$

BOUNDARY CONDITIONS

$$E_{s1} = \frac{C_{ox}}{\epsilon_{si}} (V_{g1} - \psi_{s1})$$

$$E_{s2} = - \frac{C_{ox}}{\epsilon_{si}} (V_{g2} - \psi_{s2})$$

POISSON EQUATION & ITS FIRTS INTEGRATION

$$\frac{d^2 \psi}{dx^2} = \frac{q \cdot n}{\epsilon_{si}}$$

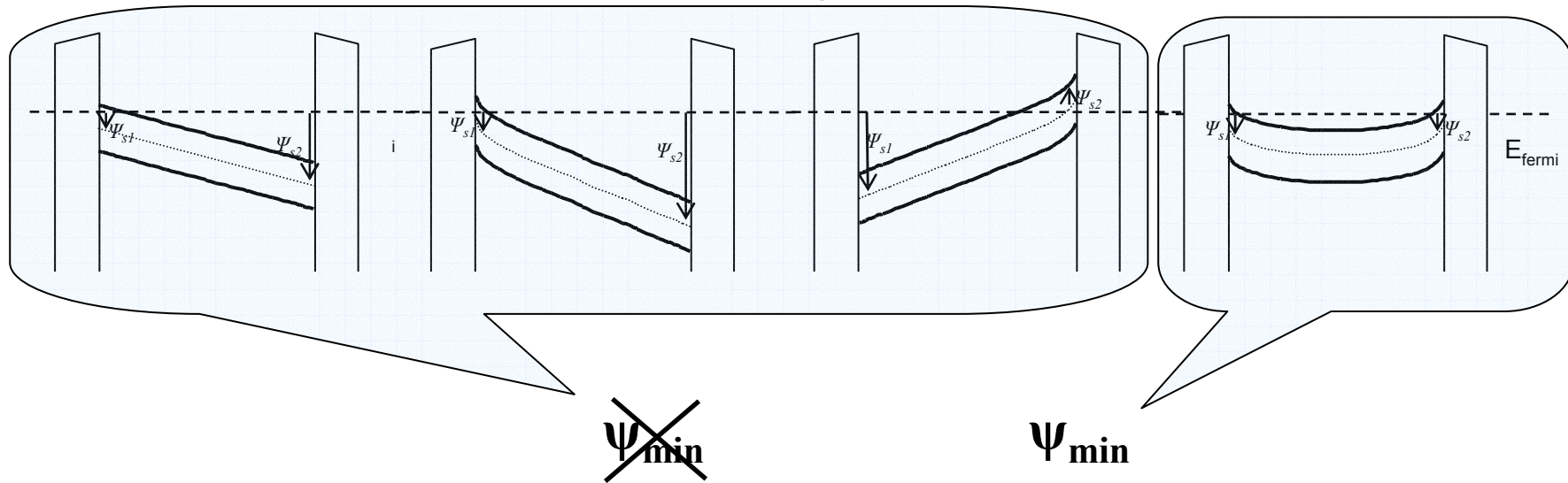
$$E_{s1}^2 - E_{s2}^2 = \frac{2 \cdot q \cdot u_t \cdot n_i}{\epsilon_{si}} \left[\exp \left(\frac{\psi_{s1} - \phi_{imref}}{u_t} \right) - \exp \left(\frac{\psi_{s2} - \phi_{imref}}{u_t} \right) \right]$$

➔ to calculate physical I_{ds} , unknowns are ψ_{s1} and ψ_{s2}

MATHEMATICAL DIFFICULTIES

ASYMMETRY \Rightarrow Not always a minimum of potential in the silicon film: 2 CASES

Band diagrams



FIRST DIFFICULTY

\Rightarrow DEFINE 2 CASES AND THEN UNIFY THEM

MODELING DIFFICULTIES

MATHEMATICAL DIFFICULTIES

SECOND DIFFICULTY

NO EXACT SOLUTIONS OF ψ_{s1} AND ψ_{s2}

2 OPTIONS

FLOATING NODE RESOLUTION

4 unknown parameters,

$\psi_{s1Source}$, $\psi_{s1Drain}$ & $\psi_{s2Source}$, $\psi_{s2Drain}$

MAKE PHYSICAL ASSUMPTIONS

→ Simplifications of Poisson equation

DIFFERENT WAYS OF MODELING

▪ 1st OPTION: IMPLICIT ANALYTICAL RESOLUTION

Use of floating nodes or iterative resolutions to solve Poisson's equation.

▪ 2nd OPTION: EXPLICIT ANALYTICAL RESOLUTION

Poisson's equation is solved with **physical approximations** → allow to get **explicit** formulations of electrical parameters → **fully** analytical model.

- Charge-based model
- V_{th} -based model

- **MAIN ACTORS: 3 teams**

- Y. Taur (USA, University of California): mainly for SDG MOSFET
- M. Chan (Hong Kong University of Science & Technology): ADG MOSFET
- T. Nakagawa (Japan, AIST): ADG MOSFET

- Y. Taur, “Analytical Solutions of Charge and Capacitance in Symmetric and Asymmetric DG MOSFET”, IEEE Trans. Electron Devices, vol.48, n°12, Dec. 2001.

- M. Chan, “Quasi-2D Compact Modeling for DG MOSFET”, NSTI Nanotech, vol.2, pp.108-113, 2004.

- Nakagawa et al., “Improved Compact Modeling for Four-Terminal DG MOSFETs”, NSTI Nanotech, 2004.

WHY ?

COMPLEXITY of basic equations

MANY ADVANTAGES

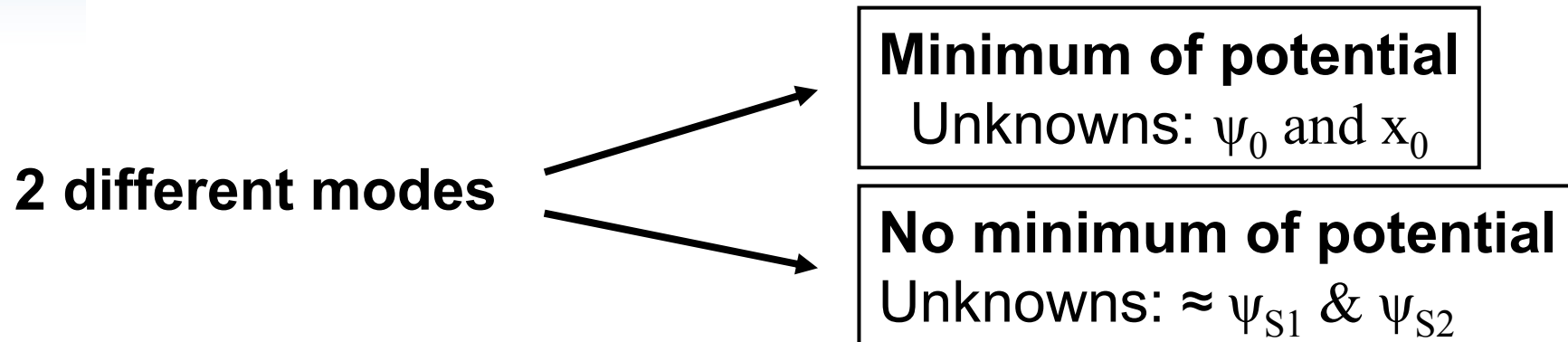
No problem to **unify** the different operating modes

ACCURACY because it keeps all basic equations without any (or with few) simplification

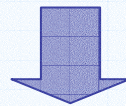
PREDICTIVITY because basic equations could be solved for **all materials** and **geometrical parameters**

IMPLICIT ANALYTICAL MODELING

PRINCIPLE OF FLOATING NODE SOLUTION (Taur model)



2 UNKNOWNNS + SOURCE & DRAIN SIDE



4 FLOATING NODES for each case

**Each mode should be NUMERICALLY solved
thanks to BOUNDARY CONDITIONS.**

IMPLICIT ANALYTICAL MODELING

PRINCIPLE OF FLOATING NODE SOLUTION (Taur model)

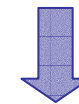
DRAIN CURRENT I_{ds}

$$I_{ds} = \mu \frac{W}{L} \int_{V_s}^{V_d} Q_{inv} d\phi_{imref}$$

NUMERICALLY

$$I_{ds} = \alpha \cdot \left[Q_{inv} - \frac{Q_{inv}^2}{2} \right]_{V_s}^{V_d}$$

ANALYTICALLY (EKV METHOD)



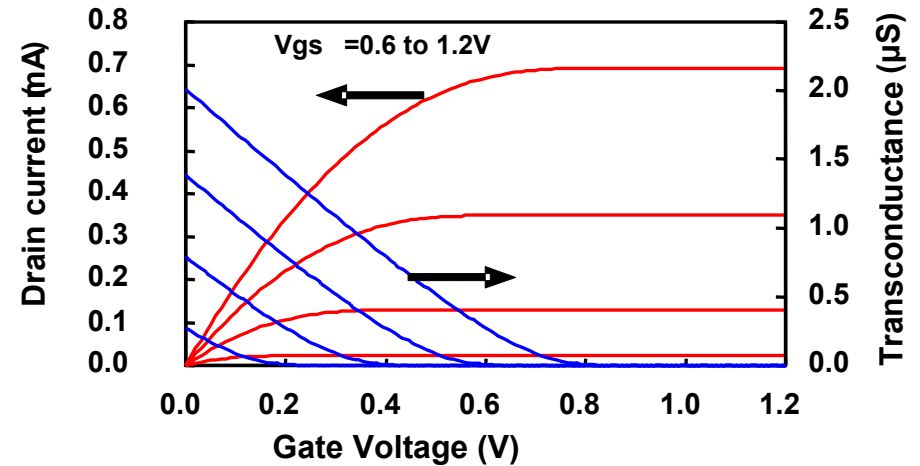
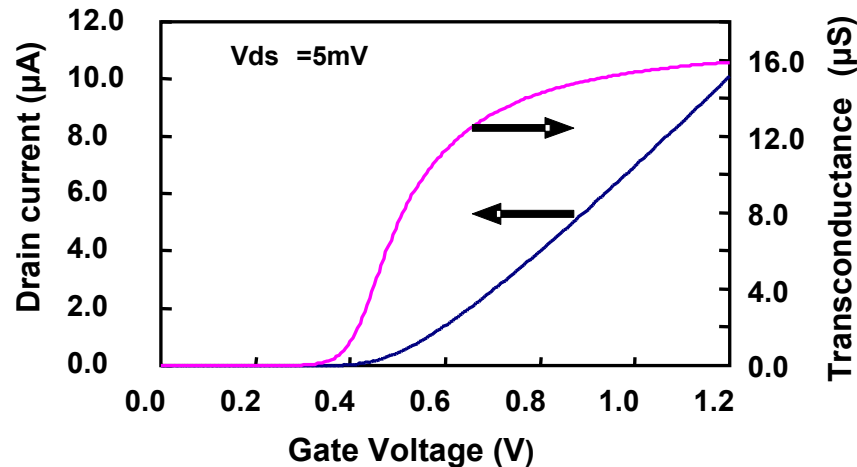
**Not really true for ADG because
of interface coupling:
need a unification**

IMPLICIT ANALYTICAL MODELING

PRINCIPLE OF FLOATING NODE SOLUTION (Taur model)

Symmetrical case: VerilogA + Eldo simulator

SDG : $L=0.5\mu\text{m}$, $W=1.0\mu\text{m}$, $T_{\text{si}}=10.0\text{nm}$, $T_{\text{ox}}=1.2\text{nm}$



Asymmetrical case: VerilogA + Eldo simulator

Currently: convergence problem

- **LIMITS:**
 - Convergence problems because of the **4 floating nodes**.
 - Simulation time.

- For that, we choose to develop an **explicit** analytical model with only 1 floating node: T°

- **MAIN ACTORS: 2 teams**
 - J. G. FOSSUM (USA, University of Florida)
 - G. Pei (USA, Cornell University)

- **TWO KINDS OF EXPLICIT ANALYTICAL MODEL**
 - Charge-based model
 - V_{th} model

- J. G. Fossum et al., “UFDG and Nanoscale FinFET CMOS Design and Performance Projections”, IEEE ICICT, 2005.
- A.V. Kammula et al., “ A long Channel Model for the Asymmetric DG MOSFET Valid in All Regions of Operation”, IEEE Southwest Symposium Mixed-Signal Design, pp.156-161, 2003.
- G. Pei, “A Physical Compact Model of DG MOSFET for Mixed-Signal Circuit Applications – Part1: Model Description”, IEEE Transac. On Electron Devices, vol.50, n°10, Oct. 2003.

ADVANTAGES OF AN EXPLICIT ANALYTICAL MODEL

- Better physical understanding
- Easier to use for circuit design because of speed and convergence whatever the number of transistors

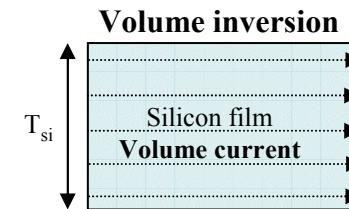
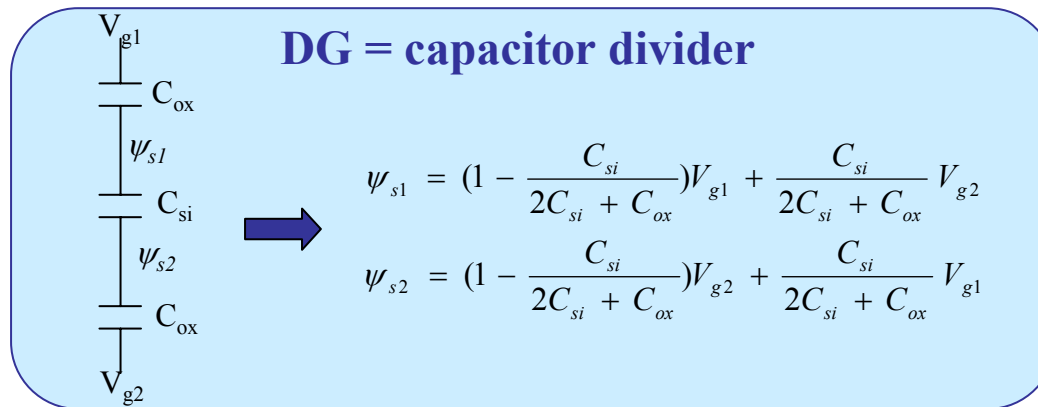
DISADVANTAGES OF AN EXPLICIT ANALYTICAL MODEL

- Less accurate in moderate inversion
- Difficulties to get well derivatives

EXPLICIT ANALYTICAL MODELING

CHARGE-BASED MODEL

- Weak inversion for both interfaces

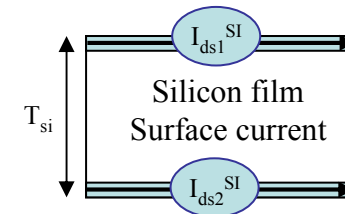


- Strong inversion for both interfaces

Both channels are independent



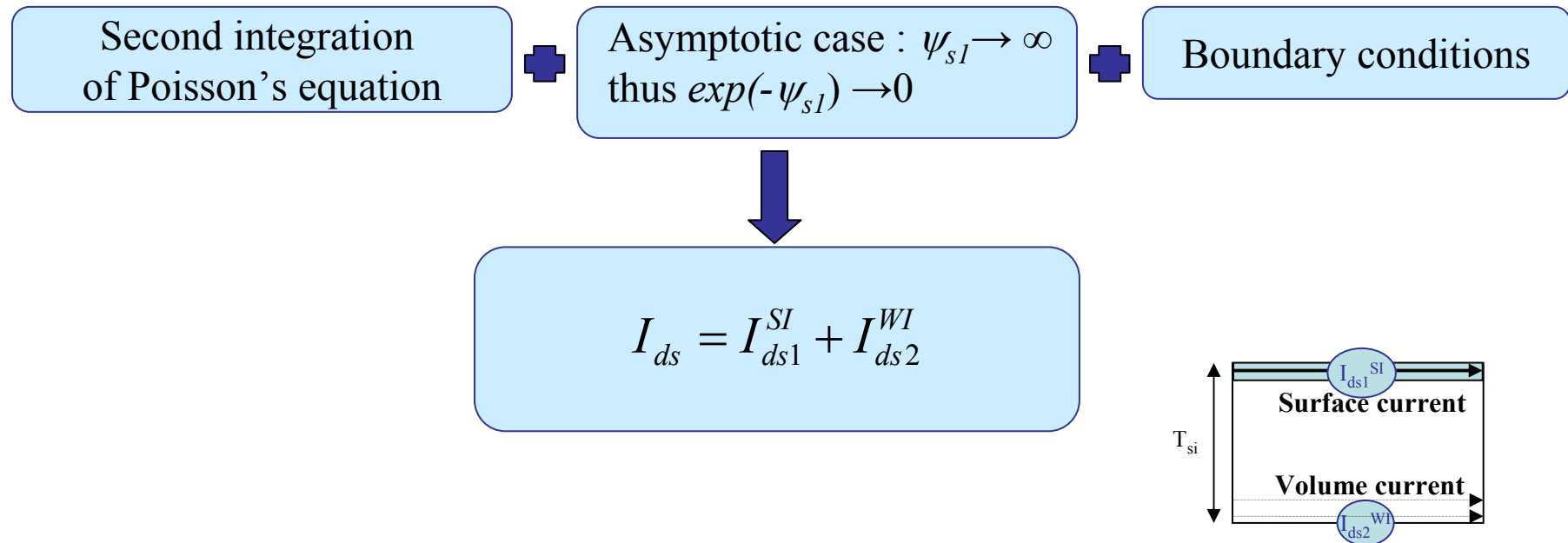
$$I_{ds}^{SI} = I_{ds1}^{SI} + I_{ds2}^{SI}$$



EXPLICIT ANALYTICAL MODELING

CHARGE-BASED MODEL

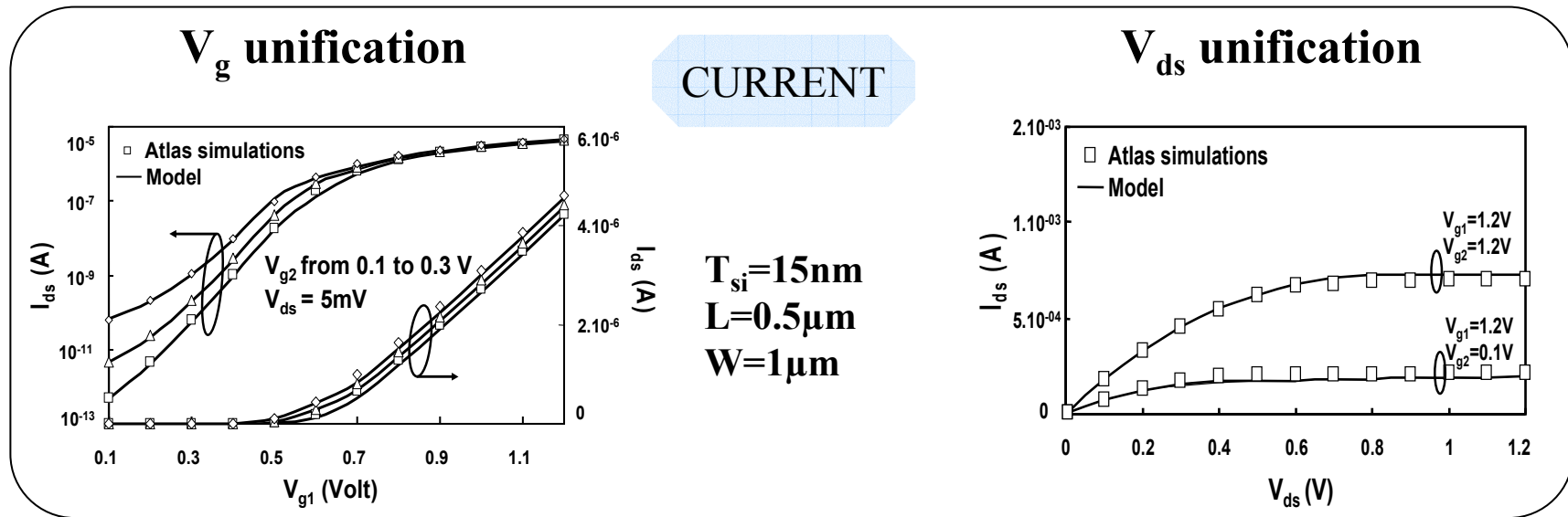
One interface is in strong inversion and the other one in weak inversion.



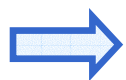
EXPLICIT ANALYTICAL MODELING

CHARGE-BASED MODEL

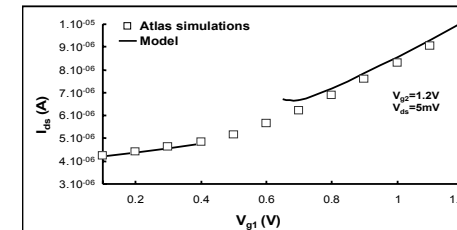
LIMITS: unification between different operating modes



- Unification problem when V_{g2} is high.
- Problems to have a continuous transconductance



V_{th} -based model is developing: charge and current model take into account interface coupling



V_{th} -BASED MODEL

- **ASSUMPTION:** no current flows from a channel to the other one (checked by TCAD simulations)

- **PRINCIPLE:** 1 DGMOS = 2 SGMOS in parallel

$$\rightarrow Q_{inv} = Q_{inv1} + Q_{inv2}$$

$$\rightarrow I_{ds} = I_{ds1} + I_{ds2}$$

+ INTERFACE COUPLING DESCRIPTION

+ CORRECTION FACTOR DEFINITION to

well describe strong inversion

UNIFICATION OF THE DIFFERENT
OPERATING MODES

V_{th} -BASED MODEL

FRONT & BACK V_{th}

$$V_{th1}' = V_{th10} - (n_1 - 1)V_{g2}' - n_1 U_t \cdot \ln \left(\frac{\tanh \left[\frac{C_{eq}}{C_{Si}} \frac{V_{g2}' - V_{g1}'}{2U_t} \right]}{\frac{C_{eq}}{C_{Si}} \frac{V_{g2}' - V_{g1}'}{2U_t}} \right)$$

$$V_{th2}' = V_{th20} - (n_2 - 1)V_{g1}' - n_2 U_t \cdot \ln \left(\frac{\tanh \left[\frac{C_{eq}}{C_{Si}} \frac{V_{g2}' - V_{g1}'}{2U_t} \right]}{\frac{C_{eq}}{C_{Si}} \frac{V_{g2}' - V_{g1}'}{2U_t}} \right)$$

V_{th} -BASED MODEL

INTERFACE COUPLING DESCRIPTION

Example: front interface in weak inversion

n_1 represents
interface coupling

$$n_1 = 1 + \frac{C_{si} \cdot C_{ox2}}{C_{ox1} (C_{si} + C_{ox2})}$$

$$Q_{inv1WI}(x) = -q \cdot n_i \cdot u_t \cdot \exp\left(\frac{V_{g1} - V_{th1} - n_1 \cdot \phi_{imref}}{n_1 \cdot u_t}\right)$$

CORRECTION FACTOR TO WELL DESCRIBE STRONG INVERSION

$$Q_{invSI}(x) = -\mu \frac{W}{L} C_{oxi} \cdot (V_{gi}' - V_{thi}' - n_i \cdot \phi_{imref}(x)) \cdot (1 - \varepsilon_i(x))$$

ε_i represents the dependance
of the interface strong inverted
versus its gate voltage

EXPLICIT ANALYTICAL MODELING

V_{th} -BASED MODEL

UNIFICATION OF THE DIFFERENT OPERATING MODES

$$V_{off} = \epsilon_1 (V_g - V_{th})$$

V_g unification

$$V_{gt1} = 2u_t n_1 \ln \left[1 + \frac{\exp\left(\frac{V_{g1} - V_{th1} - V_{off1}}{2u_t n_1}\right)}{1 + 2 \exp\left(-\frac{V_{g1} - V_{th1}}{2u_t n_1}\right)} \right]$$

Weak inversion

$$V_{gt1} = u_t n_1 \exp\left(\frac{V_{g1} - V_{th1} - \frac{V_{off1}}{2}}{u_t n_1}\right)$$

Strong inversion

$$V_{gt1} = V_{g1} - V_{th1} - V_{off1}$$

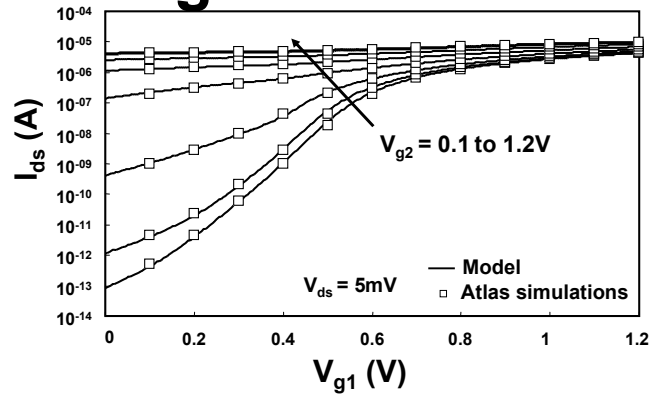
V_{ds} unification

$$V_{dsieff} = V_{dsati} - \frac{1}{2} \left[V_{dsati} - V_{ds} - \delta + \sqrt{(V_{dsati} - V_{ds} - \delta)^2 + 4\delta V_{dsati}} \right]$$

EXPLICIT ANALYTICAL MODELING

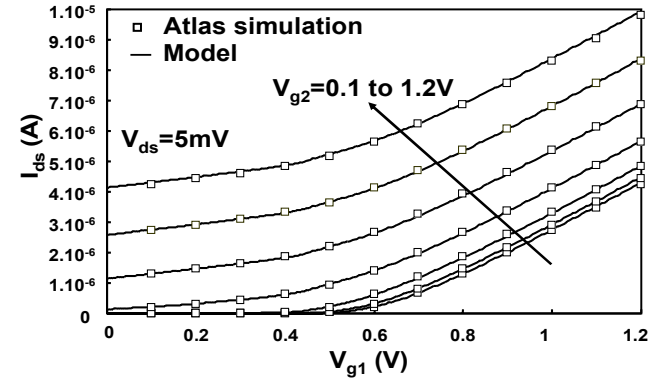
V_{th} -BASED MODEL

Logarithmic scale



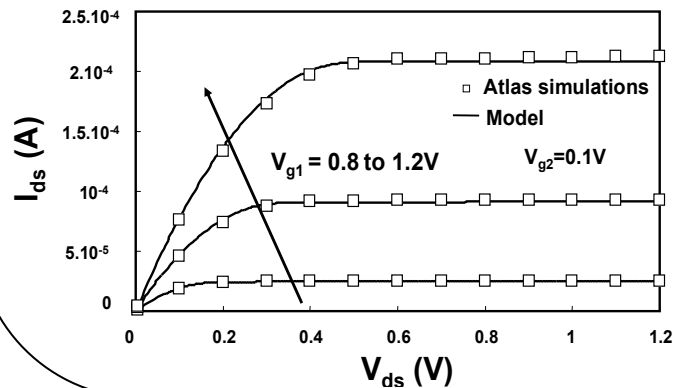
$T_{si} = 10$ nm
 $L = 0.5 \mu\text{m}$
 $W = 1 \mu\text{m}$

Linear scale

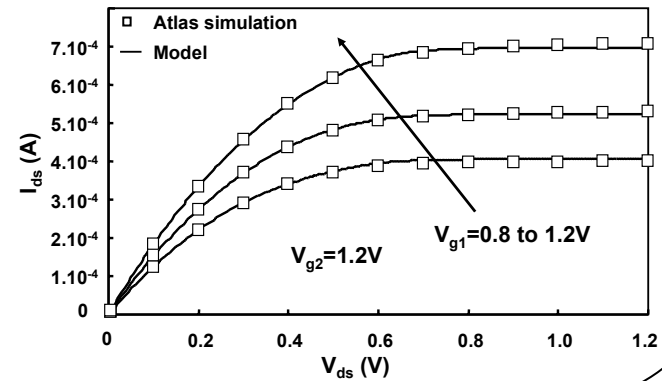


CURRENT

Linear scale

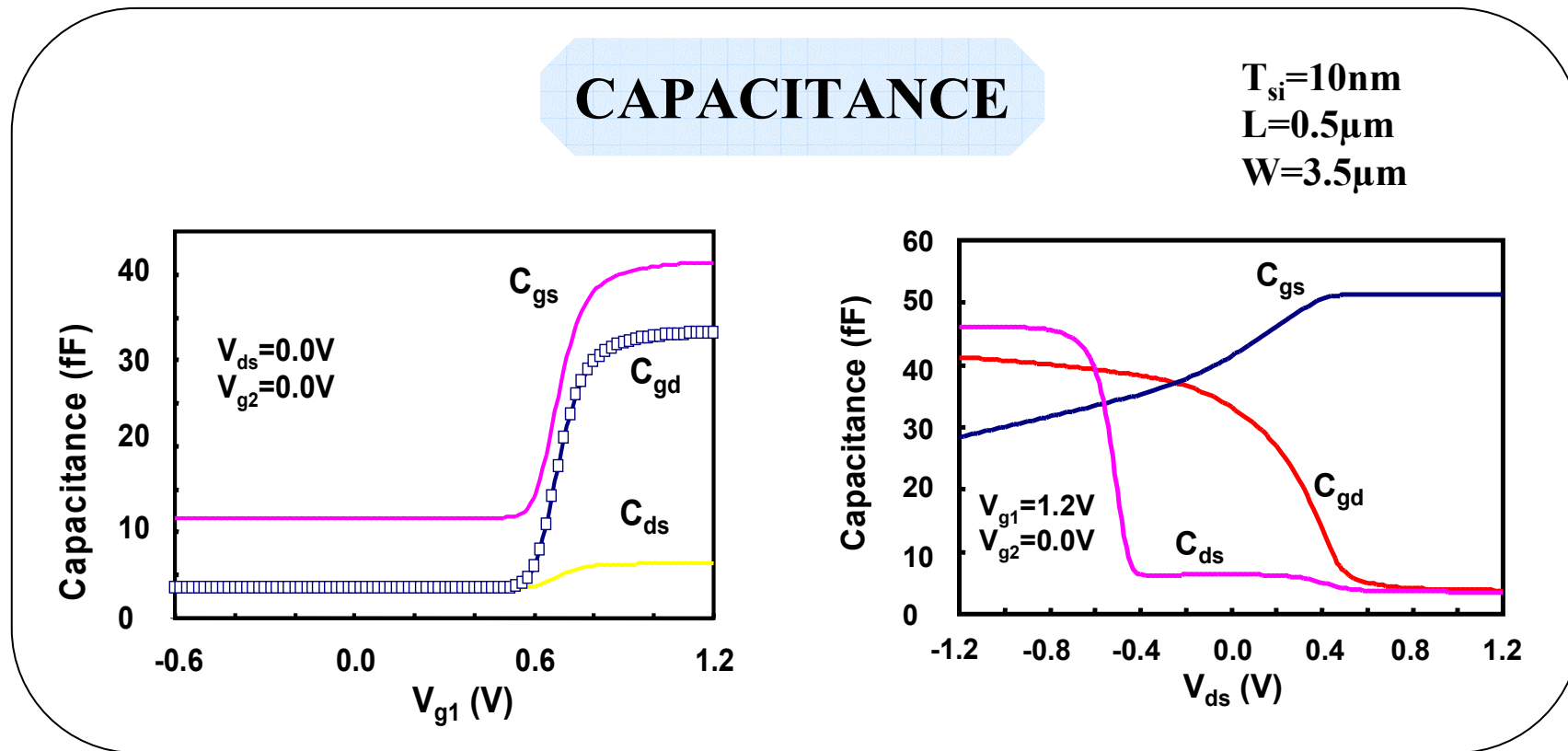


Linear scale



V_{th} -BASED MODEL

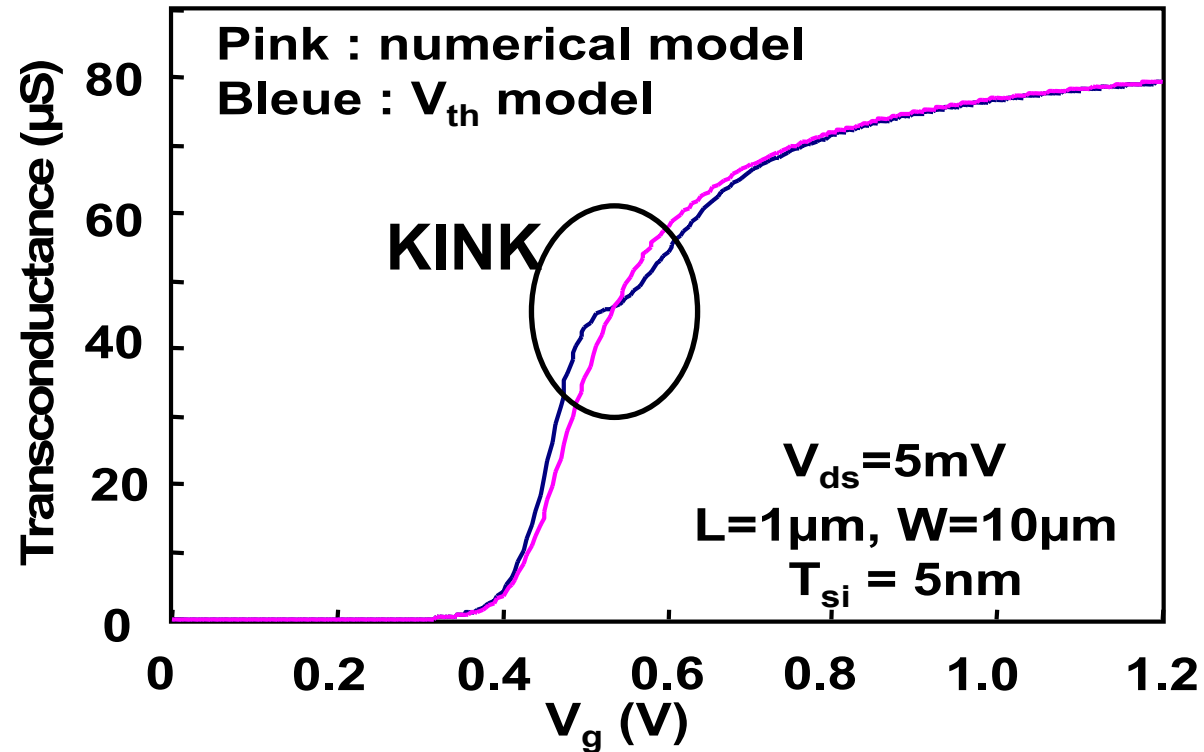
CHARGE MODELING → CAPACITANCE



V_{th} -BASED MODEL

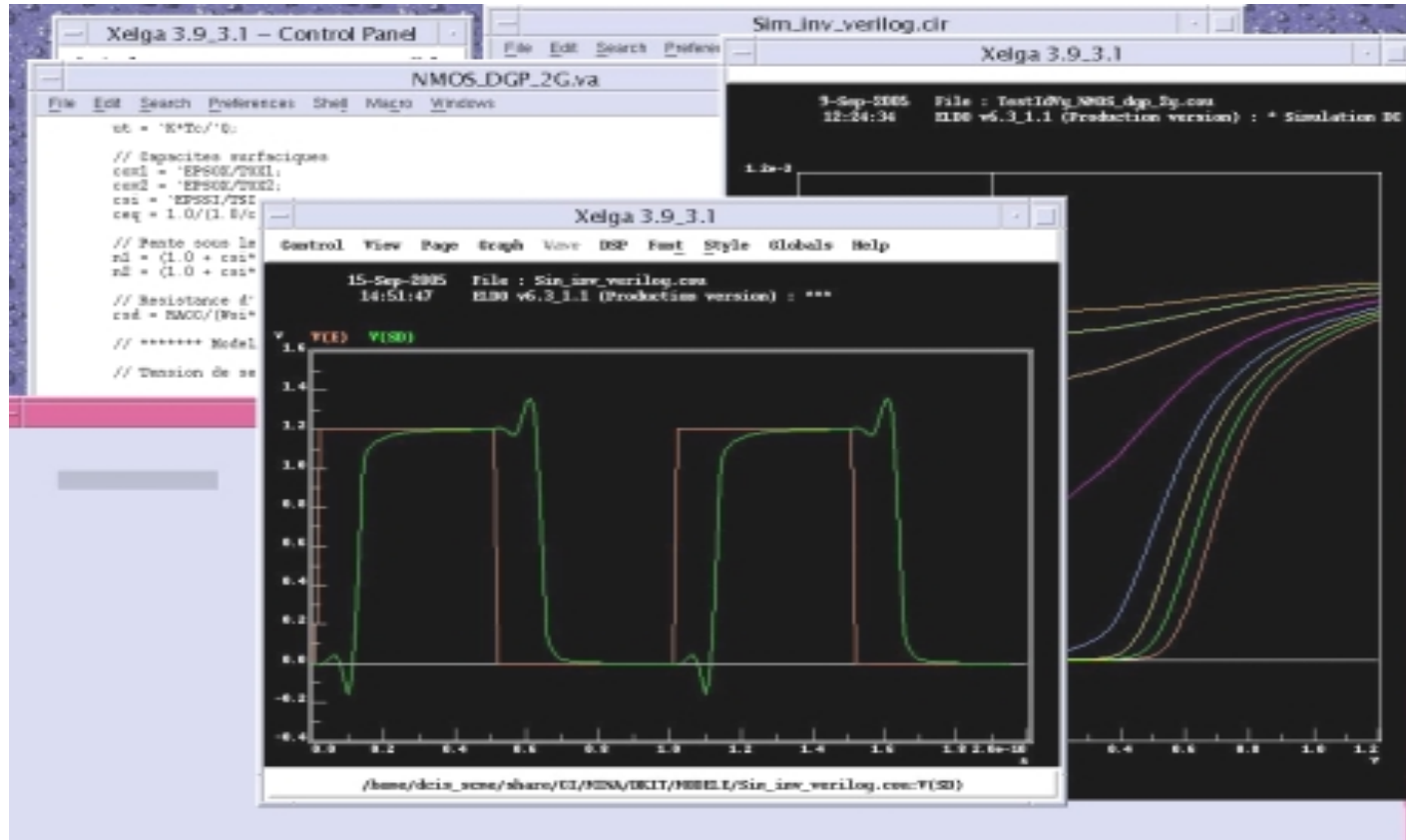
LIMITS $T_{si} < 10\text{nm}$: problem in derivative

ADG but SYMMETRICAL BEHAVIOR



EXPLICIT ANALYTICAL MODELING

EXAMPLE OF SIMULATION CIRCUITS USING V_{th} MODEL IN VERILOG-A



**INVERTORS
CHAIN
COMPOSED
OF 8
TRANSISTORS
ARE
SIMULATED IN
TRANSIENT
REGIME**

- The model took into account:
- classical SCE ($V_{th}(V_{ds})$)
 - access resistance

SUMMARY

2 MAIN WAYS TO MODEL ADG MOSFET:

IMPLICIT
ANALYTICAL MODEL:
ITERATIVE
RESOLUTION

EXPLICIT
ANALYTICAL MODEL:
FULLY ANALYTICAL
EXPRESSIONS

CHARGE-BASED
OR V_t MODEL

EFFECTS WHICH SHALL BE ADDED

Accurate
Short Channel Effects

Quantum effects

Ballistic transport

THANK YOU FOR YOUR ATTENTION