ANALOG/HV CHARACTERISATION FOR HV CMOS technology

Compact Modelling for Automotive applications

Ehrenfried Seebacher
MOS-AK 2005

a leap ahead
Presentation Overview

- HV CMOS transistor modelling
- Modelling of HV CMOS parasitics.
- High temperature modelling up to 200°C
- Mismatch considerations for HV CMOS
HV CMOS Device X-section

HV NMOS substrate based

HV NMOS isolated
- HV CMOS transistor modelling
- Modelling of HV CMOS parasitics.
- High temperature modelling up to 200°C
- Mismatch considerations for HV CMOS
Subcircuit:

The two JFETs J1 and J2 are responsible for the quasi-saturation and saturation region modelling.

The resistor R1 models the on-resistor accurately and the voltage controlled voltage source takes the scalability into account.

HV NMOS output characteristic
+= measurements,
fully scalable model for all geometries and operating conditions
solid lines = sub-circuit2.

Literature: E. Seebacher, G. Rappitsch, H. Höller and W. Posch
MOS TRANSISTOR MODELING FOR HV PROCESSES, MIXDES 2002
HV Transistor scalability

W/L=40/0.5

W/L=100/20
HV CMOS device overview

$L_c$ ........ Scalable transistor length

$L_{g1,2}$ ..... fixed length

$L_{dd}$ ........ Drift region
- splitting in three different regions
  -> three transistors
- difficult parameter extraction
- extended simulation time
- simplification is necessary

Advantage
- acceptable accuracy for the $R_{on}$ region
- parameter extraction unchanged to standard MOS
- very low simulation time

Drawback
- unacceptable deviations in the saturation region
- large deviation for MOS capacitances.
Model extension for Cap Modelling:
- Introduction of DLC (BSIM3v3
intrinsic cap parameter)
  - minimum requirement correct
gate cap.
- Introduction of a second transistor
  - results in high accurate intrinsic
capacitance behaviour.
Cap Results: Single transistor with DLC parameter

$c_{sd-g}$

$c_{bg}$

Simulation vs Measurement for $V_g = -0.0V$ to $-2.0V$ and $V_d = 0V$ to $-2.0V$ and $V_{bg} = 0V$ to $1.5V$.
Cap Results: Two Transistor Approach

A step ahead...
Presentation Overview

- HV CMOS transistor modelling
- Modelling of HV CMOS parasitics.
- High temperature modelling up to 200°C
- Mismatch considerations for HV CMOS
H- Bridge induces a parasitic substrate current

- \( I_{ds} \) .... Forward current
- Free wheeling current ....
off motor and \( V_{GS} = 0 \) results in inductive current
- parasitic pnp transistor occurs.

\[ P_v = V_{ds} \times I_{ds} \]

Free wheeling current
Transmission Gate: switching induces parasitic PNP

Symmetrical MOS Transistors:
Source and Drain can both be pulled to 50V
=> Current can flow in both Directions

Charge Loss over the parasitic PNP:
One of the NMOSI50H Transistors is always in reverse operation.
Source/Body can be higher than Drain, this can turn on the parasitic PNP.
**Requirement:**

- Junction capacitance
- SGP current model
- Scalability
- Temperature behaviour
Parasitic PNP Models for NMOSI50 Transistors

- Parasitic *pnp* SGP models have been prepared for the isolated NMOS transistors NMOSI50,

- 11 different geometries have been included in the extraction process.

- Used geometries:

<table>
<thead>
<tr>
<th>W</th>
<th>10</th>
<th>20</th>
<th>40</th>
<th>40</th>
<th>40</th>
<th>10</th>
<th>15</th>
<th>40</th>
<th>1000</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>0.5</td>
<td>0.5</td>
<td>0.3</td>
<td>0.5</td>
<td>1</td>
<td>2</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>W*L</td>
<td>5</td>
<td>10</td>
<td>12</td>
<td>20</td>
<td>40</td>
<td>80</td>
<td>100</td>
<td>150</td>
<td>400</td>
<td>500</td>
</tr>
</tbody>
</table>

- Measurements: Vb=Vs=Vg (E), Vpsub_dntub (CB) up to 50V

- Parameters scaling with area= W*L

- Temperature behavior was characterised from -40..200°C
SGP Parameter scaling

- Parameters scaling with area = W*L, BF has a random variation

\[ IS = \exp(IS_0 + ISL_0 \cdot (area + IS_0)) \]

\[ VAF = \exp(VAF_0 + VAFL_0 \cdot (area + VAF_0)) \]

![Graph showing IS and VAF scaling with inverse emitter length](image1)

![Graph showing IS and VAF scaling with inverse emitter length](image2)
Results: Parasitic PNP Models for NMOSI50 Transistors

![Graphs showing I_C/I_B vs V_{be} for different Ucb and Tamb values for NMOS_80 (NI50TC) FINAL0@FG and NMOS_80 (NI50HC) SGTMP2@FGT models.]

Measurements: symbols
- ○ Ucb=0V, Tamb=200°C
- * Ucb=10V, Tamb=175°C
- O Ucb=20V, Tamb=150°C
- * Ucb=30V, Tamb=125°C
- X Ucb=40V, Tamb=100°C
- + Ucb=50V, Tamb=75°C
- ◯ Ucb=60V, Tamb=50°C
- ◯ Ucb=70V, Tamb=25°C
- ◯ Ucb=80V, Tamb=0°C
- ◯ Ucb=90V, Tamb=-25°C
- ◯ Ucb=100V, Tamb=-40°C

IC, IB [A]
Presentation Overview

- HV CMOS transistor modelling
- Modelling of HV CMOS parasitics.
- High temperature modelling up to 200°C
- Mismatch considerations for HV CMOS
Notes on MOS High Temp. Modelling

- MOS and HV-MOS transistor
  - Temp. measurements transfer and output characteristics (−40, ..., 200 °C), Large devices and for minimum channel length
  - Threshold voltage temperature-coeff. TCVTH, mobility exponent BEX (=UTE) and on-resistor temp-coeff. TCRON have been extracted
  - No changes for standard MOS
- Diode leakage is dominant and should be modelled accurately
- Improvements for HV-MOS sub-circuit
  - The threshold voltage of the JFET and the current gain factor BETA are adjusted with a factor F(Temp):

\[ F(T) = (1 + TCVTHJ \cdot (T - TMVTHJ)) \]
Results: NMOS50H @ 175°C

IDS [A] vs. VDS [V] for different VBS [V] and VG [V].

- Measurements for W/L = 100/20:
  - VBS = 0 V, VG = 2.9, 4.8, 6.7, 8.6, 10.5, 12.4, 14.3, 16.2, 18.1, 20 V

- Measurements for W/L = 40/1:
  - VBS = 0 V, VG = 2.9, 4.8, 6.7, 8.6, 10.5, 12.4, 14.3, 16.2, 18.1, 20 V

Note: Data points are indicated by markers on the graphs.
Poly Resistor:

\[ R(T) = R(T_0) \cdot \left( TCR1 \cdot (T - T_0) + TC2 \cdot (T - T_0)^2 \right) \]

\[ TCR1(W) = \frac{TC1}{\sqrt{1 + \frac{WTC}{W^{NTC}}}} \]
- HV CMOS transistor modelling
- Modelling of HV CMOS parasitics.
- High temperature modelling up to 200°C
- Mismatch considerations for HV CMOS

Goal of Mismatch Characterisation

Characterisation and Modelling of HV-MOSFET MISMATCH

- Yield prediction during the design phase
- Improvement of the circuit robustness

NEEDED:
- Proper mismatch model
- Parameter extraction strategy
- Simulator implementation
Matched transistor pair:

Pair of MOS transistors with identical layout close to each other

Measurement:

\[
\frac{\Delta I_D}{I_D} = \frac{2 \cdot (I_D_1 - I_D_2)}{(I_D_1 + I_D_2)}
\]

\[
\sigma \left( \frac{\Delta I_D}{I_D} \right) = \sigma \left( \frac{2 \cdot (I_D_1 - I_D_2)}{(I_D_1 + I_D_2)} \right)
\]

Measured data from production: ID - mismatch [%]

n=997, min= -0.88%, max= 0.7%
• Measure current ID1 and ID2 for several gate voltages (k=21 points per curve).

• Several matched pairs of NMOS or PMOS transistors (m=60 pairs per wafer).

• Calculate relative mismatch

\[
\sigma(\Delta ID / ID) = \sigma\left(\frac{2 \cdot (ID_1 - ID_2)}{(ID_1 + ID_2)}\right)
\]

for any gate voltage.
Variance Model

Drain current model:

\[ I_D = f(P_1, P_2, \ldots, P_n) \]

Taylor Expansion:

\[
\frac{\Delta I_D}{I_D} = 1 \frac{\partial f}{\partial P_1} \Delta P_1 + 1 \frac{\partial f}{\partial P_2} \Delta P_2 + \cdots + 1 \frac{\partial f}{\partial P_n} \Delta P_n + \text{corr.}
\]

\[
\sigma^2 \left( \frac{\Delta I_D}{I_D} \right) = S_{P_1}^2 \sigma^2(\Delta P_1) + S_{P_2}^2 \sigma^2(\Delta P_2) + \cdots + S_{P_n}^2 \sigma^2(\Delta P_n) + \text{corr}
\]
HV-MOS Structure & Model

MOS Model + Drain Resistor

Parameters:

\[ V_T \quad \kappa \quad \theta \quad R_D \]

……Saturation region

\[ I_D = \frac{W \kappa (V_G - V_T)^2}{L \left( 2 + 1 + \theta (V_G - V_T) \right)} \]

……Linear region

\[ I_D = \frac{W \kappa (V_G - V_T) \cdot VDS}{L \left( 1 + (\theta + \alpha_r) \cdot (V_G - V_T) \right)}, \quad \alpha_r = \frac{W}{L} \cdot \kappa \cdot R_D \]
Sensitivities Saturation:

\[ \frac{\Delta I_D}{I_D} = f_{\text{sat}}(\Delta V_T, \Delta \kappa, \Delta \theta) \]

\[ \sigma(\Delta V_T), \sigma(\Delta \kappa), \sigma(\Delta \theta) \]

Extract from measured \( \sigma(\Delta I_D)/I_D \)

\[ I_D = \frac{W \kappa}{L} \frac{(V_G - V_T)^2}{2 + \theta(V_G - V_T)} \]

\[ \Rightarrow \]

Taylor Expansion

\[ \Delta I_D = \left( \frac{\partial I_D}{\partial V_T} \right) \Delta V_T + \left( \frac{\partial I_D}{\partial \kappa} \right) \Delta \kappa + \left( \frac{\partial I_D}{\partial \theta} \right) \Delta \theta \]

\[ \frac{\Delta I_D}{I_D} = -\left( \frac{2 + \theta(V_G - V_T)}{(V_G - V_T)(1 + \theta(V_G - V_T))} \right) \Delta V_T + \frac{1}{\kappa} \Delta \kappa - \left( \frac{V_G - V_T}{1 + \theta(V_G - V_T)} \right) \Delta \theta \]
Sensitivities linear Region:

\[ \frac{\Delta I_D}{I_D} = f_{\text{lin}}(\Delta V_T, \Delta \kappa, \Delta \theta, \Delta R_D) \]

Extract \( \sigma(\Delta V_T), \sigma(\Delta R) \) from measured \( \sigma(\Delta I_D)/I_D \)

\[ I_D = \frac{W}{L} \frac{\kappa (V_G - V_T) \cdot VDS}{1 + (\theta + \alpha_r) \cdot (V_G - V_T)}, \quad \alpha_r = \frac{W}{L} \cdot \kappa \cdot R_D \]

Taylor Expansion 1st oder

\[ \Delta I_D = \left( \frac{\partial I_D}{\partial V_T} \right) \Delta V_T + \left( \frac{\partial I_D}{\partial \kappa} \right) \Delta \kappa + \left( \frac{\partial I_D}{\partial \theta} \right) \Delta \theta + \left( \frac{\partial I_D}{\partial R_D} \right) \Delta R_D \Rightarrow \]
Sensitivities linear Region:

\[
\frac{\Delta I_D}{I_D} = \left(\frac{1}{V_G - V_T}(1 + (\theta + \alpha)(V_G - V_T))\right)\Delta V_T - \left(\frac{V_G - V_T}{1 + (\theta + \alpha)(V_G - V_T)}\right)\Delta \theta
\]

\[
+ \left(\frac{1 + \theta(V_G - V_T)}{\kappa(1 + (\theta + \alpha)(V_G - V_T))}\right)\Delta \kappa - \left(\frac{W}{L} \frac{\kappa(V_G - V_T)}{1 + (\theta + \alpha)(V_G - V_T)}\right) \cdot \Delta R_D
\]

\[
- \frac{I_D}{VDS}
\]
Sensitivity voltage dependency

![Graph showing sensitivity voltage dependency](image)

- **S** - relative sensitivities for different parameters.
- **STheta** - relative sensitivity with respect to temperature.
- **SRD** - relative sensitivity with respect to device dimensions.

The graph displays the relative sensitivities of the system as a function of gate-source voltage (Vgs). The x-axis represents Vgs in volts (V), and the y-axis represents the relative sensitivities.
Extraction of mismatch parameters

\[ \sigma^2 \left( \frac{\Delta I_D}{I_D} \right) = S_{VT}^2 \sigma^2(\Delta V_T) + S_\kappa^2 \sigma^2(\Delta \kappa) + S_\theta^2 \sigma^2(\Delta \theta) + S_R^2 \sigma^2(\Delta R) \]

1. Step: Saturation:

Extract \( \sigma(\Delta V_T), \sigma(\Delta \kappa), \sigma(\Delta \theta) \) from measured \( \sigma(\Delta I_D)/I_D \)

2. Step: linear region:

Extract \( \sigma(\Delta V_T), \sigma(\Delta R) \) from measured \( \sigma(\Delta I_D)/I_D \)

\( \sigma^2(\Delta V_T) \): threshold mismatch parameter

\( \frac{\sigma^2(\Delta \kappa)}{\kappa^2} \): gain mismatch parameter

\( \sigma^2(\Delta \theta) \): mobility reduction mismatch parameter

\( \sigma^2(\Delta R_D) \): drain resistor mismatch parameter
RESULT: Saturation Region

VG [V]  

Sigma(Delta(ID)/ID) [%]

n50h
RESULT: Saturation Region

n50h $A_{VTH} = (2.755 \times 10^{-08} \pm 3.211 \times 10^{-09}) \text{ V m} \frac{1}{\sqrt{W \cdot L}} / (1/m)$

n50h $A_{U0} = (1.06 \times 10^{-06} \pm 1.754 \times 10^{-07}) \% \text{ m} \frac{1}{\sqrt{W \cdot L}} / (1/m)$
RESULT: Linear Region

\[ \text{Sigma(Delta(\text{ID})/ID)} \% \]

\[ A_{RD} = (4.075 \pm 1.153) \text{ Ohm} \]
- HV CMOS transistor sub-circuit modelling including
  - capacitance
  - high temperature
  - mismatch
  - parasitic pnp.