FROM RESEARCH TO INDUSTRY

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NEW VERSION OF LETI-UTSOI2 FEATURING FURTHER IMPROVED PREDICTABILITY, AND A NEW STRESS MODEL FOR FDSOI TECHNOLOGY

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Leti

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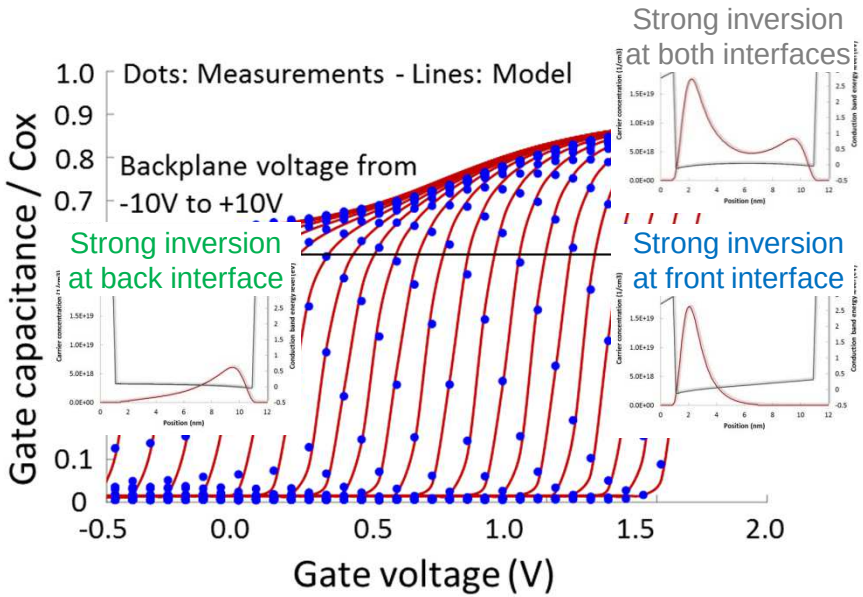
Leti-UTSOI2.1: new version of Leti compact model for FDSOI technologies

- **Status of Leti-UTSOI2**
- **Improvements implemented on the new version**
  - Predictability of 2D-electrostatic model
  - Weak/moderate inversion regime description
  - Gate current model
  - Narrow channel effects
- **Summary**

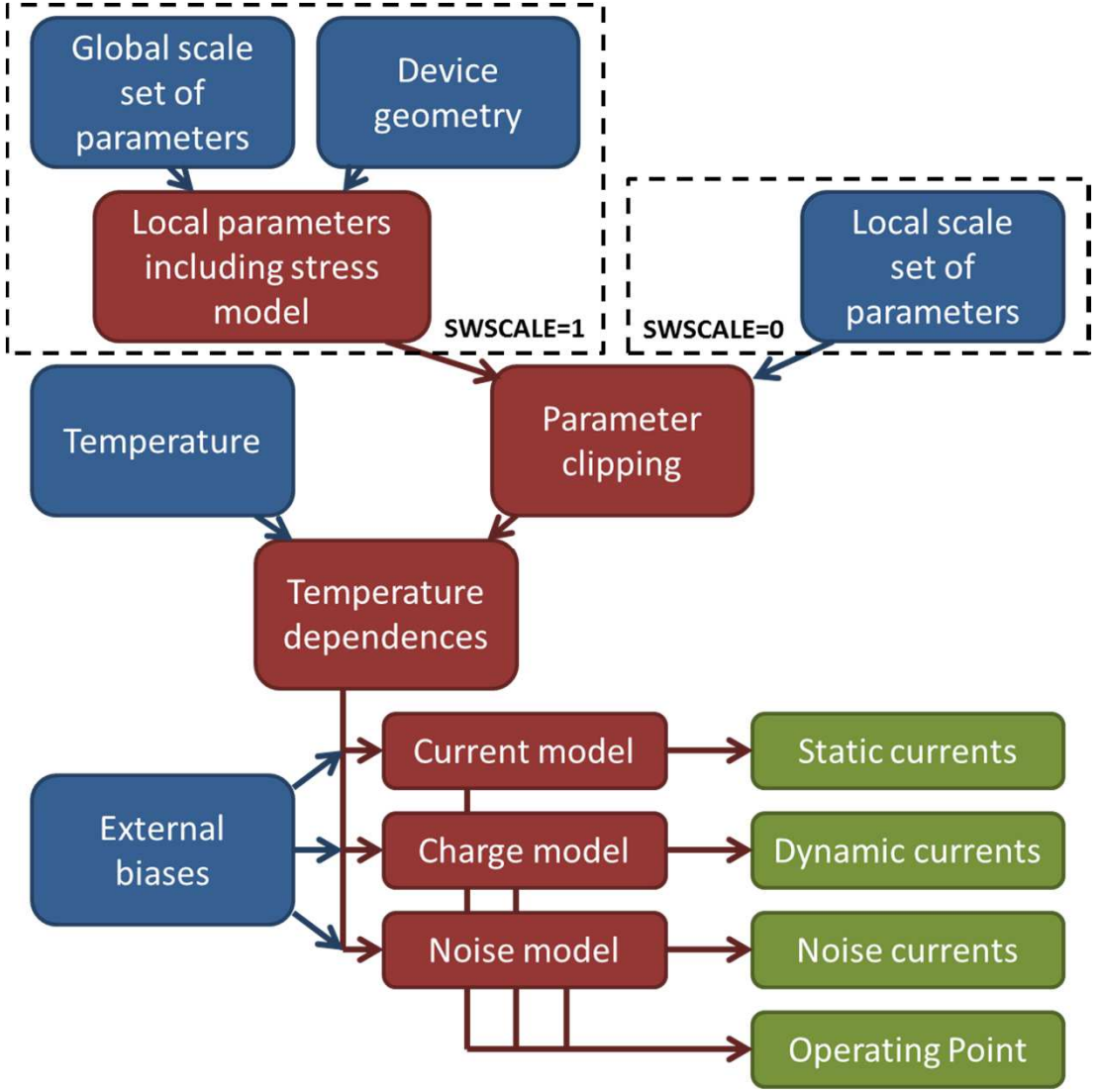
Status of Leti-UTSOI2

- Leti-UTSOI2 is the first compact model able to describe FDSOI transistor behavior in all bias configurations, including strong forward back bias
- Presented in *T. Poiroux et al, IEDM 2013* and *T. Poiroux et al, MOS-AK dec 2013*
- Leti-UTSOI2 is currently used in industrial PDKs from ST Microelectronics
- End of 2014, a new version of the model, Leti-UTSOI2.1, has been implemented in all major SPICE simulation tools



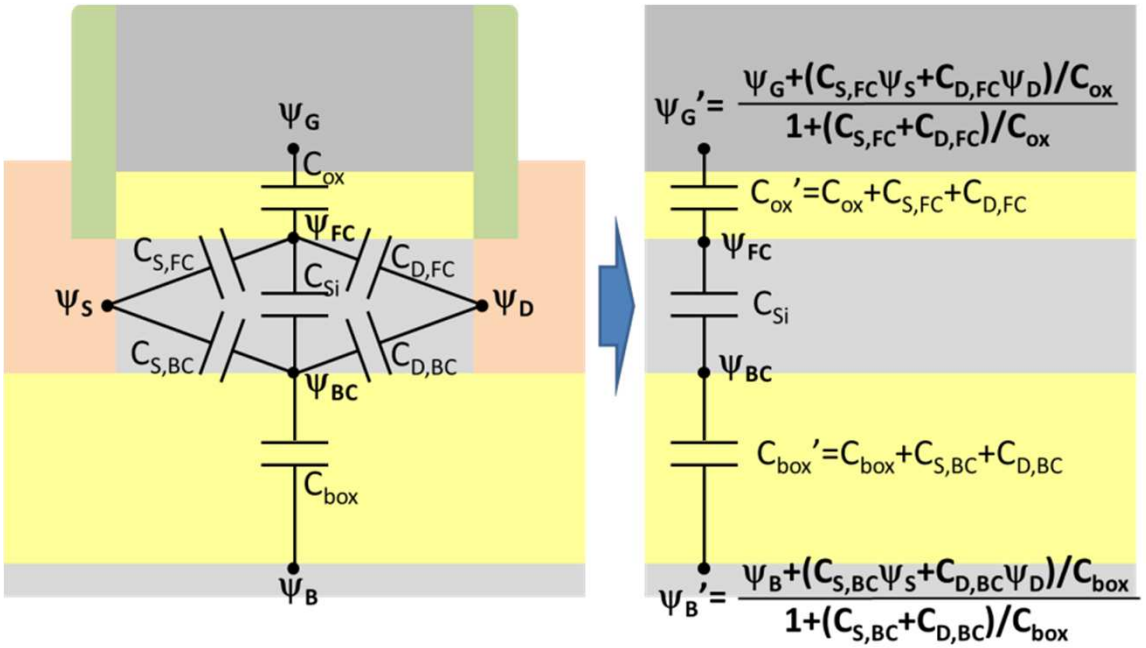
Model structure

Leti-UTSOI2 is a surface potential model featuring local / global scale levels, as PSP and Leti-UTSOI1



Predictability of 2D electrostatics

- **2D electrostatics in Leti-UTSOI2 is based on equivalent 1D model accounting for 2D couplings**
  - Effective geometry and biases allowing 2D interface potentials calculation with 1D model

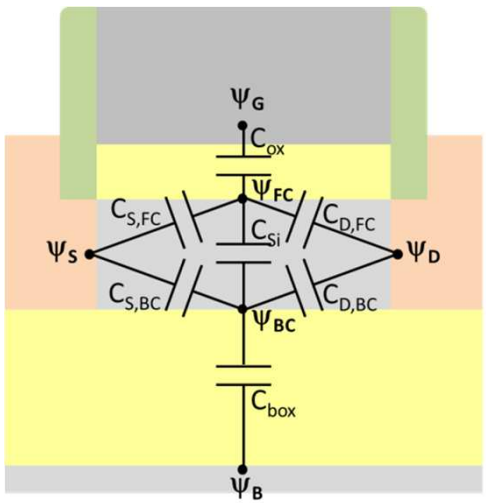


Predictability of 2D electrostatics

- **Link with process parameters at front gate (Leti-UTSOI2.1)**

$$V'_{GS} - \Delta\phi_m - \frac{E_G}{2q} = \frac{V_{GS} - \Delta\phi_m - E_G/(2q) + (C_{D,FC}/C_{ox})V_{DS}}{1 + (C_{S,FC} + C_{D,FC})/C_{ox}}$$

$$C'_{ox} = C_{ox}\left(1 + \frac{C_{S,FC} + C_{D,FC}}{C_{ox}}\right)$$



Subthreshold swing degradation factor: local parameter **PSCE**

$$\mathbf{PSCE} = 2 \times \mathbf{PSCEL}\left(\sqrt{\frac{\varepsilon_{ch} t_{Si}/2}{L_{eff}/2}\frac{t_{ox}+t_{ds}}{\varepsilon_{ox} L_{eff}}}\right)^{\mathbf{PSCELEXP}}$$

$$\mathbf{PSCE} = 2 \times \mathbf{PSCEL}\left(\lambda_{2D}/L_{eff}\right)^{\mathbf{PSCELEXP}}$$

with $\lambda_{2D} = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} t_{Si}(t_{ox} + t_{ds})}$ (same as *K.K. Young, IEEE TED, 1989*)

Predictability of 2D electrostatics

- **Link with process parameters at front gate (Leti-UTSOI2.1)**

$$V'_{GS} - \Delta\phi_m - \frac{E_G}{2q} = \frac{V_{GS} - \Delta\phi_m - E_G/(2q) + (C_{D,FC}/C_{ox})V_{DS}}{1 + (C_{S,FC} + C_{D,FC})/C_{ox}}$$

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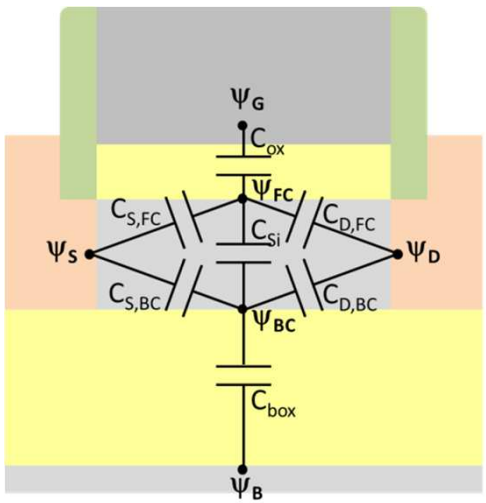


DIBL factor: local parameter **CF**

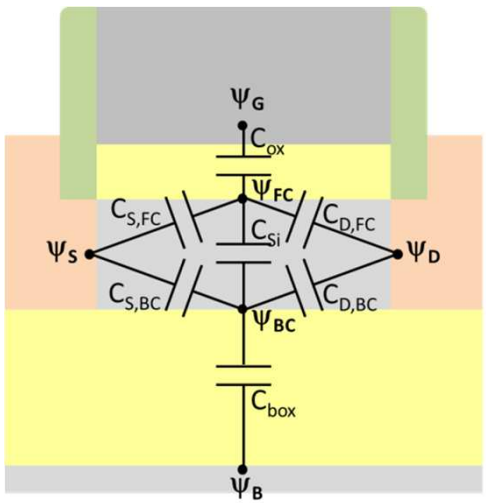
$$\mathbf{CF} = \mathbf{CFL}(\lambda_{2D}/L_{eff})^{\mathbf{CFLEXP}}$$

Predictability of 2D electrostatics

- **Link with process parameters at back gate (Leti-UTSOI2.1)**

$$V'_{BS} - \Delta\phi_{mb} - \frac{E_G}{2q} = \frac{V_{BS} - \Delta\phi_{mb} - E_G/(2q) + (C_{D,BC}/C_{box})V_{DS}}{1 + (C_{S,BC} + C_{D,BC})/C_{box}}$$

$$C'_{box} = C_{box}\left(1 + \frac{C_{S,BC} + C_{D,BC}}{C_{box}}\right)$$



Sub. swing degradation factor: asymmetry local parameter **PSCEB**

$$PSCE_{back} = \mathbf{PSCE} \times \mathbf{PSCEB} \times \frac{t_{box}}{t_{ox}} \quad \text{with} \quad \mathbf{PSCEB} = \frac{C_{S,BC}+C_{D,BC}}{C_{S,FC}+C_{D,FC}}$$

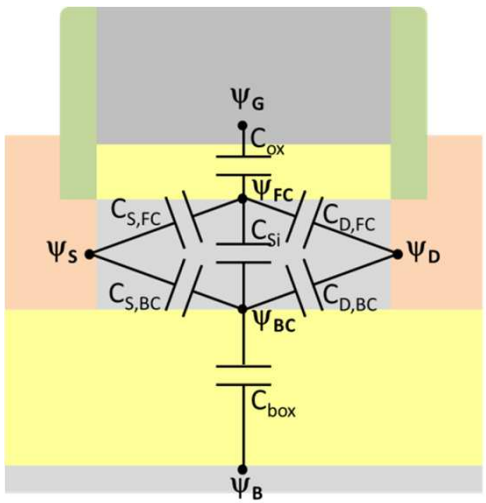
$\mathbf{PSCEB} = \mathbf{PSCEBO}$ not scalable

Predictability of 2D electrostatics

- **Link with process parameters at back gate (Leti-UTSOI2.1)**

$$V'_{BS} - \Delta\phi_{mb} - \frac{E_G}{2q} = \frac{V_{BS} - \Delta\phi_{mb} - E_G/(2q) + (C_{D,BC}/C_{box})V_{DS}}{1 + (C_{S,BC} + C_{D,BC})/C_{box}}$$

$$C'_{box} = C_{box}\left(1 + \frac{C_{S,BC} + C_{D,BC}}{C_{box}}\right)$$



DIBL factor: asymmetry local parameter **CFB**

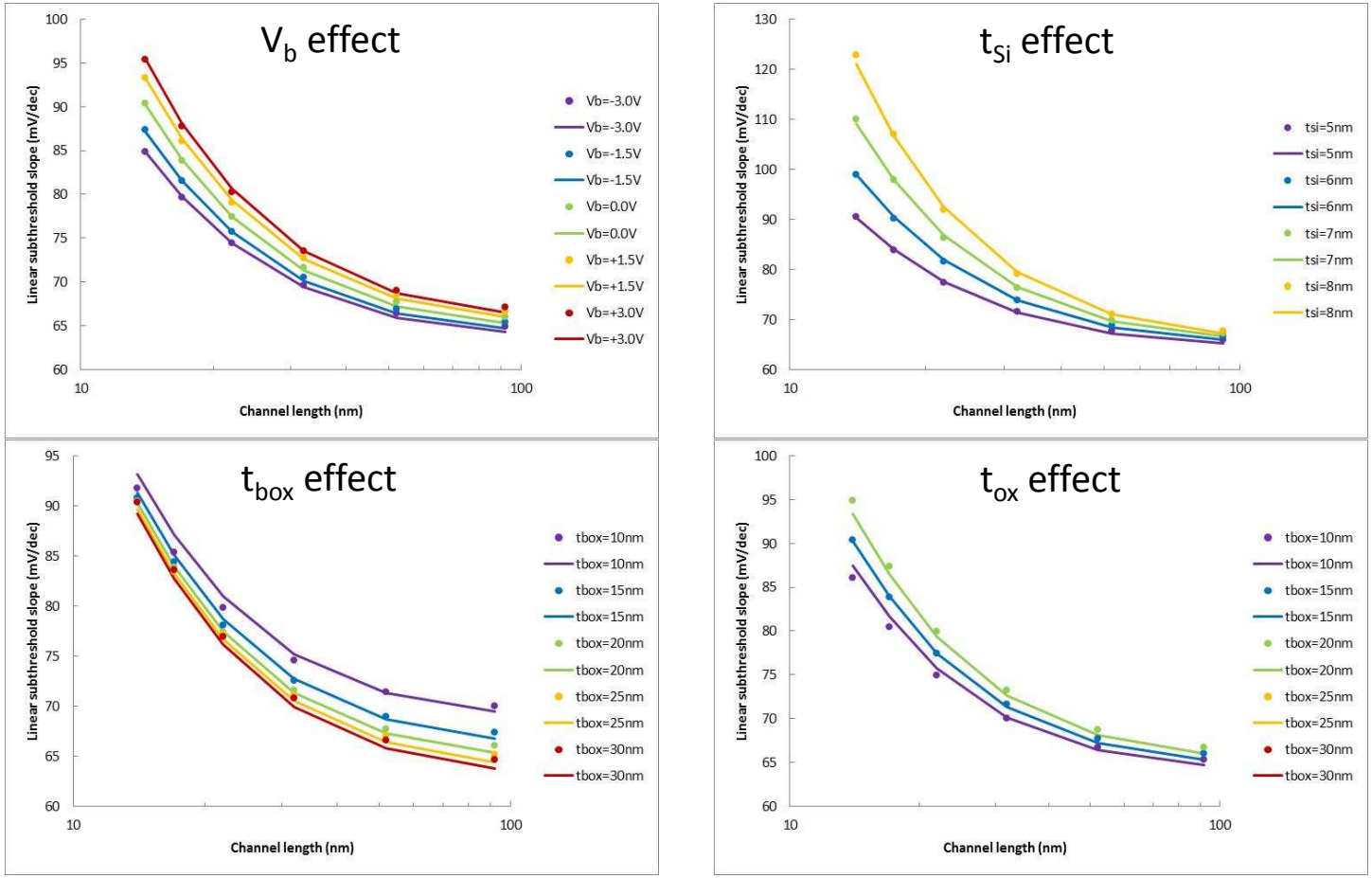
$$CF_{back} = \mathbf{CF} \times \mathbf{CFB} \times \frac{t_{box}}{t_{ox}} \quad \text{with} \quad \mathbf{CFB} = \frac{C_{D,BC}}{C_{D,FC}}$$

$\mathbf{CFB} = \mathbf{CFBO}$ not scalable

Predictability of 2D electrostatics: sub. swing

- **Comparison to TCAD simulations (lines: model, dots: TCAD)**

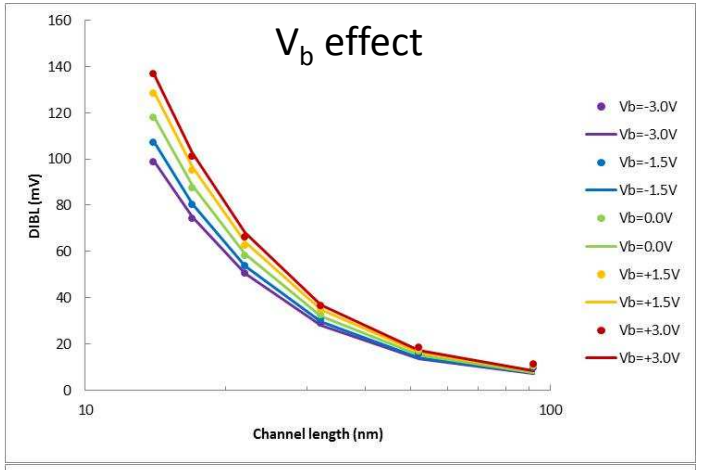
Parameters **PSCEL**, **PSCELEXP**, **PSCEBO** set on « Vb effect » curve

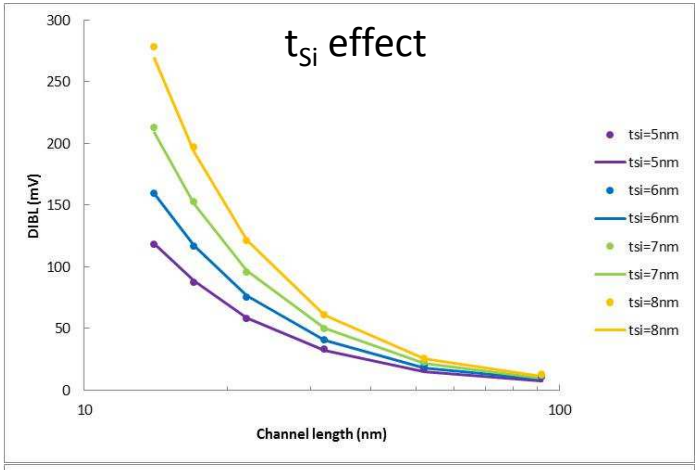


Predictability of 2D electrostatics: DIBL

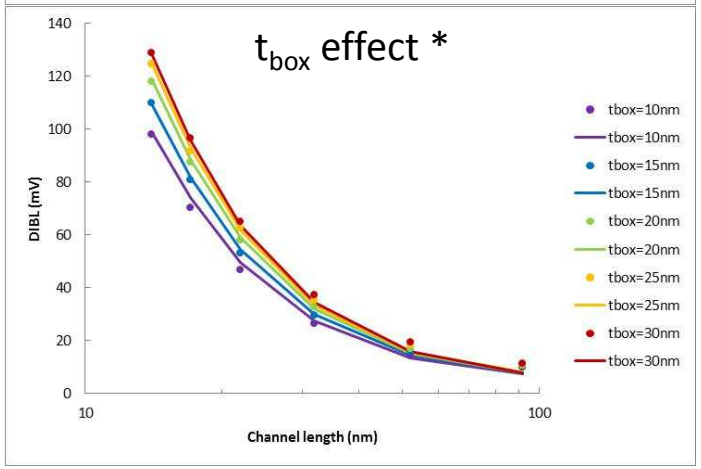
- **Comparison to TCAD simulations (lines: model, dots: TCAD)**

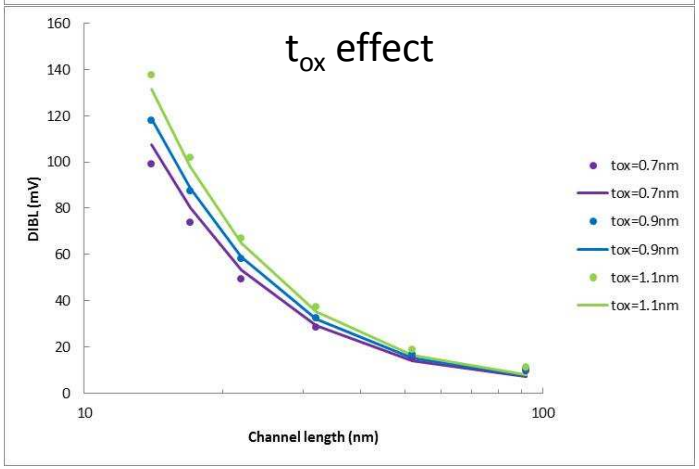
Parameters **CFL**, **CFLEXP**, **CFBO** set on « Vb effect » curve





* For large t_{box} variations, slight dependence of **CFBO** with t_{box} is required to capture properly fringing fields effect

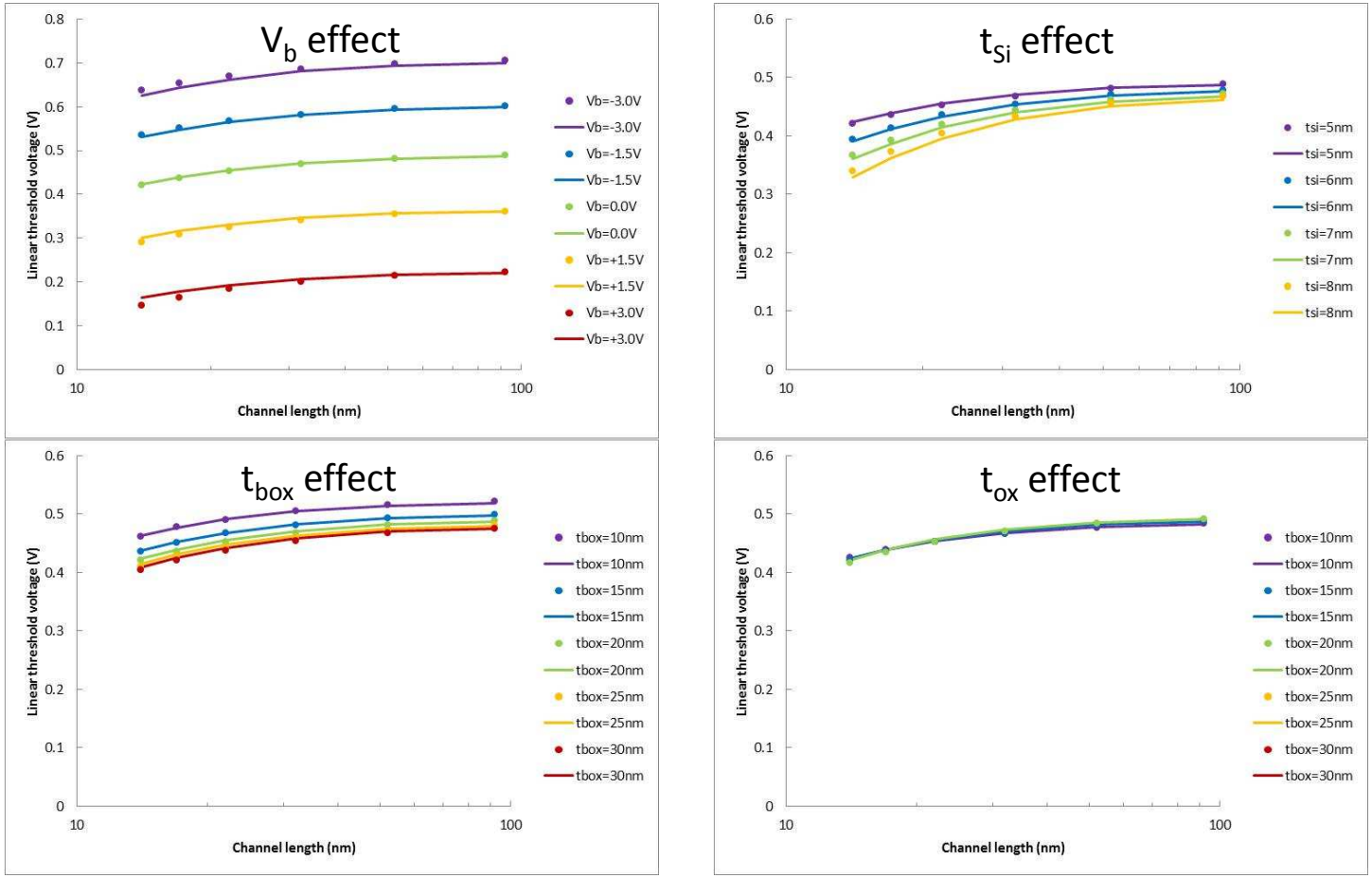




Predictability of 2D electrostatics: linear V_{th}

- **Comparison to TCAD simulations (lines: model, dots: TCAD)**

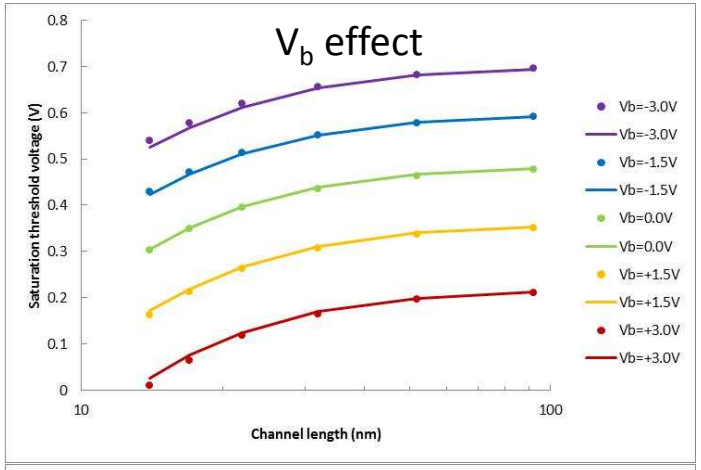
No additional parameters

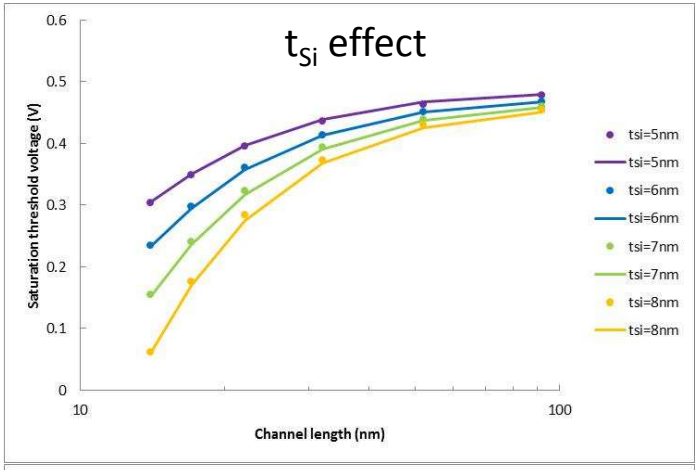


Predictability of 2D electrostatics: sat. V_{th}

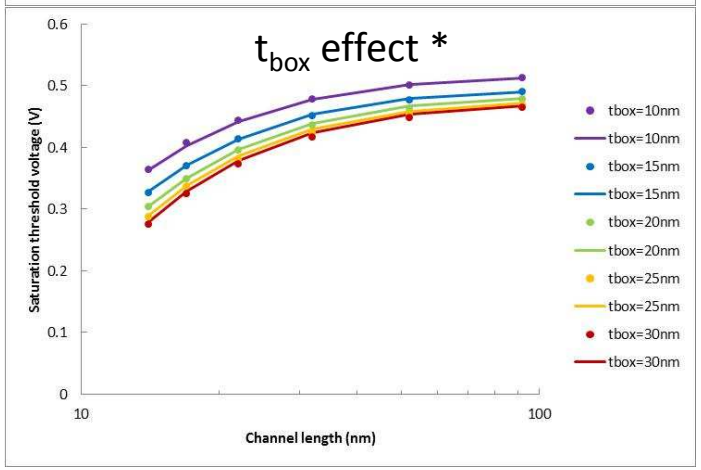
- **Comparison to TCAD simulations (lines: model, dots: TCAD)**

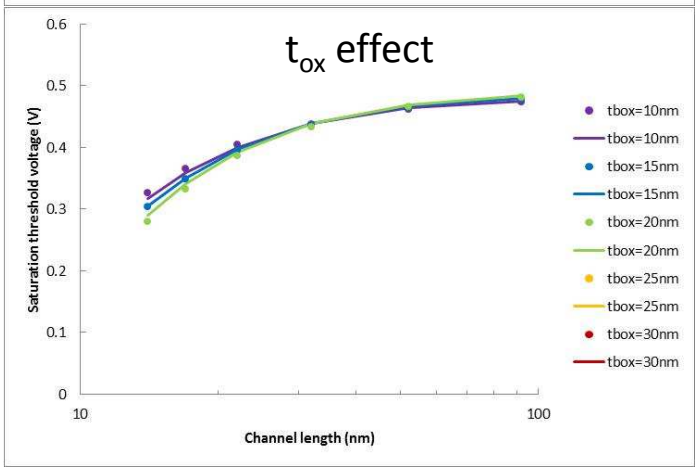
No additional parameters





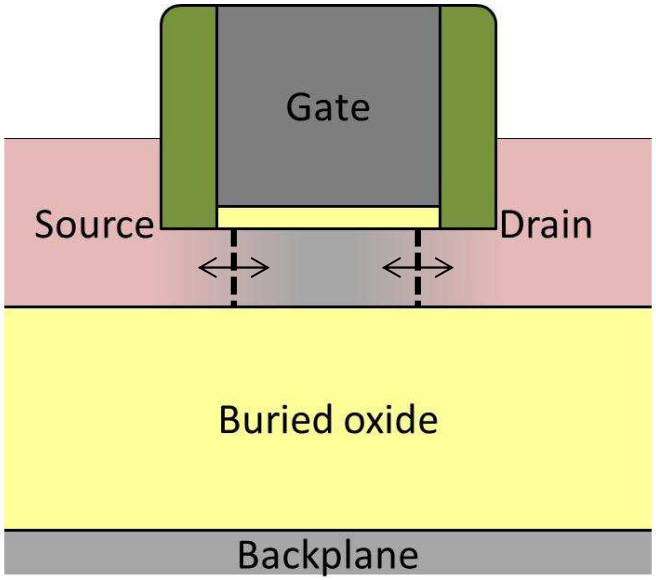
* including slight dependence of **CFBO** with t_{box}



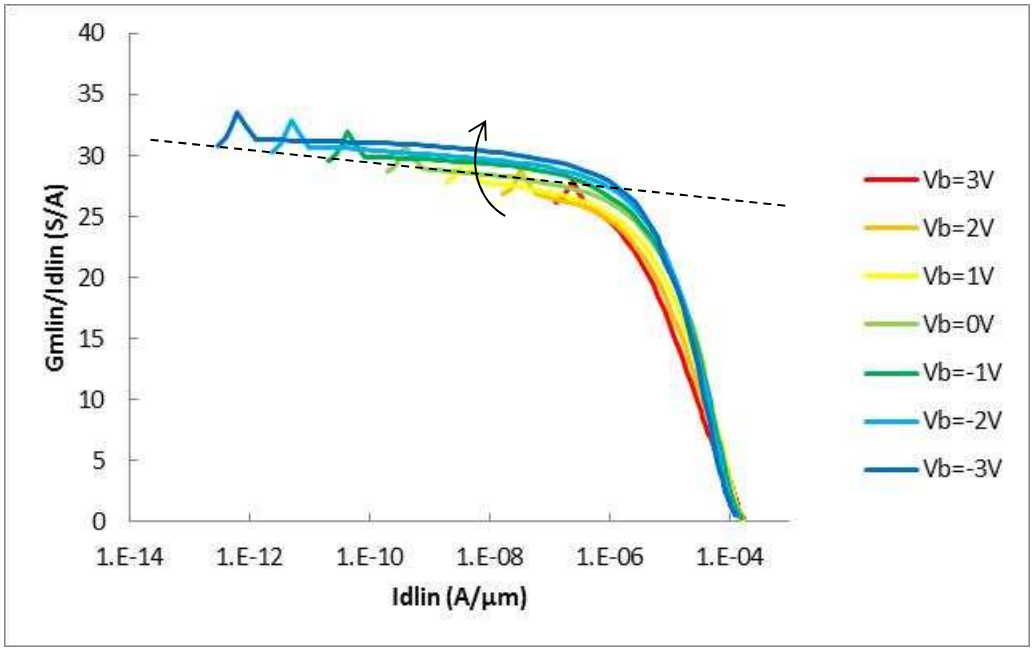


Accuracy in weak/moderate inversion regime

- **Depletion of source/drain LDD tails depends on front/back bias**
  - Electrical channel length is not constant in subthreshold regime
  - Subthreshold slope is non uniform => Gm/Id is varying vs Vg and Vb



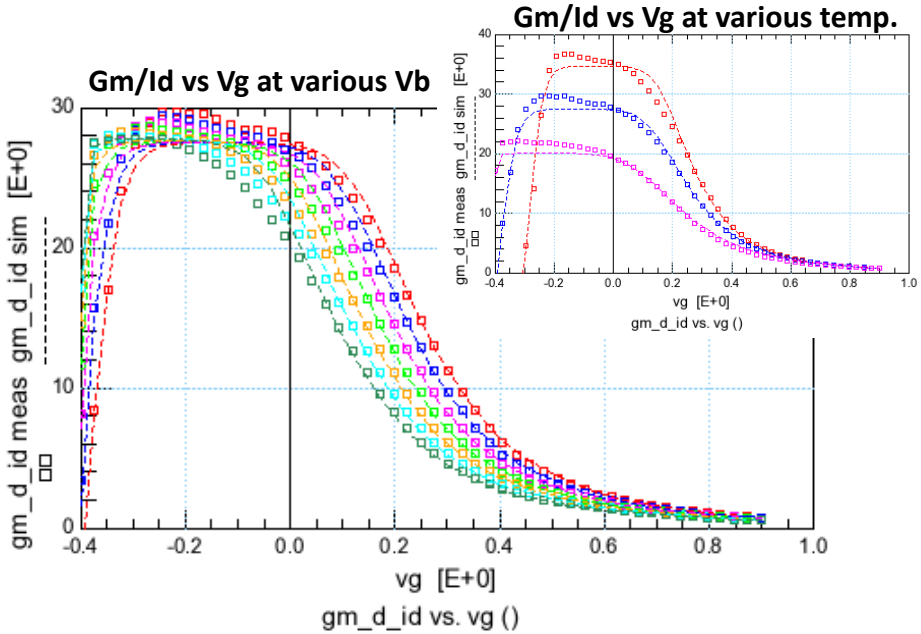
Results from TCAD simulations



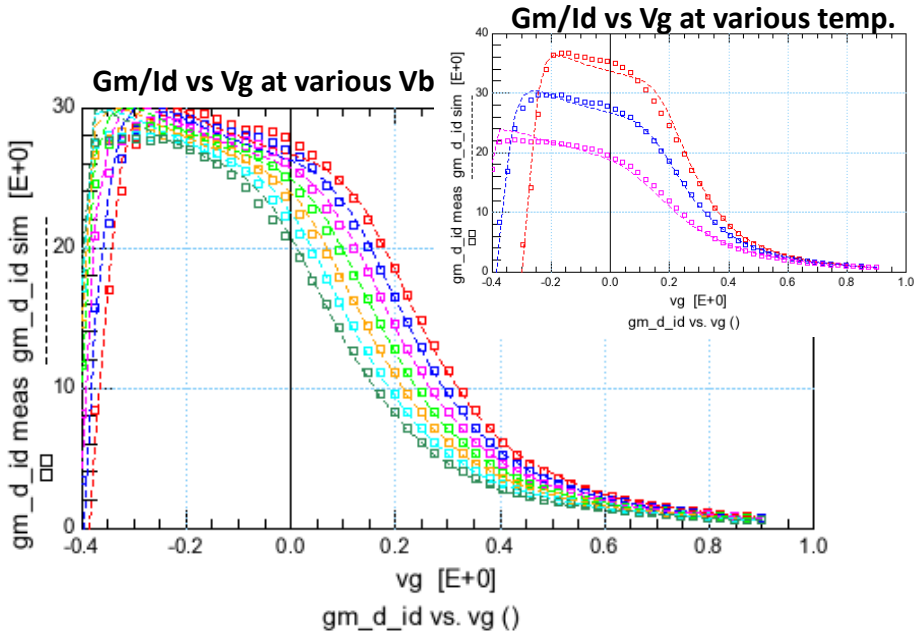
Accuracy in weak/moderate inversion regime

- Leti-UTSOI2 has been improved to capture this effect
- Comparison to hardware data

Without L_{eff} dependence (Leti-UTSOI2.0)

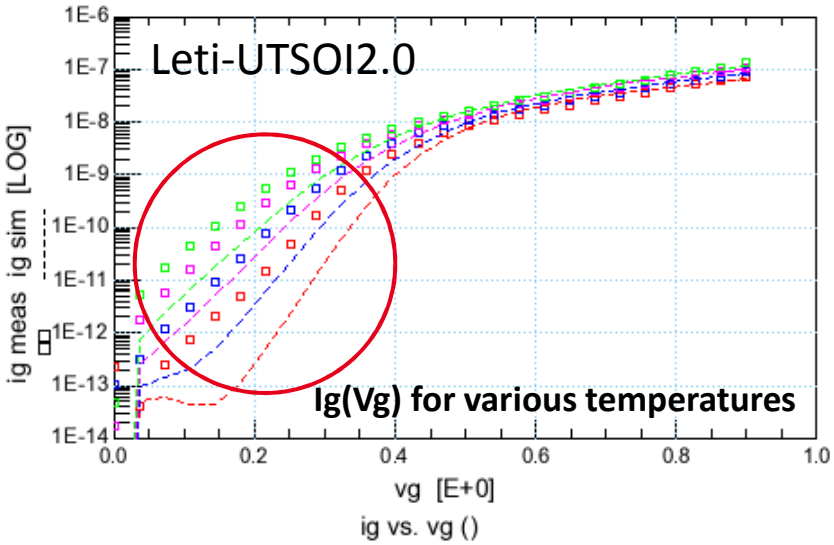


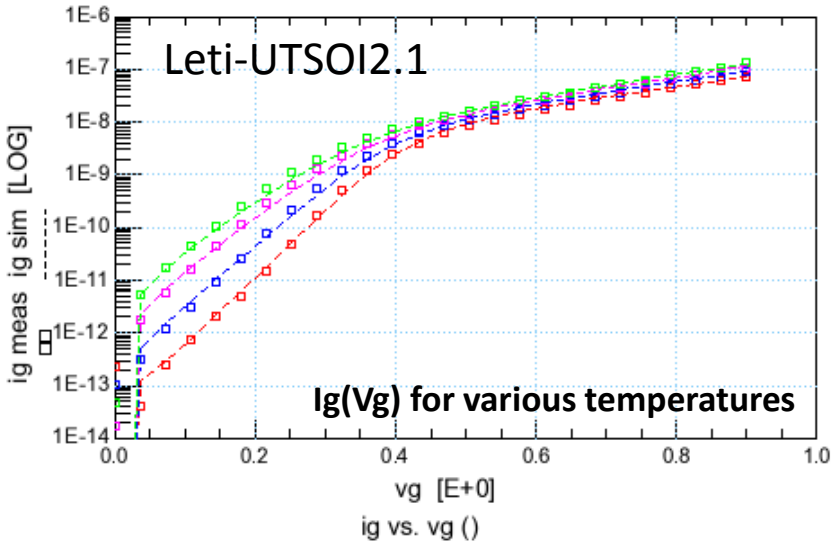
With L_{eff} dependence (Leti-UTSOI2.1)



Accuracy of gate current model

- Model completed to account for a TAT-like component of gate to channel current with a single new parameter NIGINV

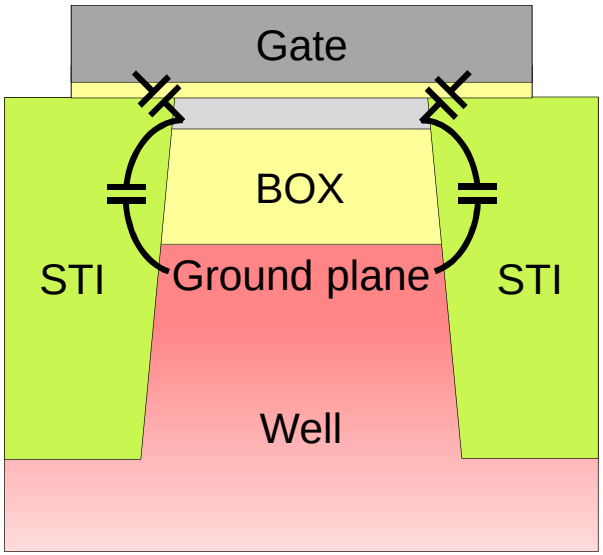


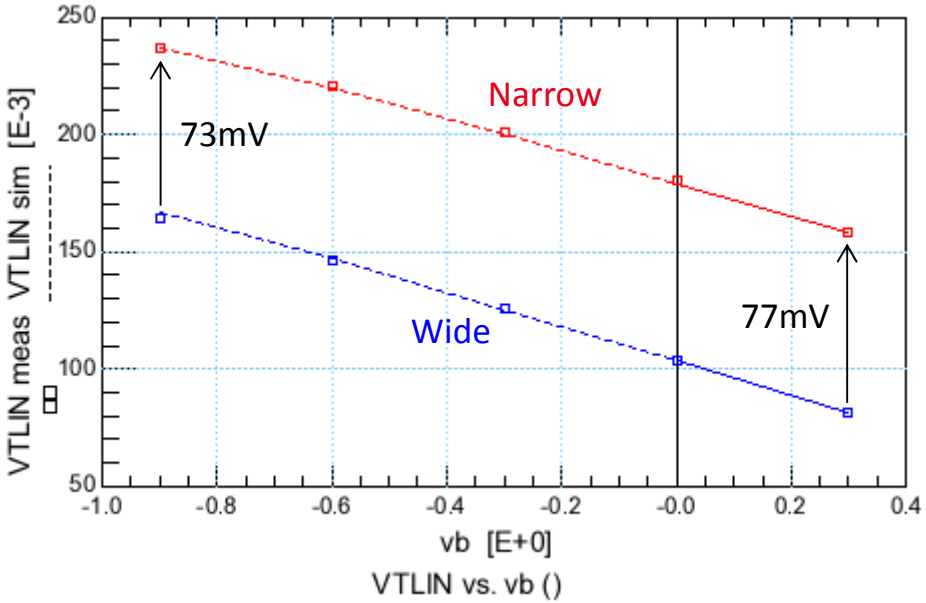


- Improved description in the subthreshold regime

Refined description of narrow channel effect

- Leti-UTSOI2.1 accounts for possible evolution of body factor with channel width through PNCE parameter
- Slight effect accurately captured





Other model improvements

- **Device thermal node is now accessible (optional 5th node)**
  - Possibility to connect external thermal RC network at circuit level
- **Mobility scaling law has been modified for more accuracy**
  - PSP-like scaling law adopted
- **Modified VFB scaling law**
  - Easier extraction of narrow channel effects

Summary

- **Improved version of Leti-UTSOI2 is available**
- **Main improvements concerns:**
  - Predictability of 2D electrostatic model over process parameters
  - Accuracy of weak/moderate inversion regime description
  - Accuracy of gate current modeling
  - Refined description of narrow channel effects
- **In addition, device thermal node is now available as an optional 5th node**

References about Leti-UTSOI2

T. Poiroux et al., "UTSOI2: A Complete Physical Compact Model for UTBB and Independent Double Gate MOSFETs", IEDM 2013

T. Poiroux et al., "UTSOI2: A compact model for UTBB devices accounting for back interface inversion", MOS-AK, dec 2013

New stress model for FDSOI technologies

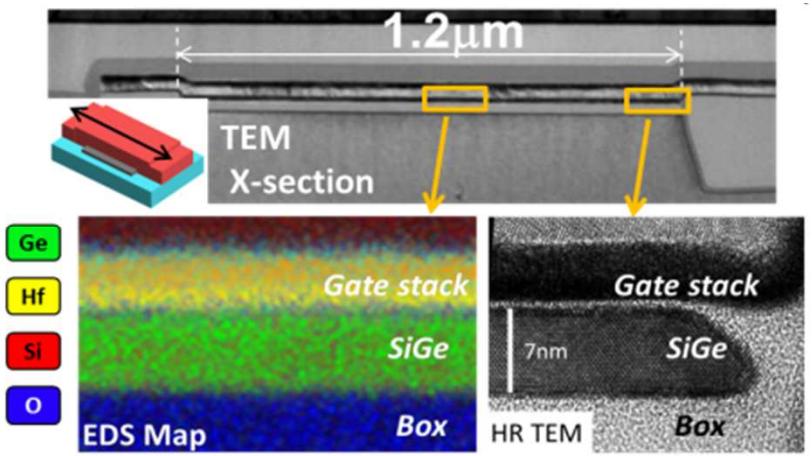
- Motivations
- Analytical model presentation
- Validation with respect to silicon data
- Summary

Motivations

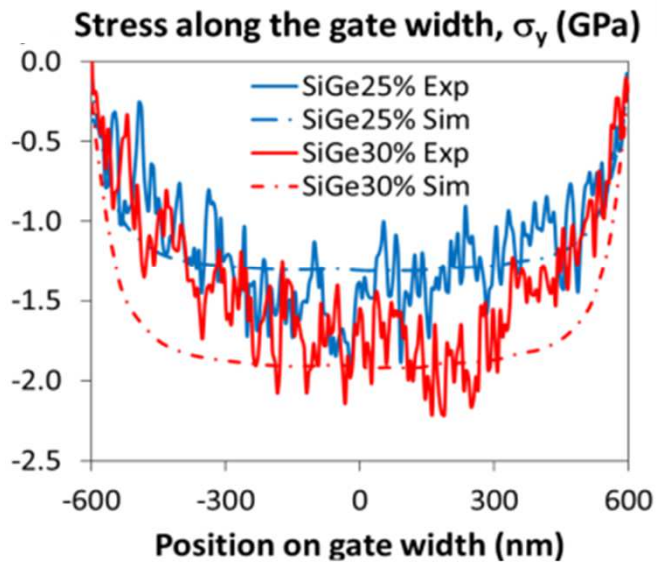
- Performance of next generation technologies increasingly rely on strain engineering
- Efficient usage of strained materials demonstrated in UTBB FDSOI 14nm [1]
- Supported by 3D mechanical simulations, quantum simulations and analytical model [2]
- For CAD offer, interest in using and adapting well-known SA/SB approach developed for STI stress [3] to capture geometry dependence of new stress effects

[1] O. Weber *et al.*, VSLI 2014
[2] B. De Salvo *et al.*, IEDM 2014
[3] R.A. Bianchi *et al.*, IEDM 2002

Case study: strain induced by SiGe channel



Courtesy from [1]

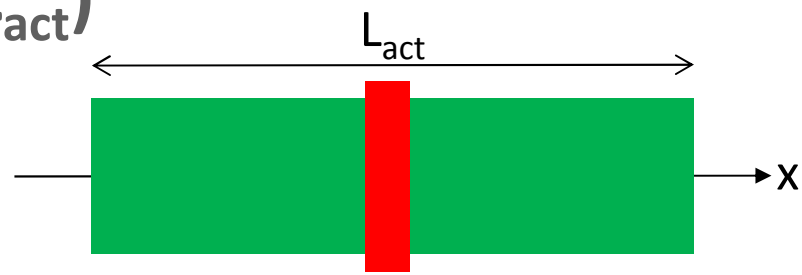


- **Ge induces compressive strain in SOI film**
- **Strain tends to relax at the edges of the film**

[1] B. De Salvo *et al.*, IEDM 2014

Model assumptions

- **Electrical parameters impacted by strain present an evolution along active area similar to that of longitudinal stress, captured by a relaxation factor $g(x,L_{act})$**



- **Impacted parameters are:**
  - Low field mobility (→ Iodlin, i.e. Ilin at Vgs-Vth=0.5V)
  - «Flat-band» voltage (→ Vtlin)
  - DIBL (→ Vtsat)
  - Saturation velocity (→ Isat, Ieff)

Model formulation using x and L_{act}

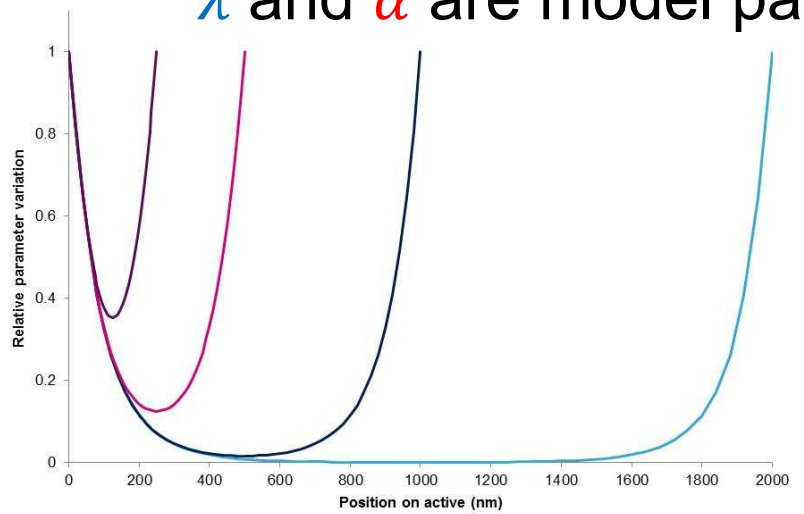
- **Evolution of electrical parameter P**

$$P(x, L_{act}) = P_{full\ strain} + \Delta P \times g(x, L_{act})$$

$\Delta P = P_{edge} - P_{full\ strain}$ can be a function of W, L

$$g(x, L_{act}) = 1 - \left[\frac{2}{(1 - e^{-x/\lambda})^{-\alpha} + (1 - e^{(x - L_{act})/\lambda})^{-\alpha}}\right]^{1/\alpha}$$

λ and α are model parameters



$g(x, L_{act})$ for $\lambda = 120nm$ and $\alpha = 3$

Model formulation using SA and SB

- **Parameter value is taken at the center of the channel:**

$$g(SA,SB) = 1 - \left[\frac{2}{(1-e^{-(SA+L/2)/\lambda})^{-\alpha} + (1-e^{-(SB+L/2)/\lambda})^{-\alpha}}\right]^{1/\alpha}$$

- **When SA=SB, relaxation factor reduces to:**

$$g(SA,SB=SA) = e^{-(SA+L/2)/\lambda}$$

- **This allows a simple parameter extraction**
  - λ (and ΔP) extraction on SA scaling with SA=SB
  - α extraction on SA or SB scaling with SA≠SB

Electrical parameter expressions with respect to SA_{ref}/SB_{ref} reference value

- **Ratio-like expression (e.g. mobility, saturation velocity)**

$$P(SA,SB) = P\left(SA_{ref},SB_{ref}\right)\frac{1+\left(\Delta P/P_{full\ strain}\right)g(SA,SB)}{1+\left(\Delta P/P_{full\ strain}\right)g\left(SA_{ref},SB_{ref}\right)}$$

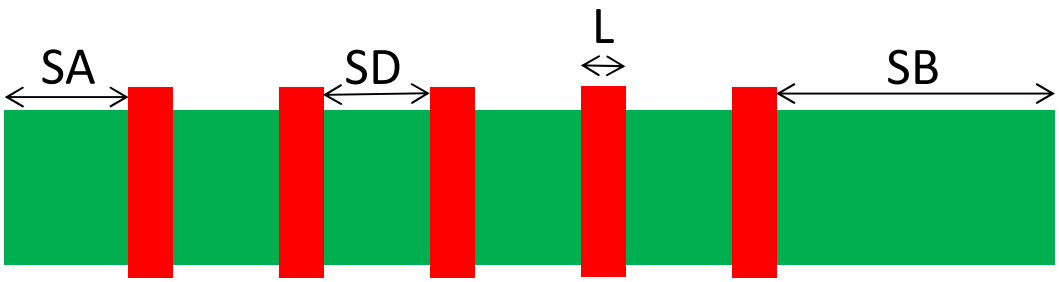
  - Amplitude parameter is $\Delta P/P_{full\ strain}$

- **Delta-like expression (e.g. Vth, DIBL)**

$$P(SA,SB) = P\left(SA_{ref},SB_{ref}\right) + \Delta P\left(g(SA,SB) - g\left(SA_{ref},SB_{ref}\right)\right)$$

  - Amplitude parameter is ΔP

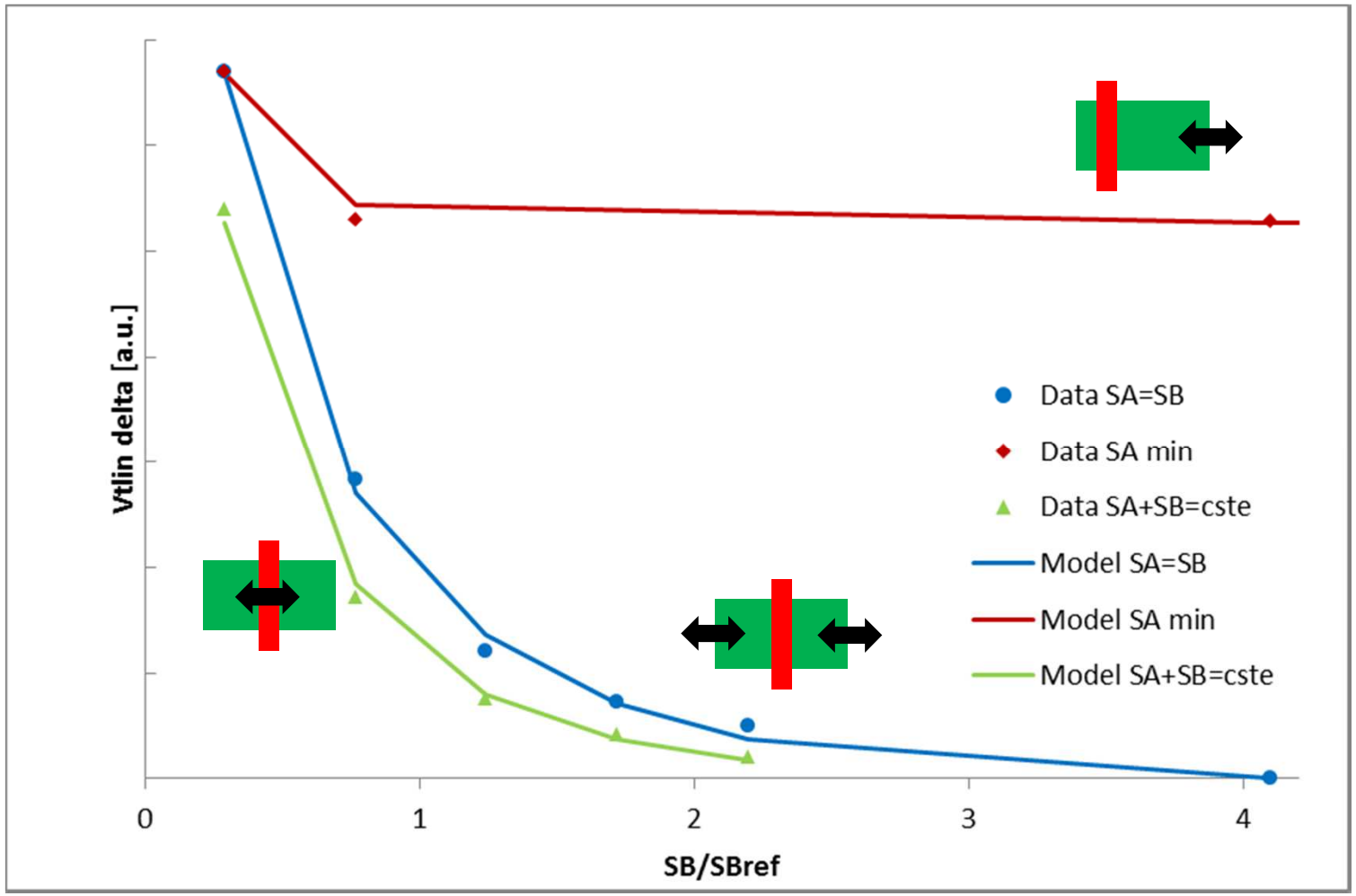
Model formulation for multi-finger devices (useful for pre-layout simulations)



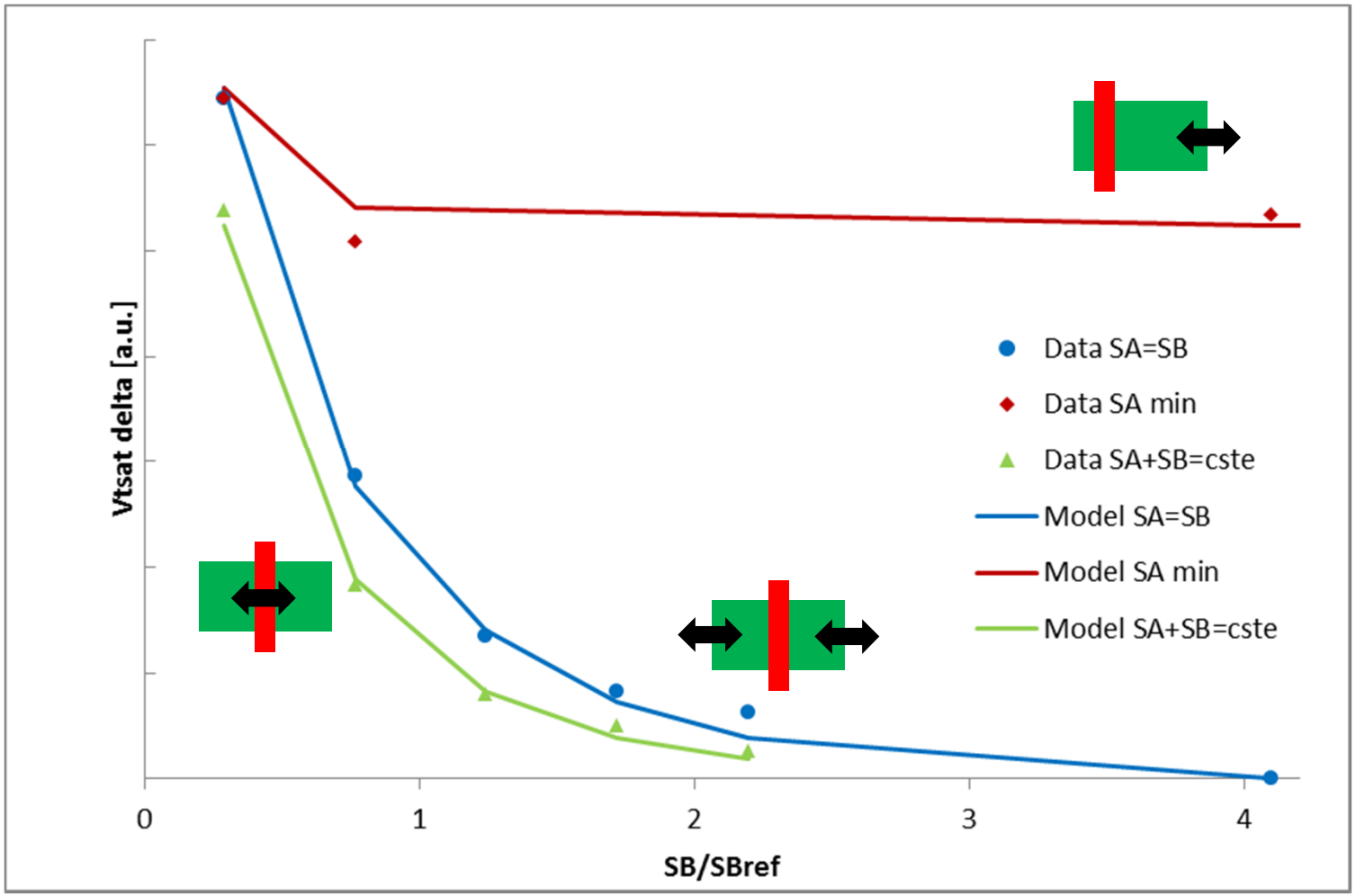
- **In previous model equations, relaxation factor, $g(SA, SB)$ is replaced by $\hat{g}(SA, SB)$**

$$\hat{g}(SA, SB) = \frac{1}{NF} \sum_{i=0}^{NF-1} g\big(SA + i(SD + L), SB + (NF - 1 - i)(SD + L)\big)$$

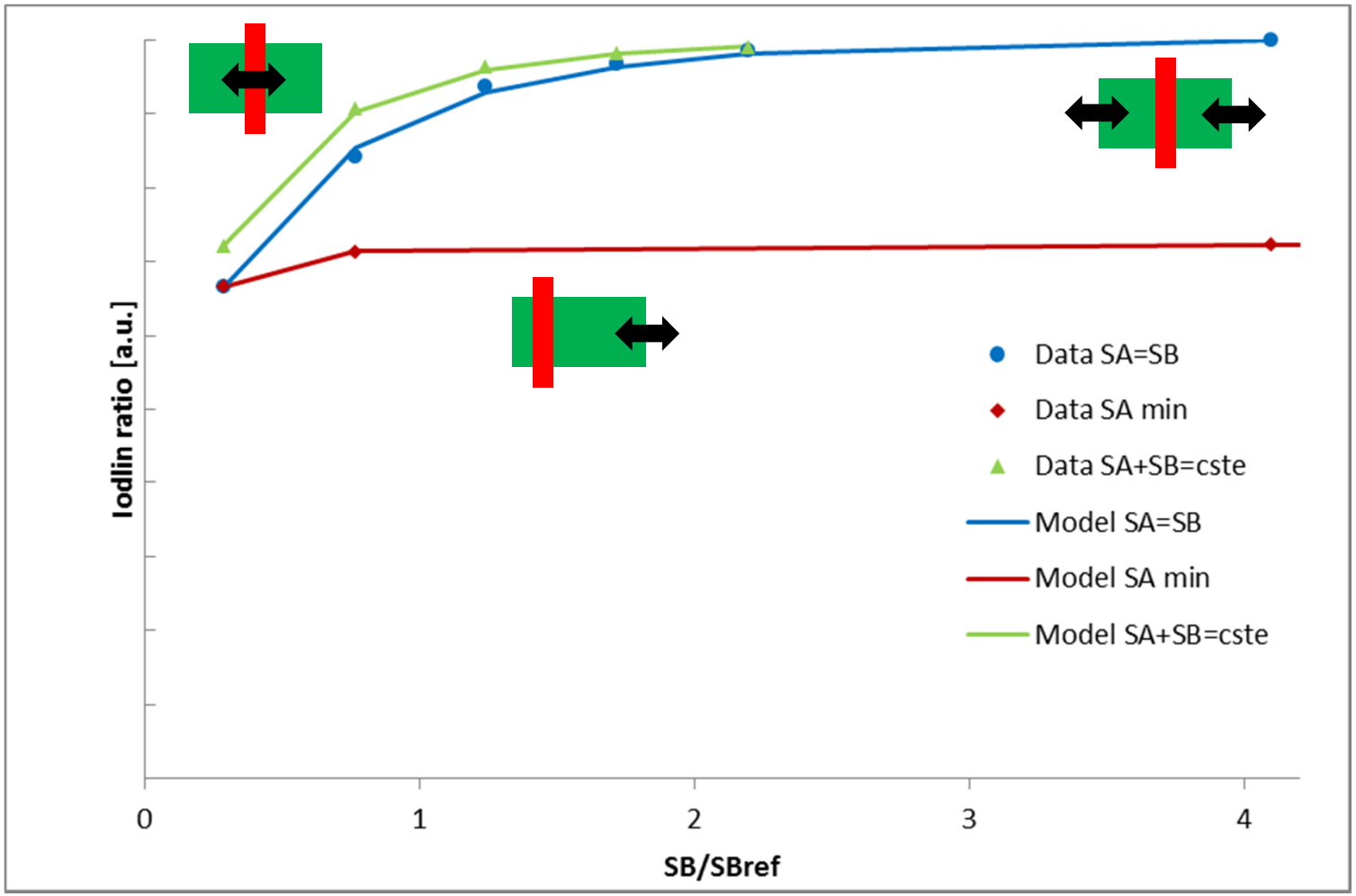
Experimental validation: Vtlin



Experimental validation: Vtsat



Experimental validation: Ilin @ Vgs-Vth=0.5V



Summary

- Stress model used in SPICE has to be updated to handle new strain engineering strategies of advanced technologies
- A new semi-empirical model is proposed, which is compatible with SA/SB formalism of initial stress model
- Model accuracy is validated against 14nm UTBB FDSOI silicon data
- This model will be implemented in Leti-UTSOI2 compact model, besides existing STI stress model (stress model selector will be added too)

References

- R.A. Bianchi *et al*., "Accurate Modeling of Trench Isolation Induced Mechanical Stress Effect on MOSFET Electrical Performance“, IEDM 2002
- O. Weber *et al*. , “14-nm FDSOI Platform Technology for High-Speed and Energy-Efficient Applications”, VLSI Technology Symposium 2014
- B. De Salvo *et al*., “A mobility enhancement strategy for sub-14nm power-efficient FDSOI technologies”, IEDM 2014

Thank you for your attention