Qucs-S and QucsStudio for Compact Device Modeling

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Presentation Topics

- Qucs-S and QucsStudio compact device modelling and simulation features
- QucsStudio and Qucs-S: a combined modelling and simulation package
- QucsStudio Verilog-A module development: facilities and properties
- Built in Verilog-A modules: CMC and others
- Equation-Defined Device (EDD) modelling: principles and application
- Qucs-S Verilog-A module synthesis: facilities and link to QucsStudio
- The Verilog-A Equation-Defined Device (VAEDD): structure and properties
- Enhanced QucsStudio compact device modelling and simulation
- Enhanced Qucs-S/Xyce behavioural EDD modelling
- Onwards to the next generation package
QucsStudio and Qucs-S

Back porting of Qucs-S code to Qucs is a long term goal but may take time due to the complexity of the software and investment required!

Release 0.0.1 2003
Release 1.0.0 2011
Release RC1 2015
Today

Qucs

NEW CODE

FORK

RF

QucsStudio

Qucs-S

SPICE

QucsStudio with Qucs-S provide advanced RF design, compact device modelling and simulation linked to industrial level Xyce SPICE circuit simulation "glued" together by behavioural compact device models and Verilog-A modules.

Linux and Windows compact device modelling and simulation package

Around 60% of the Qucs and Qucs-S downloads are for the Windows operating system.

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QucsStudio and Qucs-S

QucsStudio

- Equation-Defined Devices (EDD)
- Frequency Equation-Defined Devices (FEDD)
- Verilog-A Equation-Defined Devices (VAEDD) and Verilog-A hand coded modules

Compact Modelling

- Verilog-A synthesised modules
- CMC Verilog-A modules: BSIM6 and HICUM2, for example

Qucs-S

- XYCE script
  - XYCESCR1
  - SpiceCode=
    - AC LIN 2000 100 10MEG
    - PRINT AC format=raw file=ac.txt V(1)
- INCLUDE SCRIPT
  - INCLSCR1
  - SpiceCode=
    - PARAM rp = 1k
    - FUNC prod(x,y) = \{x*y\}

GUI

QucsStudio SIMULATION

DC, AC, S-parameter, and NOISE, TRAN and periodic steady-state, HB with large-signal AC and NOISE analysis, System simulation, Parameter sweep, optimization, tolerance analysis and manual tuning with sliders.

XYce SIMULATION

DC, AC, DATA, DC, DCVOLT, EMBEDDED_SAMPLING, END, ENDS, FOUR, FUNC, GLOBAL, HB, IC, INC (or .INCLUDE), LIB, LIN, MEASURE (or .MEAS), MODEL, NODESET, NOISE, .OP, OPTIONS, .PARAM, .PREPROCESS, .PRINT, .RESULT, .SAMPLING, .SAVE, .SENS, .STEP, SUBCKT, TRAN.
Synthesize Verilog-A Module Code [with ADMS] To form “Transistor.va.cpp” and Compile C++ code to form “Transistor.dll”

“Turn-Key” system

Edit Verilog-A module code

Click to display generated C++ code

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Verilog-A Development

Add pins PC, PB and PE. Draw model symbol.

Pass symbol parameter values to “user compiled model” via name = name construction.

Drag and drop “transistor.va”
Built in Verilog-A modules

Windows “turn key” ADMS Verilog-A module development system

QucsStudio
Standard SPICE models: Diode, BJT, MOSFET, JFET and MESFET

CMC and other models:
BJT – HICUM/L2/L0
MOSFET – EKV2.6

The Windows serial (single processor) version of Xyce is compiled under Cygwin64 using static libraries. Hence, a “turn key” Verilog-A module development system is NOT implemented.

Qucs-S/Xyce
Standard SPICE models: Diode, BJT, MOSFET, JFET and MESFET

CMC and other models:
BJT – VBIC 1.3, FBH HBT_X, HICUML0/L2, MEXTRAM
MOSFET – BSIM3, BSIM4, BSIM6, BSIM_SOI, BSIM_CMG, MVS, PSP

Verilog-A ADMS generated models

CMC = Compact Modelling Coalition
QucsStudio: 8 two port terminals max.

Qucs-S: 20 two port terminals max.

\[ I = I(V), \quad g = \frac{dl}{dV} \]
\[ Q = Q(V,I), \quad C = \frac{dQ}{dV} = \frac{\partial Q(V)}{\partial V} + \frac{\partial Q(I)}{\partial I} \cdot g, \text{ where} \]
the current flowing in branch n is \( I_n = I(V_n) + \frac{d}{dt}(Q_n) \), and 1 \( \leq \) n \( \leq \) 20.

- EDD is a multiterminal nonlinear component with branch currents that can be functions of EDD branch voltage, and stored charge that can be a function of both EDD branch voltages and currents
- EDD is similar, but more advanced to the SPICE 3f5 B type I or V controlled sources
- EDD can be combined with conventional circuit components and Qucs-S equation blocks when constructing compact device models and subcircuit macromodels
- EDD is an advanced component, allowing users to construct prototype experimental models from a set of equations derived from physical device properties
- EDD operator \( \frac{d}{dt} \) is undertaken internally by Qucs-S
- Qucs-S EDD can have a maximum of 20 two terminal branches
Equation-Defined Devices

1. \( VG' = VGDash = VG \cdot VTO + \Phi + \beta \cdot \sqrt{\Phi} \)
2. \( VP = \Phi \cdot \gamma \cdot \sqrt{\frac{VG'}{\gamma^2} - \gamma V2} \)
3. \( BETA = (KP \cdot WL) \cdot \frac{1}{(1.0 + \Phi \cdot VP)} \)
4. \( N = 1.0 + \gamma(2.0 \cdot \sqrt{VP + B + 4.0 \cdot VTO}) \)
5. \( IF = \ln(1.0 + \ln exp(X1)) + \ln(1.0 + \ln exp(X2)) \)
   \[ IR = \ln(1.0 + \ln exp(X2)) + \ln(1.0 + \ln exp(X2)) \]
   \[ X1 = (VP-VS) \cdot VVT, X2 = (VP-VD) \cdot VVT \]
6. \( DS = 2.0 \cdot N \cdot \beta \cdot VT^2 \) (IF-IR)

EKV 2.6 long channel static I/V model equations

EKV 2.6 intrinsic long channel model symbol
EKV 2.6 Id/Vd Example
EKV 2.6 Example-dynamic charge

**Parameter simulation**
- SP1
  - Type=list
  - Points=100e6

**Parameter sweep**
- SW
  - Type=lin
  - Start=2
  - Stop=81

**Equation**
- Eqn1
  - y=ystory()
  - W=20e-6
  - L=10e-6
  - COX=3.5e-3
  - Omega=2*pi*frequency
  - Cap=imag[y(1,1)]/Omega
  - C_parallel_plate=W*L*COX
  - C_ratio=Cap/C_parallel_plate

**Results**
- Voltage vs. Current for various parameters:
  - Vgs (V) vs. Cap (F)
  - Vgs (V) vs. C_ratio

**Table**

<table>
<thead>
<tr>
<th>number</th>
<th>C_parallel_plate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7e-13</td>
</tr>
</tbody>
</table>

Matthias Bucher et al., The EPFL-EKV MOSFET Model Equations for Simulation, Technical Report, Model Version 2.6, June 1997,

Electronics Laboratories, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland.
EKV 2.6 intrinsic and extrinsic models

Intrinsic part of EKV 2.6 model

Extrinsic part of EKV 2.6 model

Typical example diode parameters

$\begin{align*}
\text{Is} &= 1\text{e-15 A} \\
\text{N} &= 1 \\
\text{Cj0} &= 10 \text{ fF} \\
\text{M} &= 0.5 \\
\text{Vj} &= 0.7 \text{ V} \\
\text{Fv} &= 0.5 \\
\text{Rs} &= 1.0
\end{align*}$

$\begin{align*}
\text{C1} &= \text{CGB} \\
\text{C2} &= \text{CGS} \\
\text{C3} &= \text{CGD}
\end{align*}$

$\begin{align*}
\text{X4} &= \text{W} = 80\text{e-6} \\
\text{L} &= 8\text{e-6} \\
\text{VTO} &= 1.0 \\
\text{Cgb} &= 0.01p \\
\text{Cgd} &= 0.01p \\
\text{Cgs} &= 0.01p \\
\text{COX} &= 3.45e-3 \\
\text{TNOM} &= 26.58 \\
\text{TEMP} &= 26.58 \\
\text{KP} &= 30\text{e-6} \\
\text{PHI} &= 0.5 \\
\text{HDIF} &= 0.9\text{e-6} \\
\text{RSH} &= 510 \\
\text{GAMMA} &= 0.7 \\
\text{AF} &= 1.0 \\
\text{KF} &= 1.\text{e-27}
\end{align*}$
Qucs-0.0.22-S includes a GPL Verilog-A synthesis tool for compact device modeling.

- The Verilog-A synthesizer is a fully working version of this open source ECAD tool,
- Verilog-A device/subcircuit models can be synthesized from the following built in components:
Verilog-A module synthesis
Verilog-A module synthesis

Internal nodes - two I(xx) <+ … contributions per EDD equation

External nodes - one I(yy) <+ … contribution per node pair.
Verilog-A module synthesis

Only one $I(\text{yy}) <+ ...$ contribution per external node pair

Dynamic charge currents

Static current $I(n_D,n_S)$
Simulation of complex EDD compact models can be very slow.

Constructing complex Verilog-A models often requires considerable time and effort.

Introduce a compromise: construct a compact device model from a mixture of EDD blocks and very simple Verilog-A modules where each Verilog-A module models at most two or three EDD equations.

These simplified Verilog-A blocks are called Verilog-A Equation-Defined devices or VAEDD.
One or more VAEDD blocks can be mixed with EDD to construct a compact device model.

VAEDD Example

EKV2.6 : Vgdash VP BETA

include "disciplines.vams"
include "constants.vams"
module VAEDDnDash(n2p, n2n, n1p, n1n);
input n2p, n2n, n1p, n1n;
electrical n2p, n2n, n1p, n1n;
parameter real VTO = 0.5;
parameter real PHI = 0.5;
parameter real GAMMA = 0.7;
branch (n2p, n2n) B1;
branch (n1p, n1n) B2;
begin
  analog begin
    i(B1) = V(V1)*1e-9;
    i(B2) = V(V1)+VTO+PHI+GAMMA*sqrt(PI(1e-10));
  end
endmodule

include "disciplines.vams"
include "constants.vams"
module VAEDDnBeta(n1p, n1n, n2p, n2n);
input n1p, n1n, n2p, n2n;
electrical n1p, n1n, n2p, n2n;
parameter real VTO = 0.5;
parameter real PHI = 0.5;
parameter real GAMMA = 0.7;
real GAMMA2;
branch (n2p, n2n) B1;
branch (n1p, n1n) B2;
begin
  analog begin
    GAMMA2=GAMMA/2;
    i(B1) = V(V1)*1e-9;
    if (V(V1) > 0.6) begin
      i(B2) = i(B1)+PHI+GAMMA*sqrt(PI)+GAMMA2;
      GAMMA2=GAMMA/2;
    end else begin
      i(B2) = -PHI;
    end
  end
endmodule

QucsStudio 3.3.2 was released on the 15 July 2020 two years after version 2.5.7.

**New features: NOT in any specific order**

- EM field simulation using openEMS,
- New diagram: equation,
- HICUM L0 model implemented,
- Improved random-number generation,
- Smith chart: enable impedance and admittance circles,
- New document type: PCB layout,
- Differentiate name.i and name.v in simulator equations,
- Complex source and load impedance possible in matching dialogue.

**Plus others and many bug fixes**
- This package has reached an advanced stage of development in that it offers an almost complete set of circuit simulation routines covering the d.c. to transient domains with significant additions beyond SPICE 3f5, like multi-tone Harmonic Balance analysis, Monte Carlo analysis, parameter sweep, multi-port S parameter and noise simulation, optimization and system simulation.

- Full "turn-key" Verilog-A compact modelling is also offered via the ADMS software.

- In terms of development QucsStudio is particularly interesting in that it is the first of the Qucs series of circuit simulators to introduce interactive animation as a tool for advanced circuit simulation.

- QucsStudio allows one or more parameter values to be simultaneously controlled by sliders.

- With the computational power of a modern PC changes in simulation output data can be observed as movements in plotted curves as the sliders are moved.
Enhanced QucsStudio features

Measurements: Digilent “Analog Discovery 2” [16]

R and C Parameter tuning

Synthesized simulation a.c. control icon and measured data icons

Measured data and simulation output visualization

A simple RC low pass passive filter example showing an advanced test bench schematic with a computer controlled transfer function measurement system where the measured output data is converted from CSV format to Qucs simulation control icons.

Enhanced QucsStudio features
Three parameter optimization (Bf, Is, Vaf) with parallel IC/Vce BJT test bench using a single Vce parameter sweep and (1) Ib=200u, PricM measured Ic data and (2) Ib= 400u, Pric1M measured Ic data.
Enhanced QucsStudio features

EM field simulation using openEMS: 1.5 GHz bandpass filter (imported from HyperLynx file by Koen De Vleeschauwer). Example developed by Dr M. Margraf as part of the Qucs-Studio 3.3.2 release.
Xyce 7.1 was released on 8 June 2020.

**New features: NOT in any specific order**

- Non-linear solution dependent capacitors
  Cap1 1 2 q = \{ca*(c1*v1*ln(cosh((v(1,2)-v0)/v1)+c0*v(1,2))}, or
  Cap1 1 2 c = \{ca*(c0+c1*tanh((v(1,2)-v0)/v1))}, where both forms are implemented to ensure charge conservation,

- C-style ternary conditional operator,

- .LIN transfer analysis and extraction of S, Y and Z parameters from a general multiport network,

- .SAMPLING: calculates a full analysis (.DC, .TRAN, .AC etc.) over a distribution of parameter values,

- Sweep loops can now use .DATA command

**Plus others and many bug fixes**
Adding new Xyce features to Qucs-S.

- These Xyce specific icons allow new features to be placed on a circuit schematic and interpreted during simulation.

- Qucs-S has in fact a two level GUI system; items common to SPICE 3f5, and other equivalent simulators, operate via built-in Icons or a XYCE script, while the less used or recently added features, can only be accessed via a XYCE script.

- For example, since 2018 approximately 20 important additions to Xyce functionality have been implemented, including Monte Carlo analysis and Lattice Hypercube sampling via a new .SAMPLING feature, transient simulation direct sensitivity analysis that supports .FOUR, .LIN for S parameter multiport analysis with Y and Z output data in Touchstone level 1 and level 2 format, and a new charge expression variant for capacitors that is similar to the EDD branch charge implementation.
A Xyce SPICE style tunnel diode compact model with a test bench for investigating the effects of stepped device parameters.
Enhanced Qucs-S/Xyce features

Much improved SPICE style behavioral modelling facilities
Enhanced Qucs-S/Xyce features

Ids versus Vds output characteristics generated by .DC scan using parallel test circuits with fixed values of Vgs
Future Qucs-S/Xyce changes

- Xyce 7.0/7.1 and beyond: Improved mixed-signal interface via the Verilog Procedural Interface (VPI); Increased Verilog-A simulation speeds; bug fixes (.MEASURE, .AC etc); Improved simulation data output. Current and future Verilog-A developments: Xyce/ADMS compiler modified to use analytic derivatives, new Xyce XML templates. Possible future Verilog-A additions – full implementation of ddx function and a new non-ADMS-based model compiler !.

- Tighter linking between QucsStudio/Qucs-S, Verilog-A/Xyce and device/circuit parameter measurements via an Octave “Toolkit”.

- Introduction of multi-physics modelling via links to OPENMODELLICA: simulation of real world systems built from non-electrical and electrical components.
Low-cost high-performance PC engineering workstations have encouraged the development of compact device modelling and circuit simulation tools centered on a high-resolution graphics interface for schematic drawing, simulation control and output data visualization. This presentation outlined the capabilities of the Qucs/Qucs-S and QucsStudio series of circuit simulators and modelling tools.

These tools allow interactive prototyping of compact device models and their testing using Qucs/QucsStudio and Qucs-S as a central platform in the construction of Verilog-A modules and Equation-Defined Device models.

Each of these, when coupled with established, or new compact modeling techniques like mixed Equation-Defined Device and Verilog-A models (VAEDD), make the current software a highly flexible and innovative platform for compact modeling and circuit simulation.

Future improvements to the Qucs software indicate that by merging device parameter measurements with circuit simulation for device parameter extraction, and the introduction of EM field simulation with openEMS will significantly extend the scope of traditional circuit simulation.
References


Software sources


- **QucsStudio** - Download Windows version QucsStudio-3.3.2.zip from [http://www.dd6um.darc.de/QucsStudio/download.html](http://www.dd6um.darc.de/QucsStudio/download.html).

- **Qucs-S (Qucs with SPICE)** - Download – version (Linux or Windows) as required from home page [https://ra3xdh.github.io/](https://ra3xdh.github.io/).