Latest developments of L-UTSOI: A compact model dedicated to low-power analog and digital applications in FDSOI technologies

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Outline

- Status of L-UTSOI

- Recent mayor development in L-UTSOI
  - Gm/Id improvement
  - Impact ionization evidence and modeling
  - Accurate model for overlap gate current

- L-UTSOI model extraction using 28NM FDSOI technology

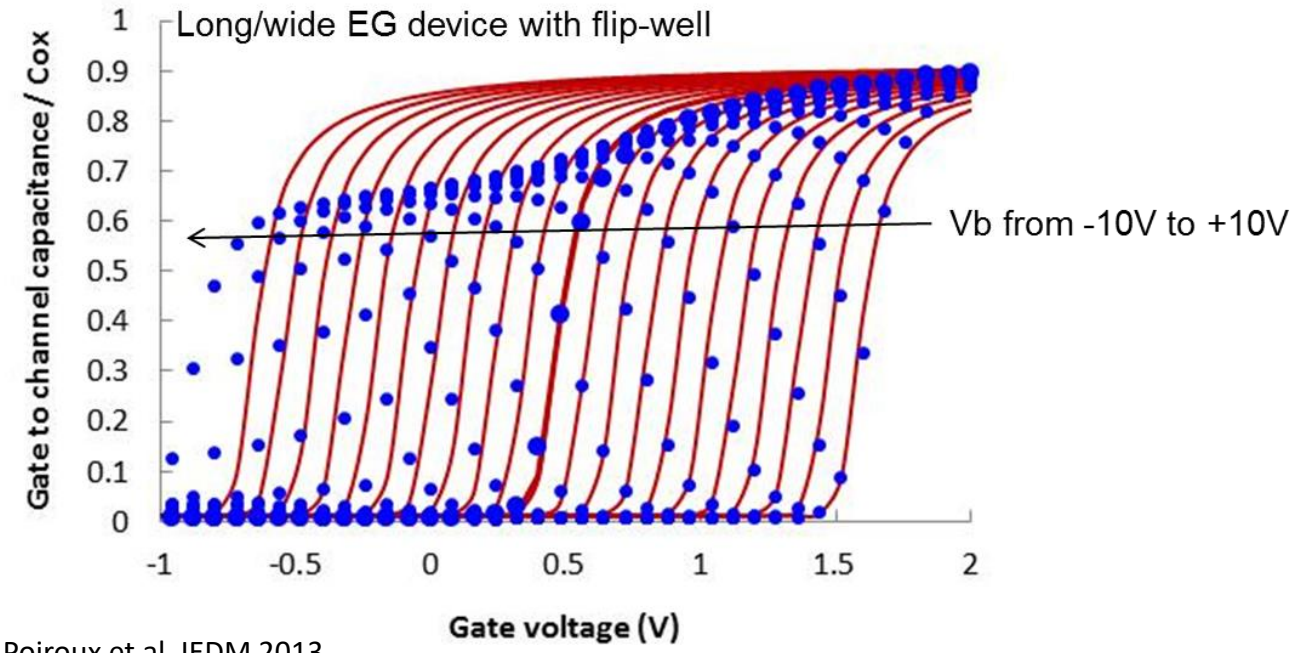
- Conclusions/perspectives

INTRODUCTION:
STRONG FORWARD BACK BIAS MANDATORY FOR FDSOI

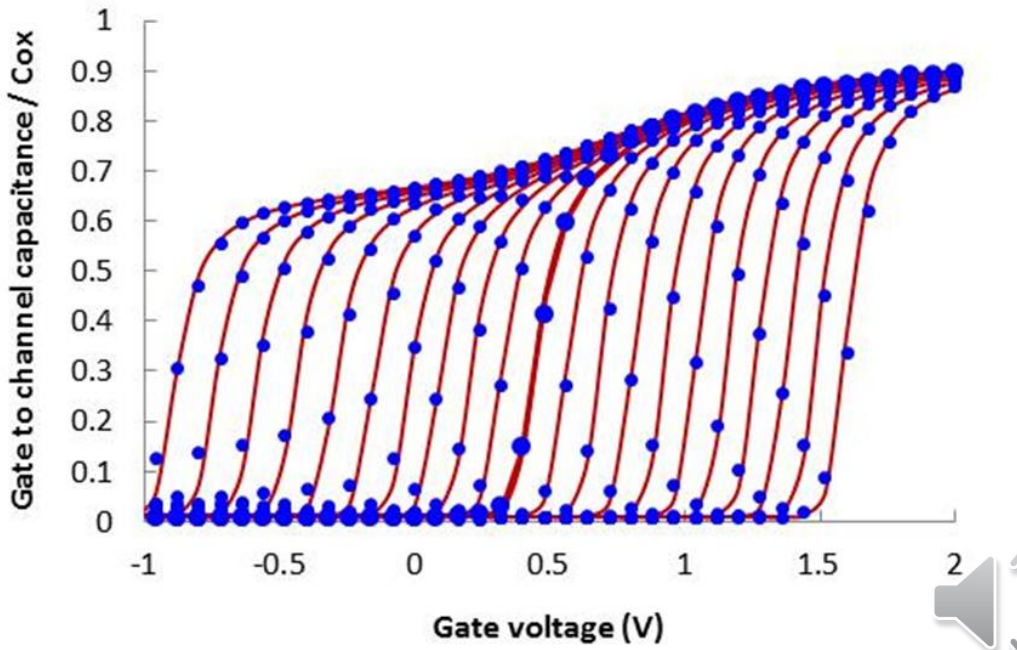
- **L-UTSOI is the first compact model able to describe FDSOI transistor behavior in all bias configurations, including strong forward back bias.**
- **But a model ignoring the formation of a strong inversion layer at the back interface lacks of accuracy in transistor electrostatics description**
  - **even at null back-bias in case of flip-well devices**
  - **inaccuracy gets worse as back-bias goes forward**
  - **inaccuracy not only on C(V) but also on Gm**

➢**To be considered as a mandatory requirement for FDSOI technologies**

Without back gate induced inversion layer



With back gate induced inversion layer



[1] T. Poiroux et al, IEDM 2013.

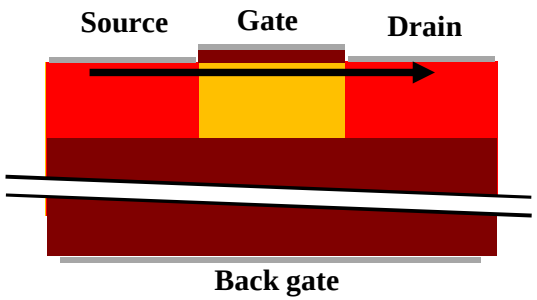
INTRODUCTION:
BRIEF MODEL HISTORY

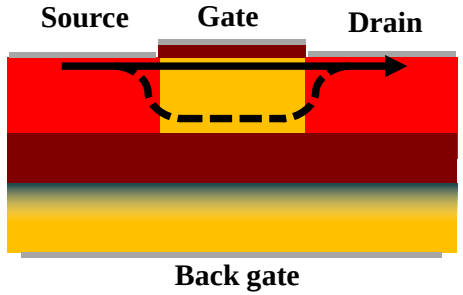
- From 2013, the need to consider FDSOI transistor as a true independent double gate transistor, with possible conduction at both thin body interfaces, is fulfilled by Leti-UTSOI 2.x.x versions.
- Since 2013, the model has been further improved, based on industrial partner needs.
- Since 2020 L-UTSOI is a standard model.

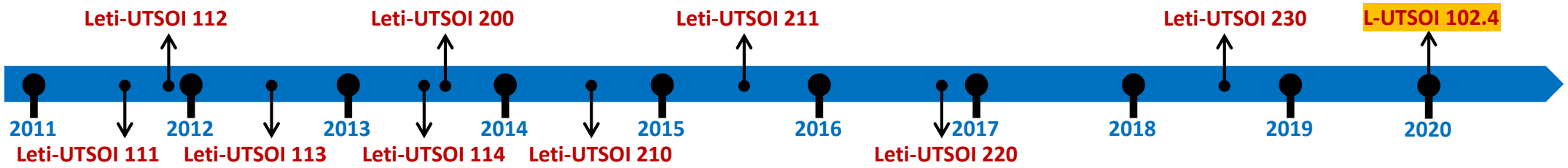
Leti-UTSOI 1.x.x
Back interface assumed depleted/weakly inverted

Leti-UTSOI 2.x.x
No assumption on back interface regime

L-UTSOI
New model name within CMC







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GM/ID IMPROVEMENT: INTRODUCTION OF EFFECTIVE DOPING

Starting from the surface potential accounting for SCE [1]:

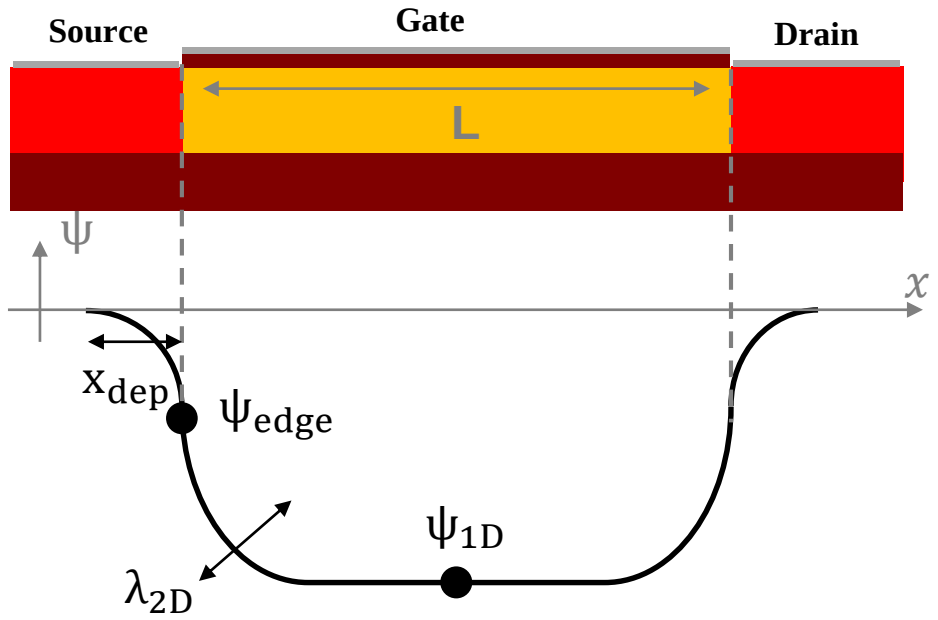
$$\psi_{2D(x)} = \psi_{1D} + (\psi_{edge} - \psi_{1D})e^{-x/\lambda_{2D}} + (\psi_{edge} - \psi_{1D})e^{-(L-x)/\lambda_{2D}}$$

In the depleted S/D region, we simplify the 2D Poisson's equation by considering that a fraction of the depletion charge α acts on the longitudinal electric field:

$$\begin{cases} E_{x,edge} = \pm(\psi_{edge} - \psi_{1D})/\lambda_{2D} \\ \varepsilon_{Si} E_{x,edge} = q\alpha N_{sd} x_{dep} \\ \psi_{electrode} - \psi_{edge} = E_{x,edge} x_{dep}/2 \end{cases}$$

$$\psi_{edge} = \psi_{1D} + \psi_{dep}\left[\sqrt{1 + 2(\psi_{electrode} - \psi_{1D})/\psi_{dep}} - 1\right]$$

$$\psi_{dep} = q\alpha N_{SD}\lambda_{2D}{}^2/\varepsilon_{Si}$$

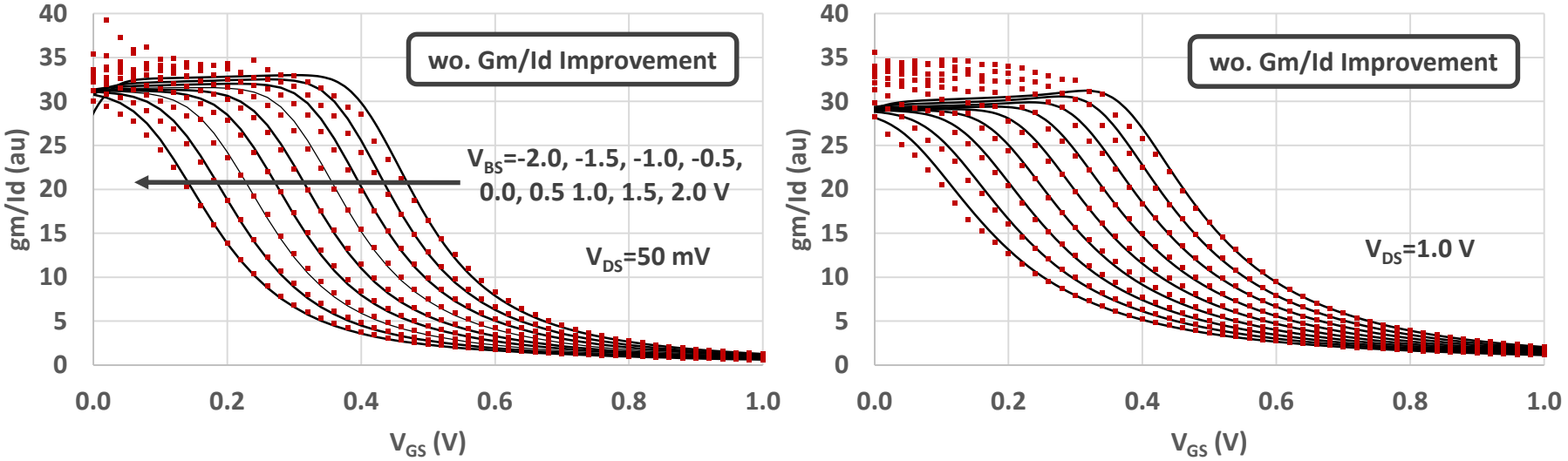


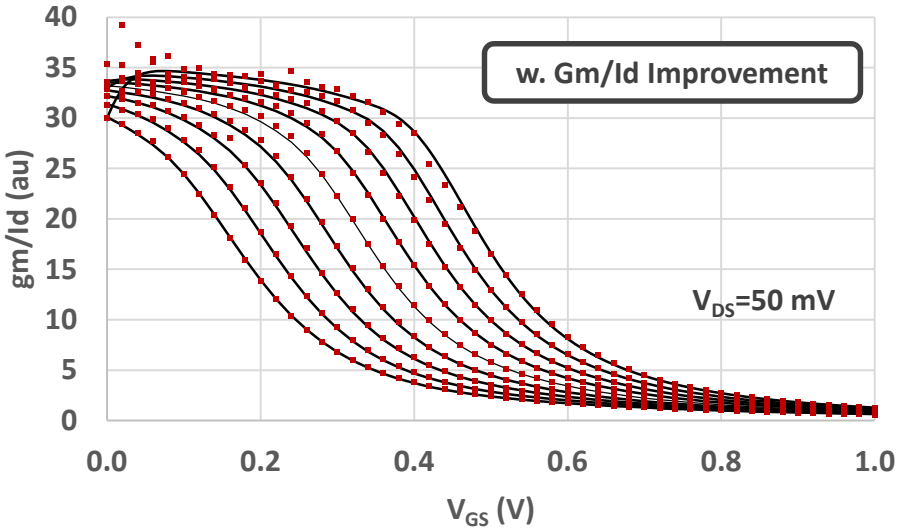
where ψ_{1D} is a smooth minimum function between the long channel surface potential at the center and its threshold value (to extend the validity in moderate inversion) & λ_{2D} is the bi-dimensional characteristic length of the device

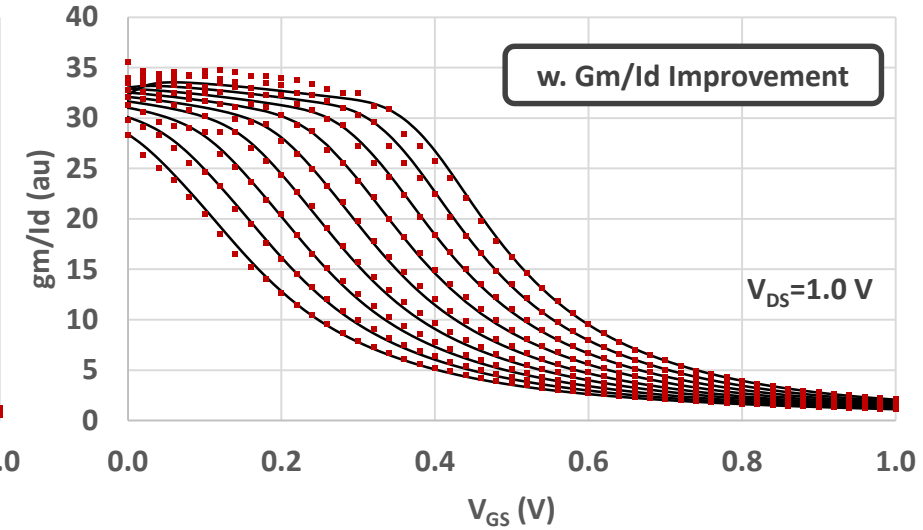
This effective doping αN_{SD} is the model parameter to modulate the source/drain depletion. (implementation is detailed in the user's manual [2])

[1] K.K. Young, TED 1989, [2] L-UTSOI 102.4.0 user's manual.

GM/ID IMPROVEMENT: MODEL VS EXPERIMENT







Short channel on thin front oxide device @ 25°C

An accurate description of gm/Id is achieved thanks to implementation of S/D depletion

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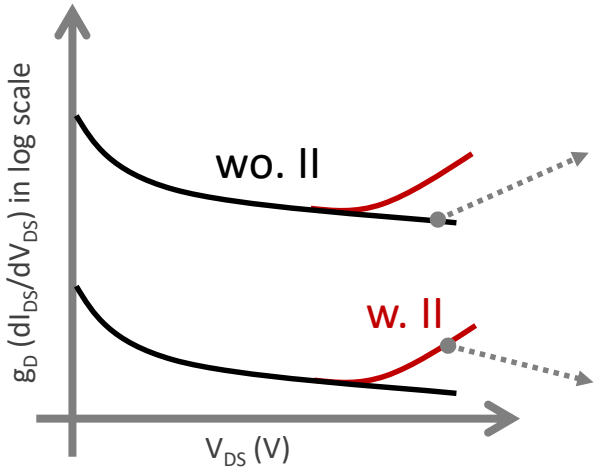
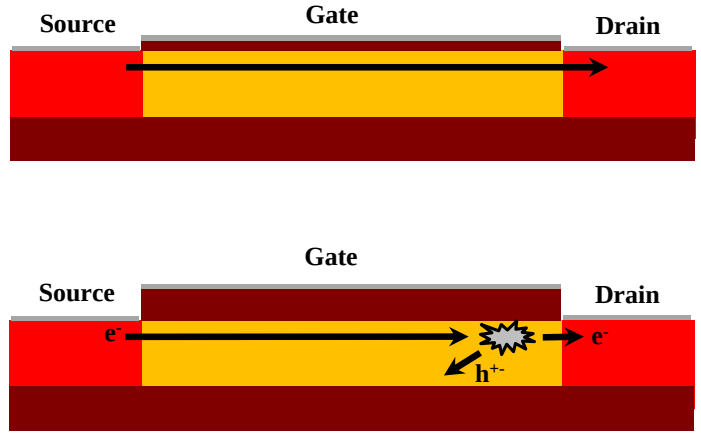
IMPACT IONIZATION EVIDENCE AND MODELING: PHYSICAL FOUNDATION

In FDSOI transistor, Impact ionization is more significant for thicker oxide transistors, featuring higher supply voltages, and only weak avalanche occurs.

This small impact ionization component increases source/drain current (in opposition to bulk MOSFET where impact ionization results in a bulk/drain current).





Inclusion of this model in term of physics and code implantation is close to that of PSP model [1]. For low-level avalanche multiplication, the avalanche current is [2]:

$$I_{aval} = I_{DS}.\int_0^L \alpha_n.dx \sim A1.\Delta V_{sat}.I_{DS}.e^{-\frac{a_2}{\Delta V_{sat}}}$$

$$\begin{cases} \Delta V_{sat} = V_{DS} - A3.V_{DSsat} \\ a_2 = A2.(T_{KC}/T_{KR})^{STA2} \end{cases}$$

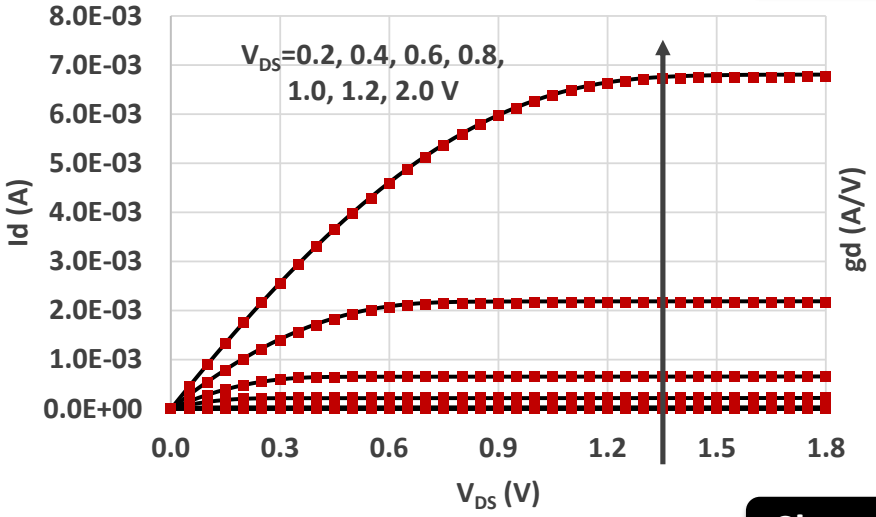
where A1, A2, A3 and STA2 are related parameters

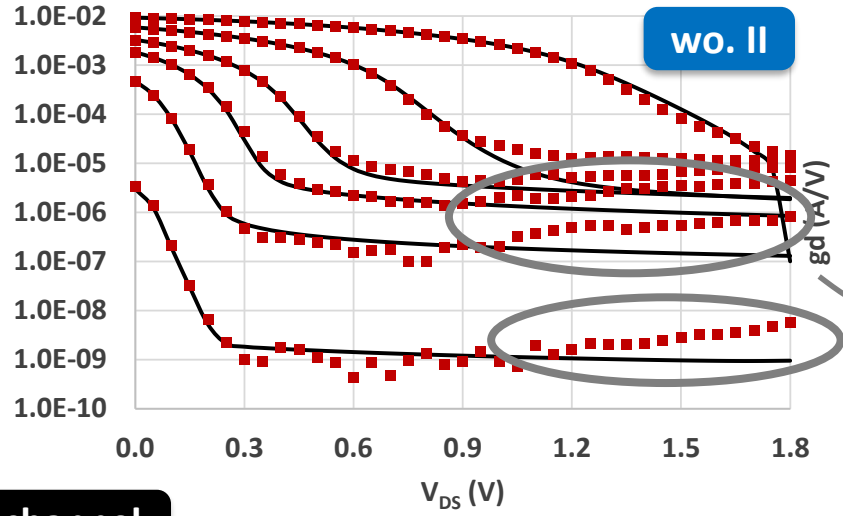
[1] PSP 103.6 Verilog-A and documentation; [2] R. van Langevelde et al Physical Background of MOS Model 11, Level 1101, 2003

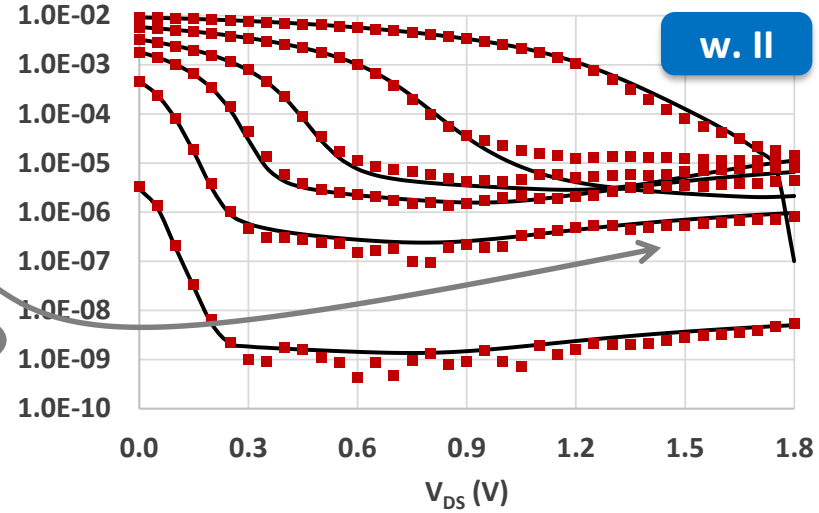
IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT

Negative gm is the consequence of SHE

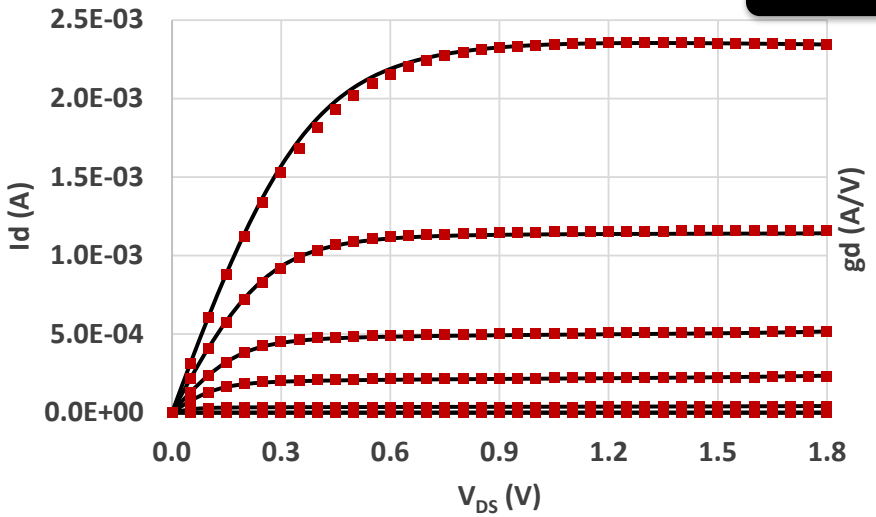
Long channel

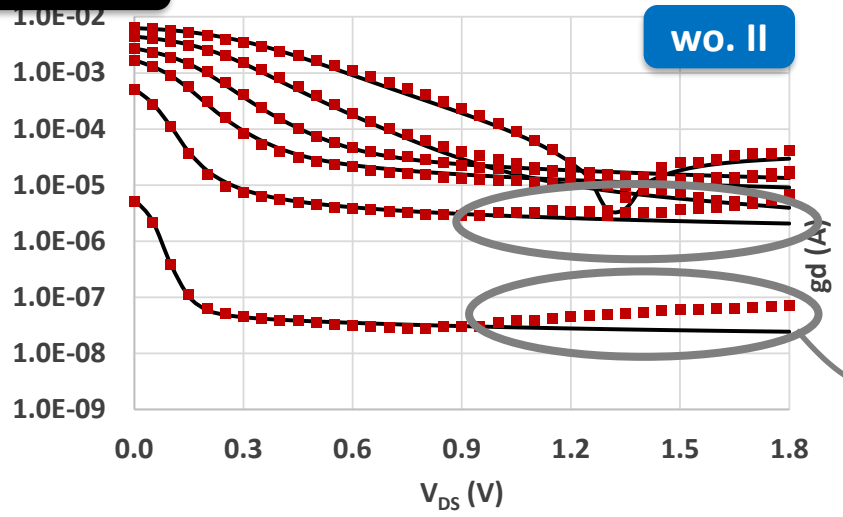


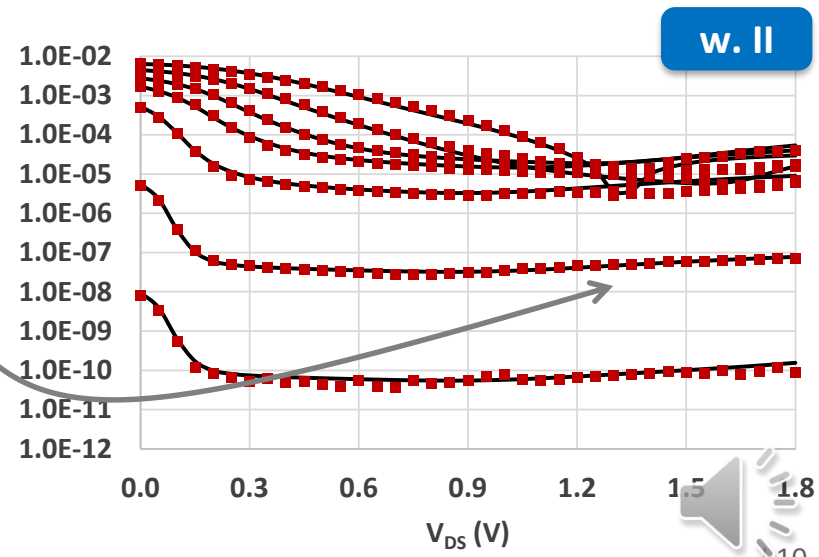




Short channel

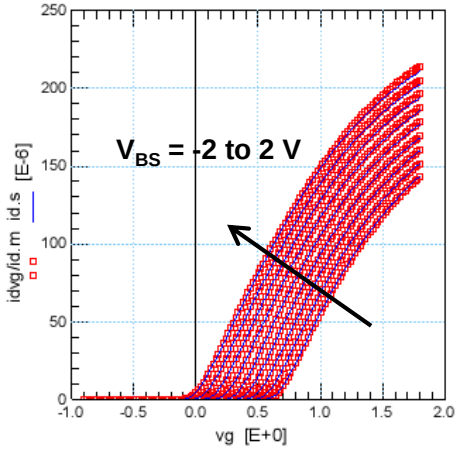




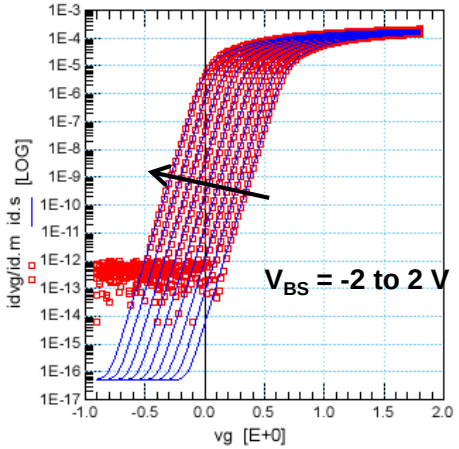


IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT

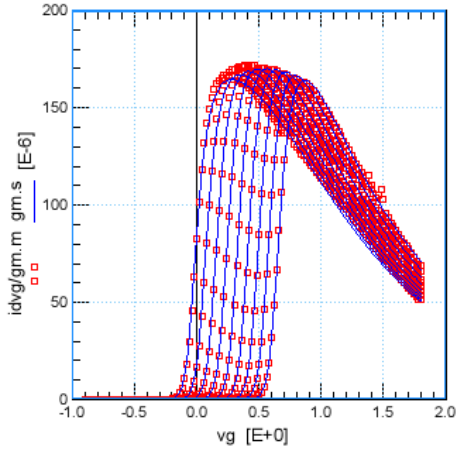
I_D-V_{GS} (lin scale)



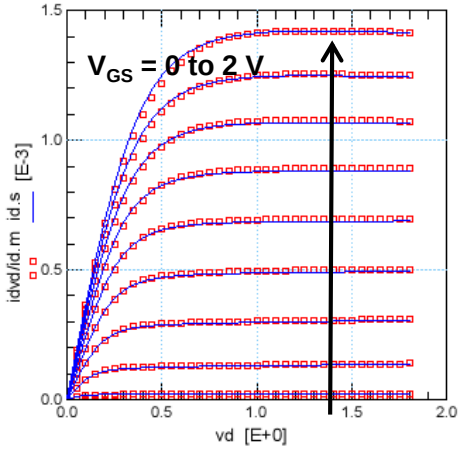
I_D-V_{GS} (log scale)



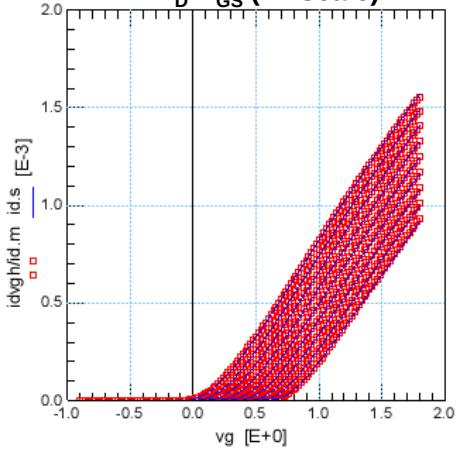
g_{mlin}-V_{GS} (lin scale)



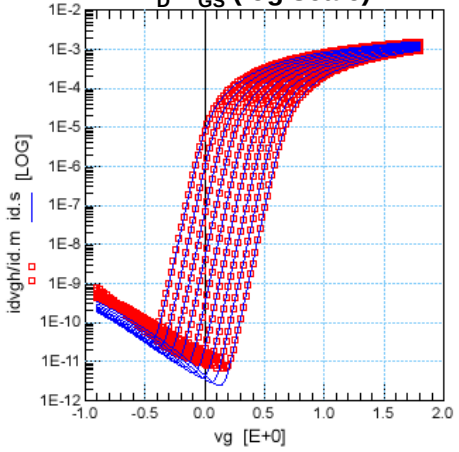
I_D-V_{DS} (lin scale)



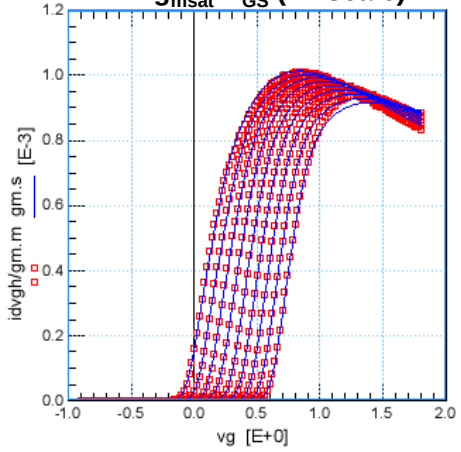
I_D-V_{GS} (lin scale)



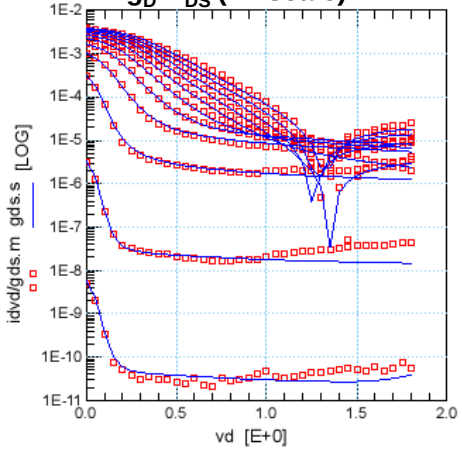
I_D-V_{GS} (log scale)



g_{msat}-V_{GS} (lin scale)



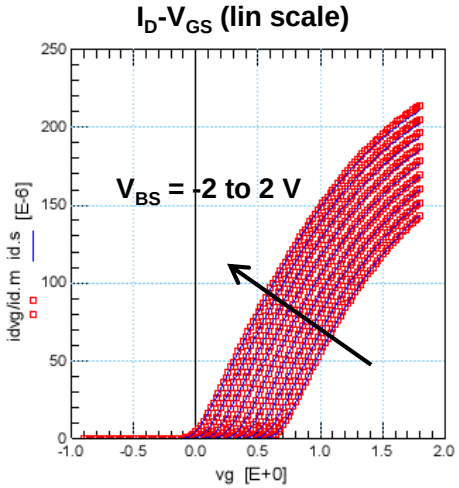
g_D-V_{DS} (lin scale)

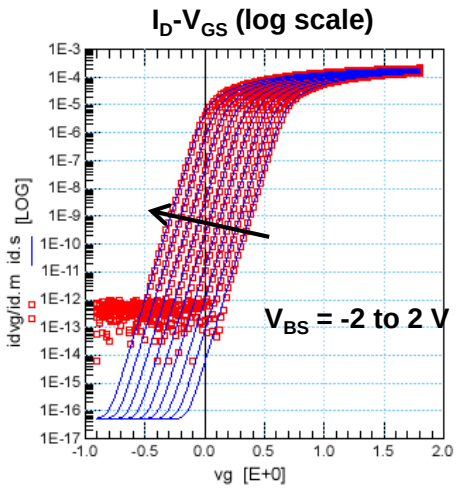


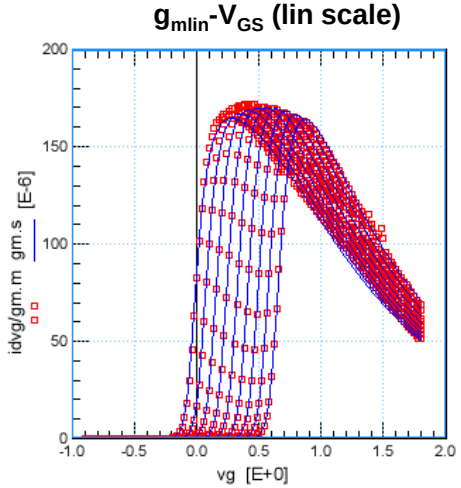
Short channel on thick front oxide device @ 25°C

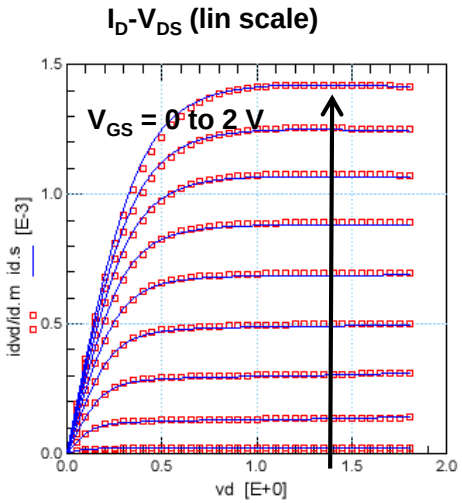
Wo. Impact Ionization

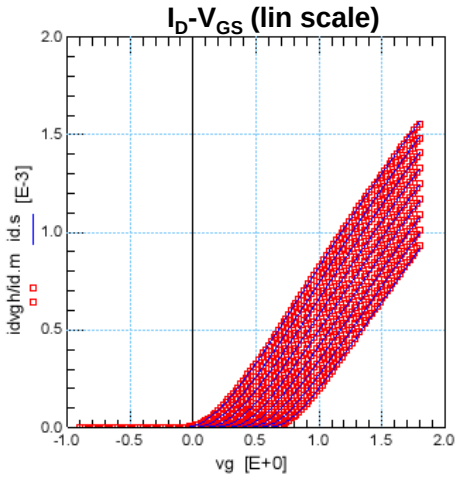
IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT

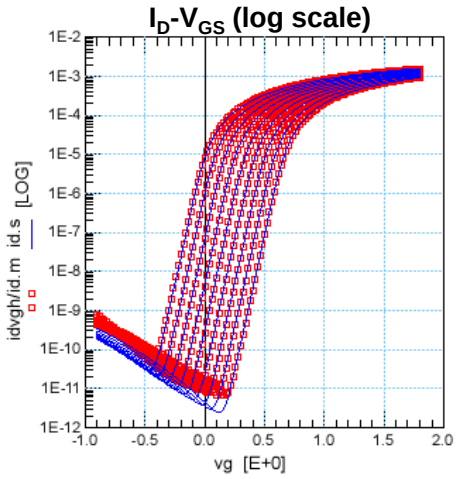


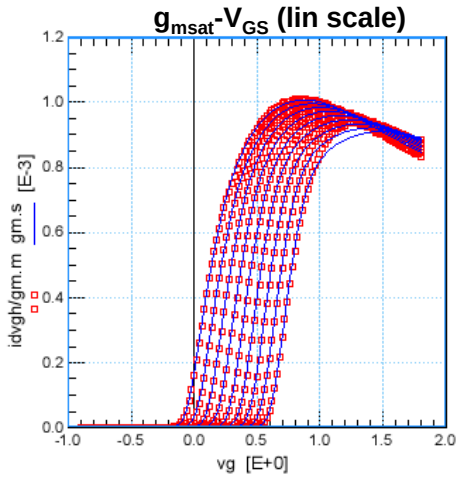


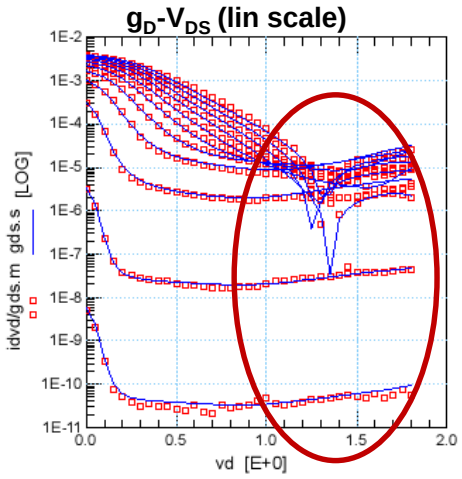












Short channel on thick front oxide device @ 25°C

W. Impact Ionization

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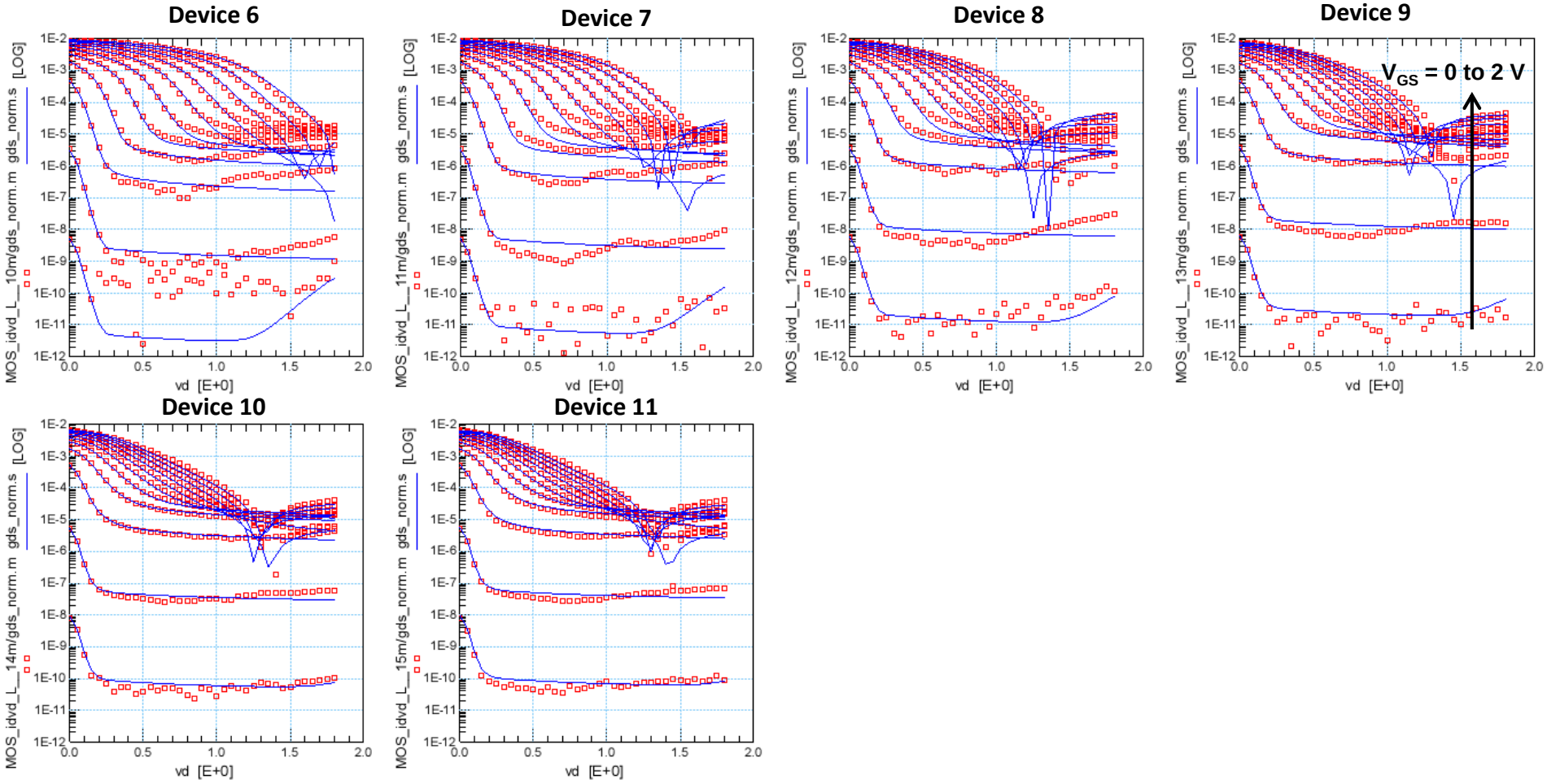
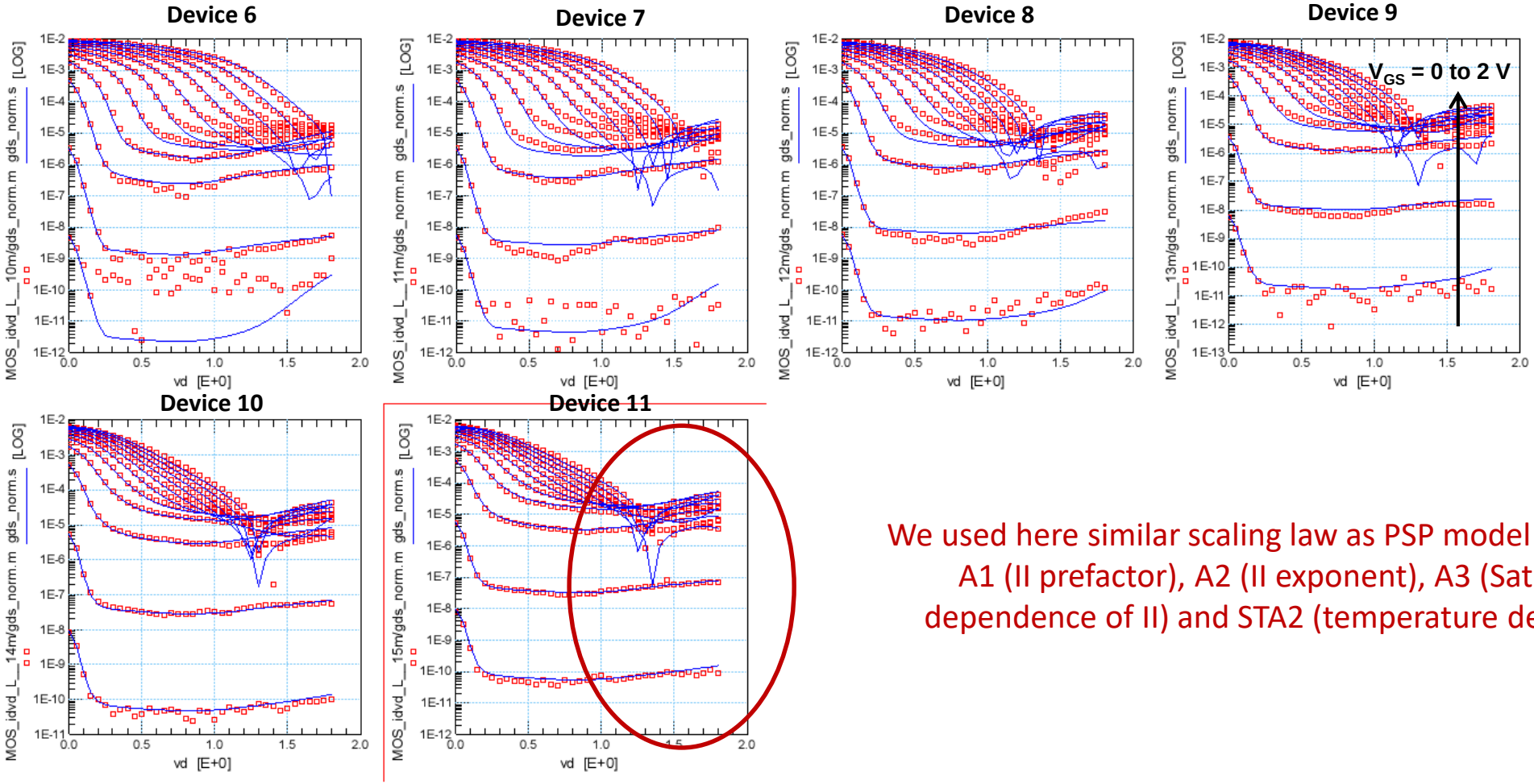


L scaling on thick front oxide device @ 25°C

W\L	Long	…	…	…	…	Short
Narrow	12	13	14	15		16
…	6	7	8	9	10	11
Wide	1	2	3	4		5

Wo. Impact Ionization

IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT



L scaling on thick front oxide device @ 25°C

We used here similar scaling law as PSP model with introduction of A1 (II prefactor), A2 (II exponent), A3 (Saturation-voltage dependence of II) and STA2 (temperature dependence of A2).

W\L	Long	…	…	…	…	Short
Narrow	12	13	14	15		16
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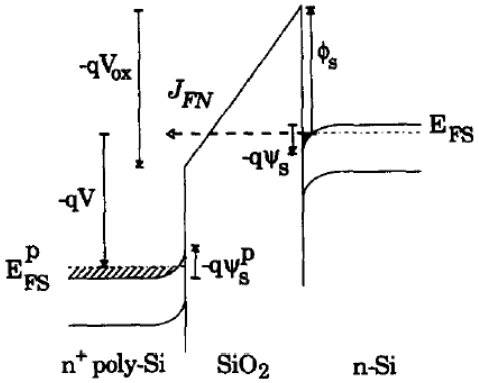
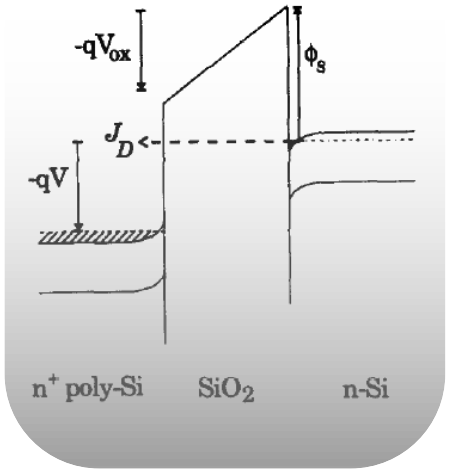
ACCURATE MODEL FOR OVERLAP GATE CURRENTS: PHYSICAL FOUNDATION OF GATE CURRENT MODEL IN L-UTSOI 1/2

Fowler-Nordheim (FN) [1-2]:
- For MOS structures with a relatively thick oxide.
- Barrier is triangular.

Direct Tunneling (DT) [1-2]:
- Oxides have thicknesses in the order of a few nanometers.
- Barrier is not triangular, but approximately trapezoidal.





Energy band diagram [1]

$$J_{FN} = AF_{ox}^2 \exp\left[-\frac{B}{F_{ox}}\right]$$

$$J_{DT} = \frac{A F_{ox}^2}{\left[1-\left(\frac{\phi_s + qV_{ox}}{\phi_s}\right)^{1/2}\right]^2} \times \exp\left[-\frac{B}{F_{ox}}\frac{\phi_s^{3/2} - (\phi_s - qV_{ox})^{3/2}}{\phi_s^{3/2}}\right]$$

Tunneling current density [2]

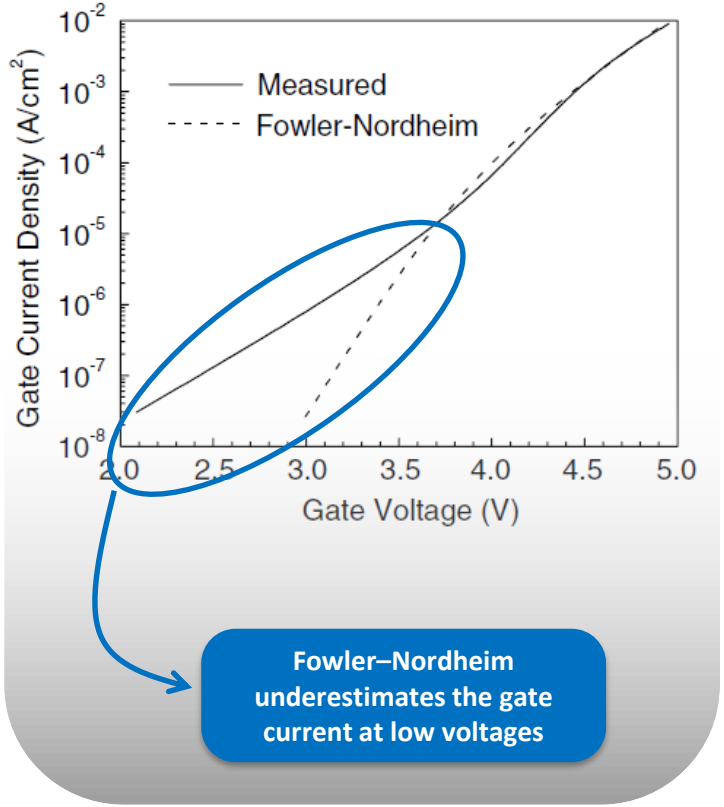


Illustration of experimental gate current density vs Fowler-Nordhiem [2]

In view of reduction of oxide thickness and supply voltage Direct tunneling is sufficient to model at first order gate current.

[1] M. Depas et al, SSE 1995; [2] Juan C. Ranuarez et al, Microelectronics Reliability 2006.

ACCURATE MODEL FOR OVERLAP GATE CURRENTS: PHYSICAL FOUNDATION OF GATE CURRENT MODEL IN L-UTSOI 2/2

Initially this model comes from PSP [1], where the integration over energy is skipped to obtain explicit function by assuming that all electrons have the same kinetic energy.

$$J_{g(x)} = J_0 . \int_0^{\infty} D_{(E,x)} . Fs_{(E,x)} . dy \sim J_0 . D_{(x)} . Fs_{(x)}$$

IGINV, IGOV … in PSP

$$\rightarrow \quad D_{(x)} = e^{-B0.f_{(zg)}}$$

$$\rightarrow \quad f_{(zg)} = \frac{1-(1-zg)^{1.5}}{zg} \sim -\frac{3}{2} + G2.zg + G3.zg$$

DT-like formulation

$$-\frac{B}{F_{ox}} \frac{\phi_s^{3/2} - (\phi_s - qV_{ox})^{3/2}}{\phi_s^{3/2}}$$

GC2O in PSP

GC3O in PSP

where $D_{(E,x)}$ is the transmission coefficient calculated in the WKB approximation, $Fs_{(E,x)}$ is the supply function and x is the position along the channel.

where zg is the voltage drop through the gate oxide normalized to the built-in voltage, J_0 and B_0 are constant related to the tunneling current.

G2 (0.375), G3 (0.063) is taylor expansion parameter.

In current version of L-UTSOI, this model is derived for « inversion » and « overlap » branch.

[1] Xin (Ben) Gu, Ten-Lon Chen, Gennady Gildenblat et al, TED Jan. 2004.

ACCURATE MODEL FOR OVERLAP GATE CURRENTS: EXTRA FOWLER-NORDHEIM CURRENT

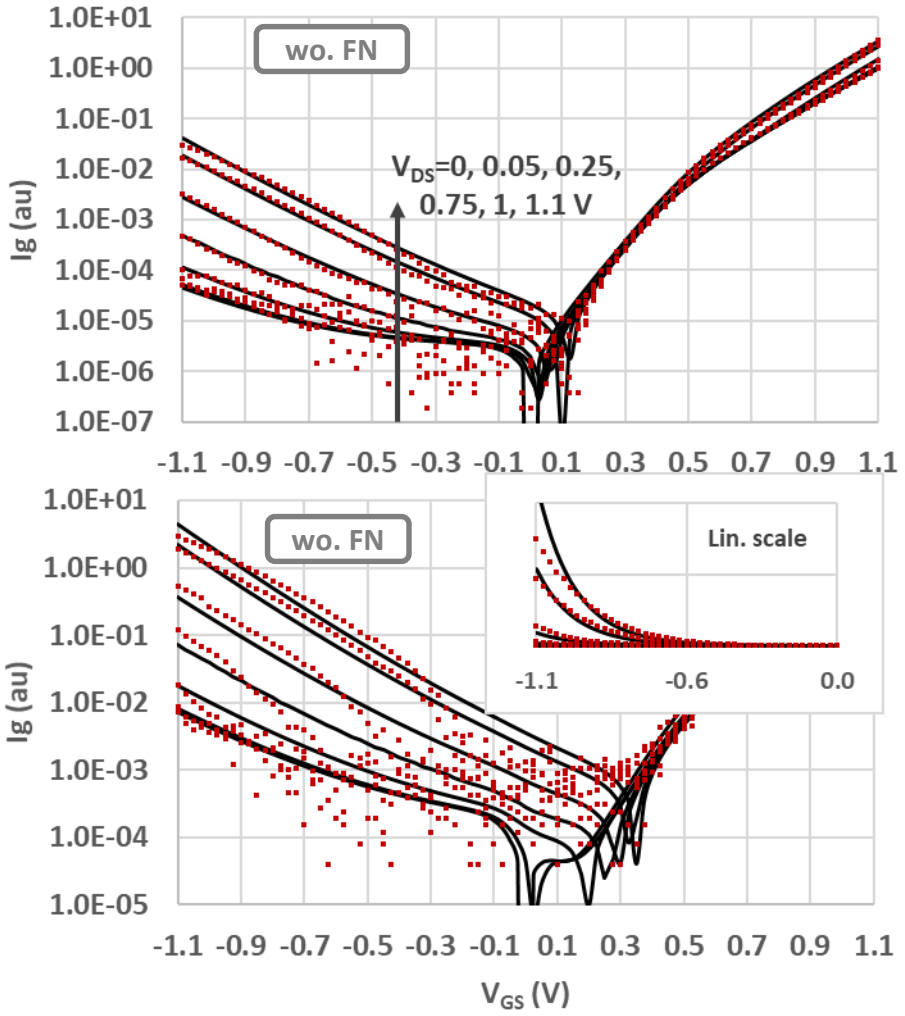
Discrepancy observed on gate current is evident for V_{GS}<<0 and V_{DS}>>0. We observe 2 differents behaviors at low and high V_{GD} values.

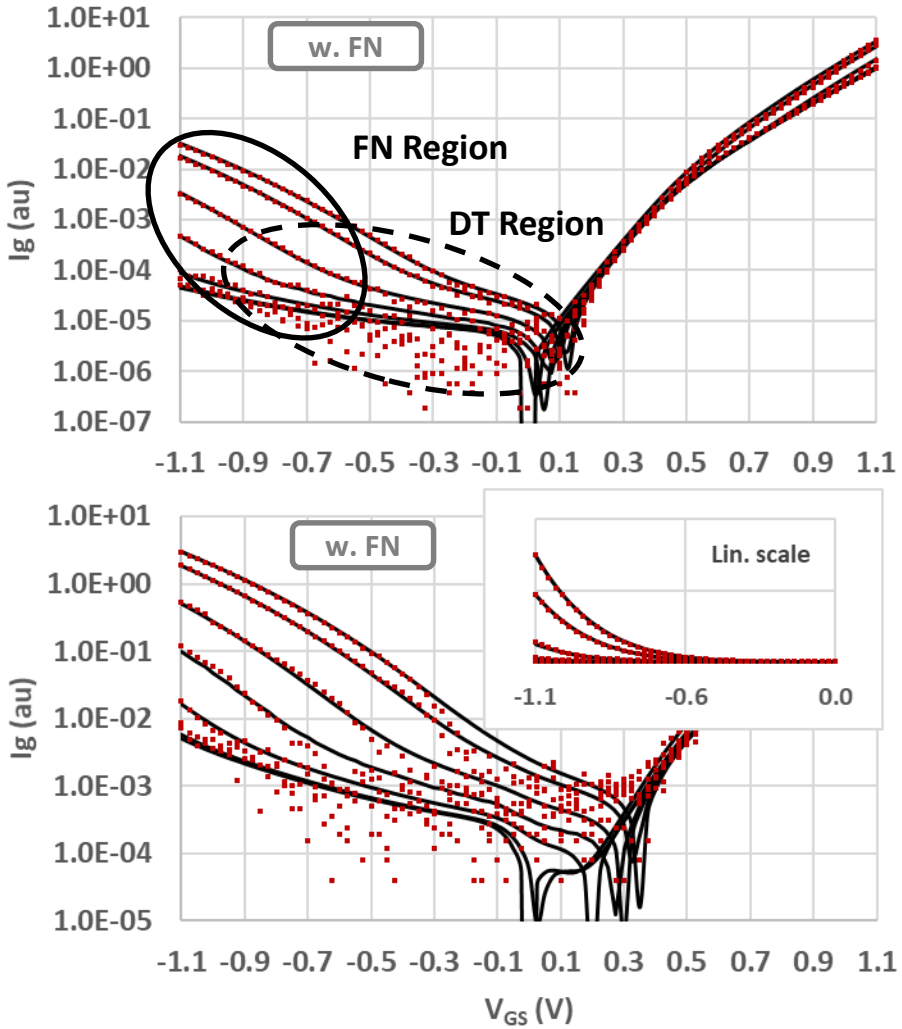
We propose to add high electric field component close to Fowler-Nordheim (FN) equation: $J_g \sim J_0 . Fs_{(x)} . \left[e^{-B0.(f_{(zg)})} \right] + FNOV . e^{-B0.\frac{GCOVFN}{zg}}$

We introduce 2 more parameters FNOV and GCOVFN

Long channel →

Short channel →





Outline

- Status of L-UTSOI

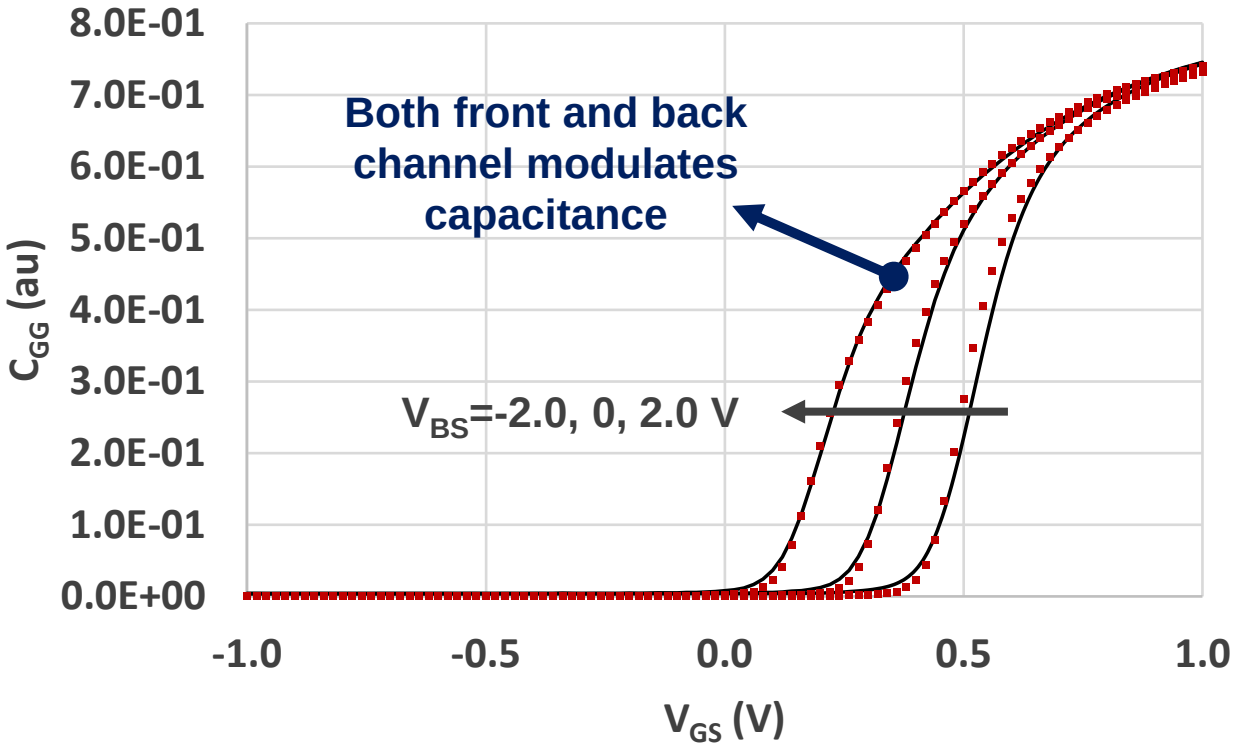
- Recent mayor development in L-UTSOI
  - Gm/Id improvement
  - Impact ionization evidence and modeling
  - Accurate model for overlap gate current

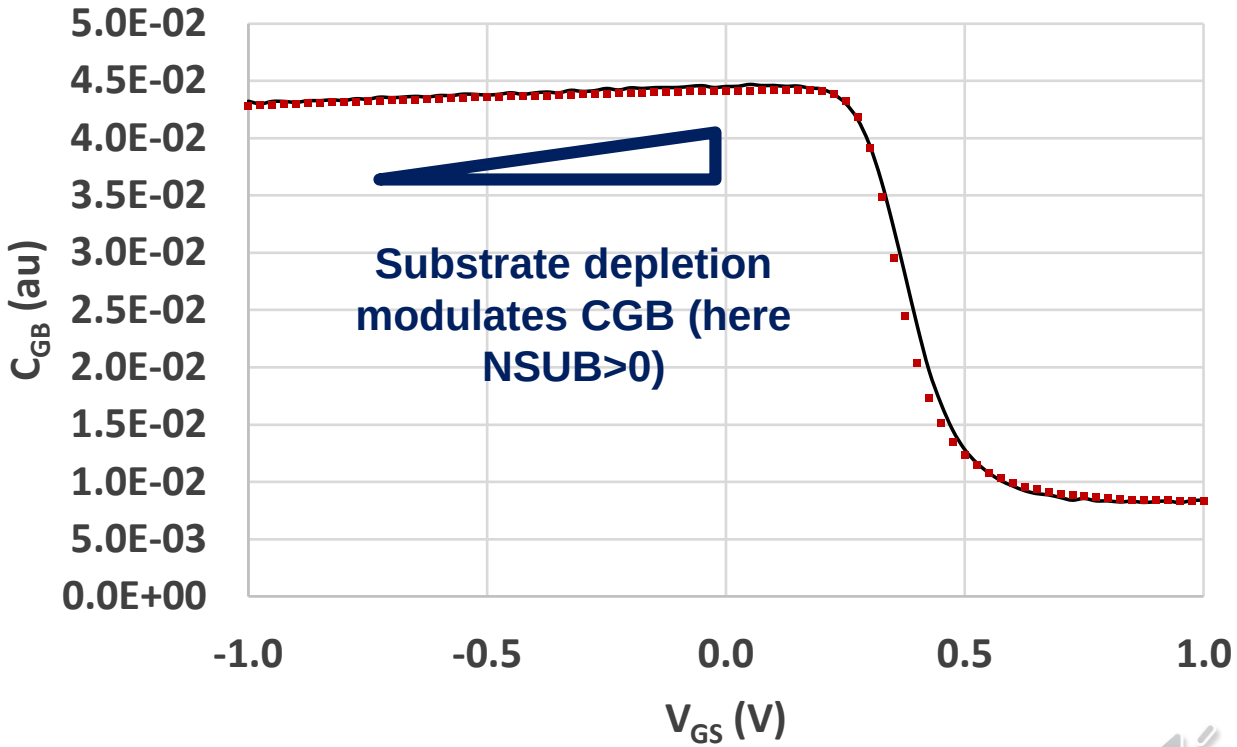
- L-UTSOI model extraction using 28NM FDSOI technology

- Conclusions/perspectives

L-UTSOI MODEL EXTRACTION USING 28NM FDSOI TECHNOLOGY: CV ILLUSTRATION ON LARGE DEVICE

Following the model extraction strategy [1], we have realized a parameter extraction using 28nm FDSOI technology. L-UTSOI is able to model all the features of FDSOI transistor characteristics for any bias configuration, including the case of the strong forward back bias, where two channels take place at the front and back interfaces of the thin silicon body



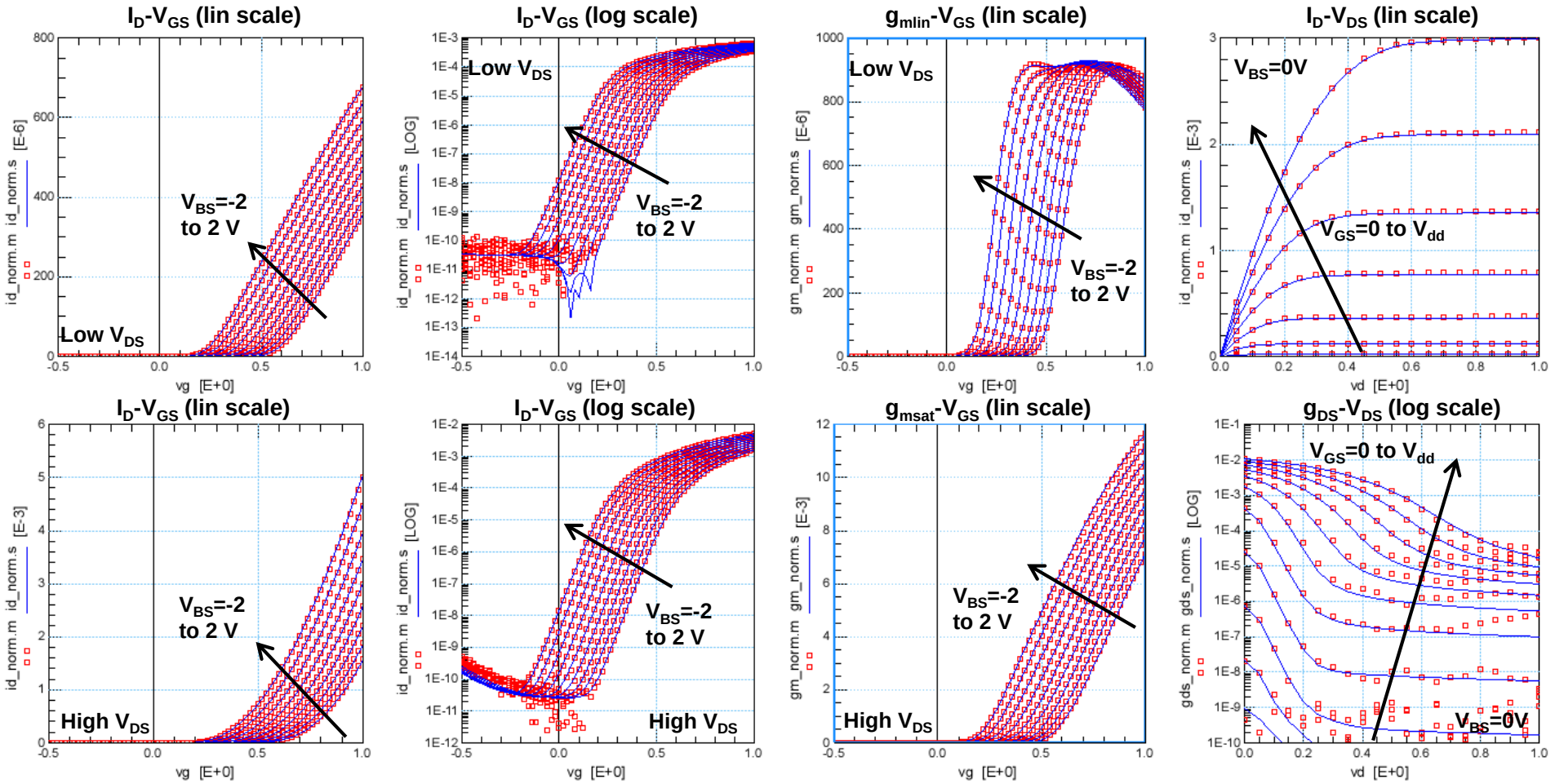


[1] L-UTSOI 102.4.0 user's manual.

CORNERS DEVICES: DEVICE 1 AT AMBIENT TEMPERATURE

W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

Dots: hardware
Lines: model

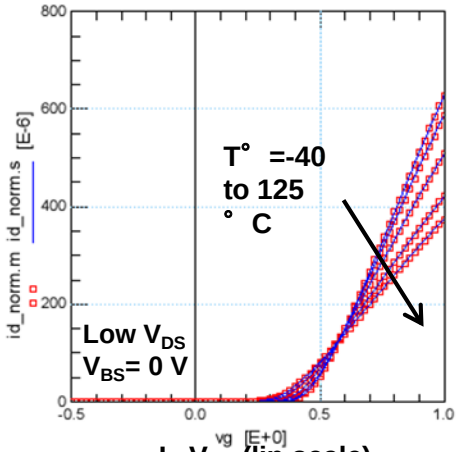


CORNERS DEVICES: DEVICE 1 VERSUS TEMPERATURE

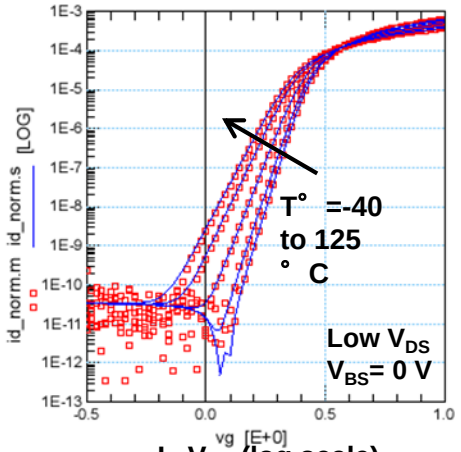
W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

Dots: hardware
Lines: model

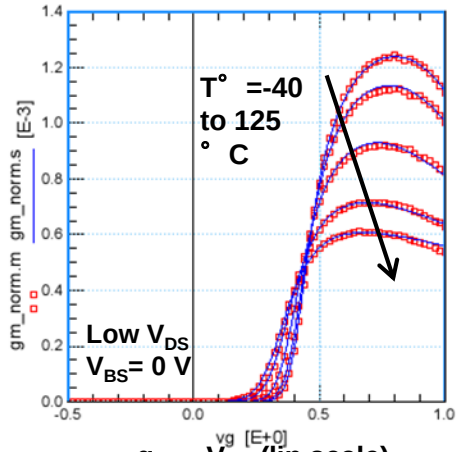
I_D-V_{GS} (lin scale)



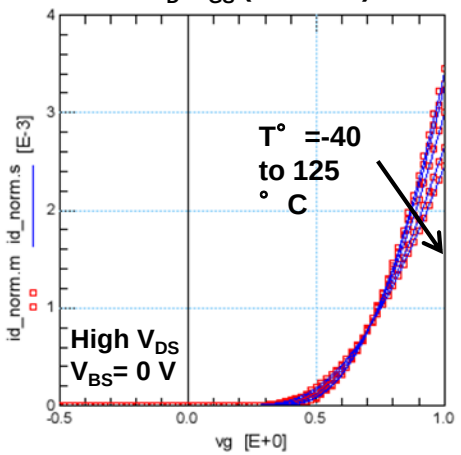
I_D-V_{GS} (log scale)



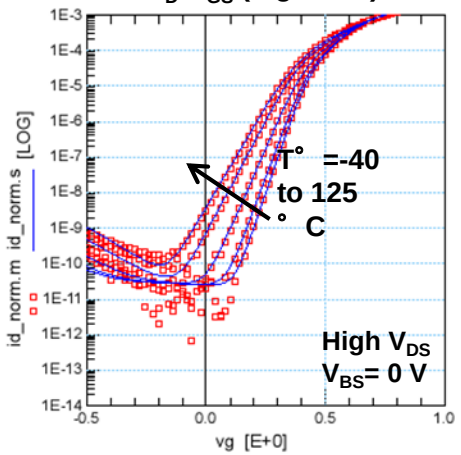
g_{mlin}-V_{GS} (lin scale)



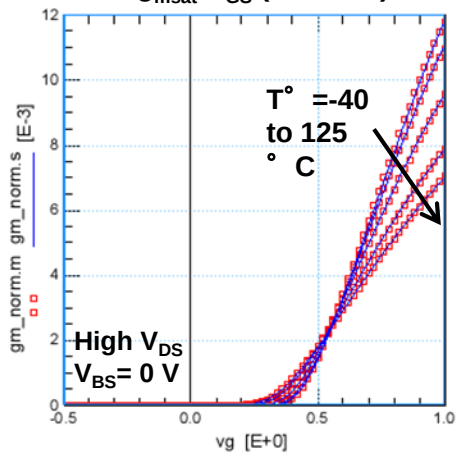
I_D-V_{GS} (lin scale)



I_D-V_{GS} (log scale)



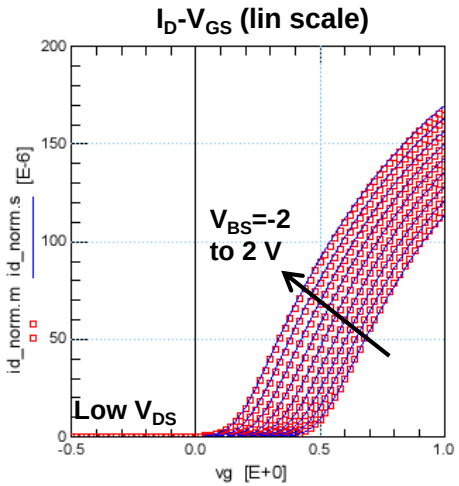
g_{msat}-V_{GS} (lin scale)

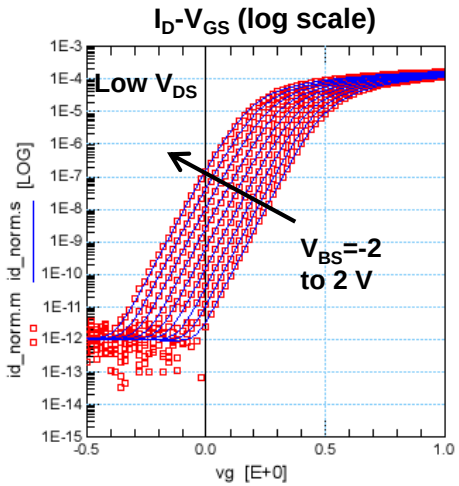


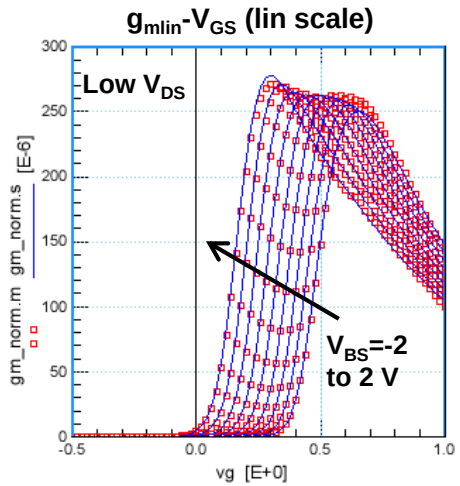
CORNERS DEVICES: DEVICE 6 AT AMBIENT TEMPERATURE

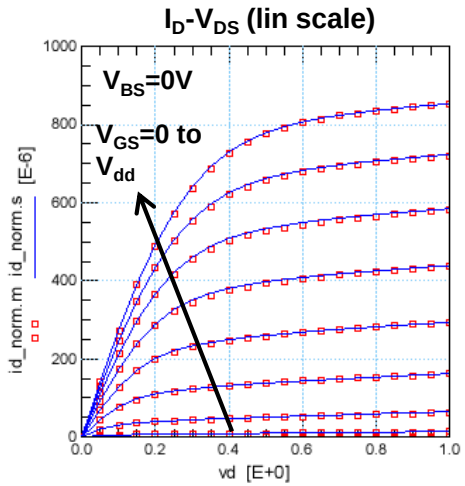
W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

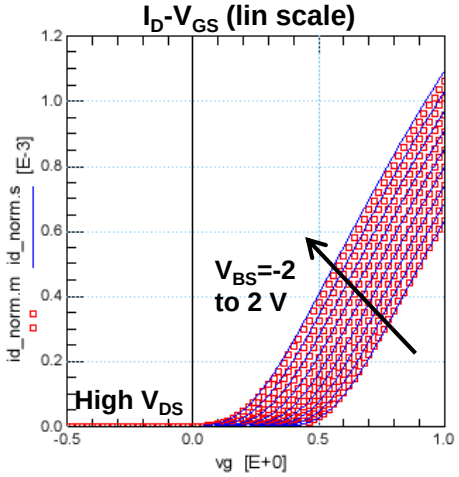
Dots: hardware
Lines: model

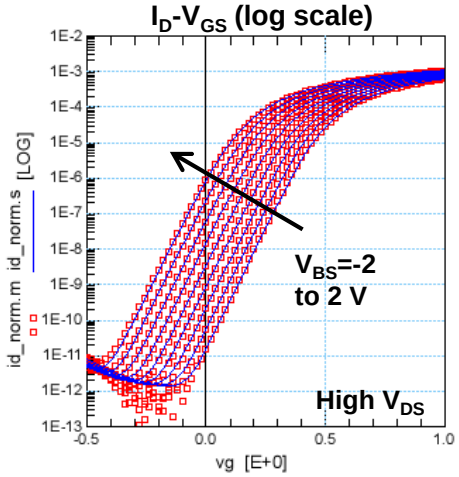


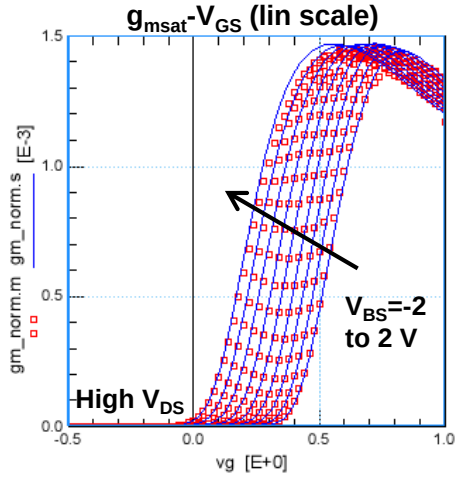


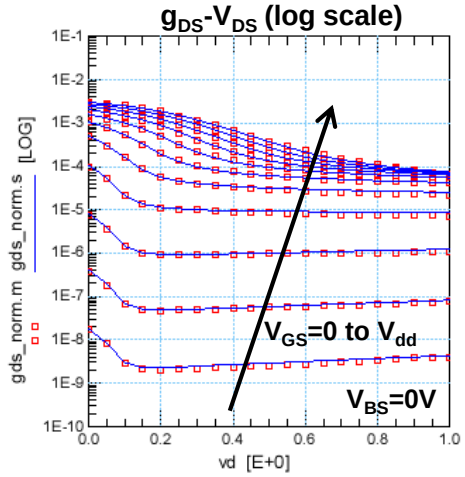










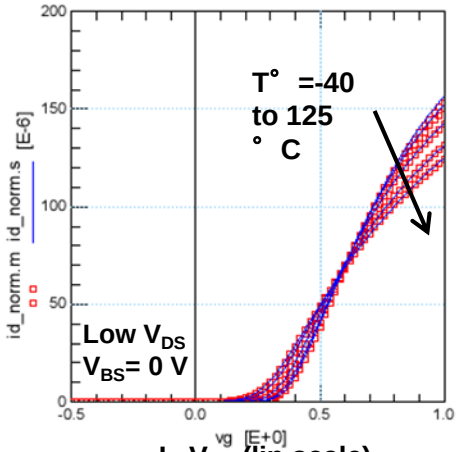


CORNERS DEVICES: DEVICE 6 VERSUS TEMPERATURE

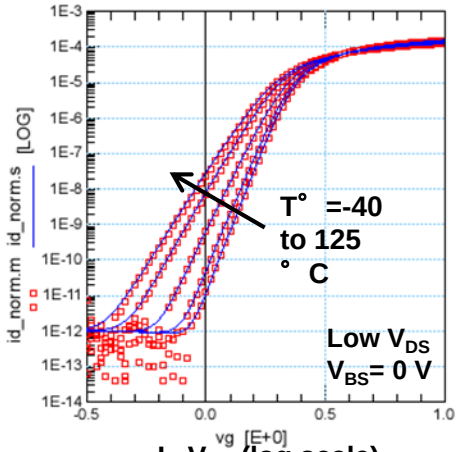
W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

Dots: hardware
Lines: model

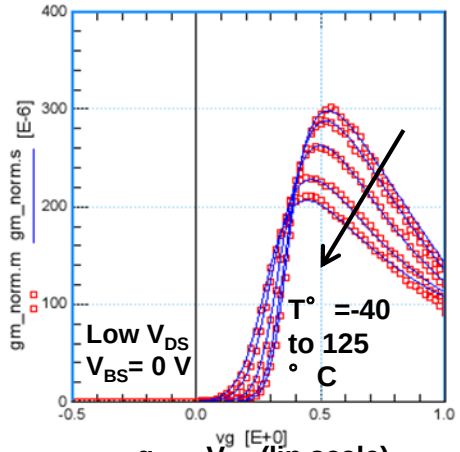
I_D-V_{GS} (lin scale)



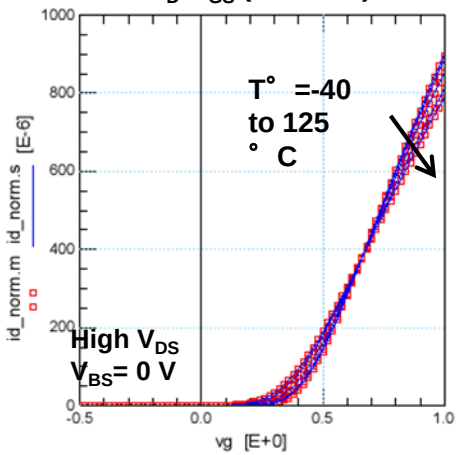
I_D-V_{GS} (log scale)



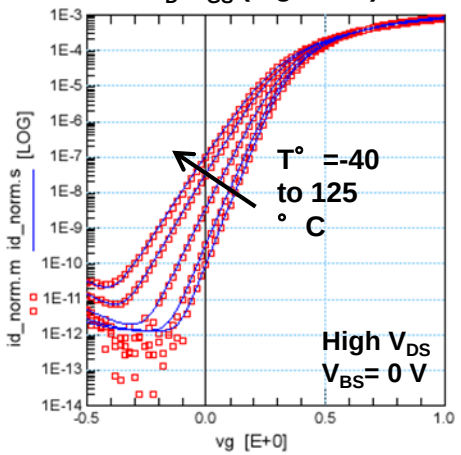
g_{mlin}-V_{GS} (lin scale)



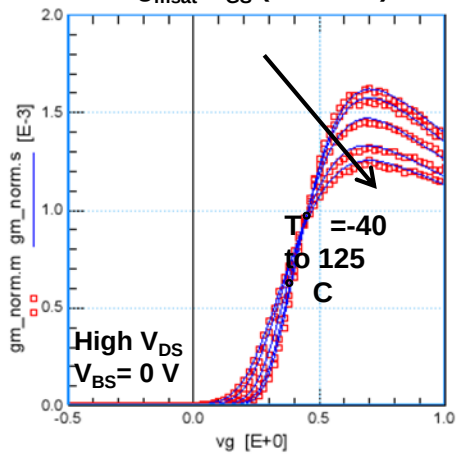
I_D-V_{GS} (lin scale)



I_D-V_{GS} (log scale)



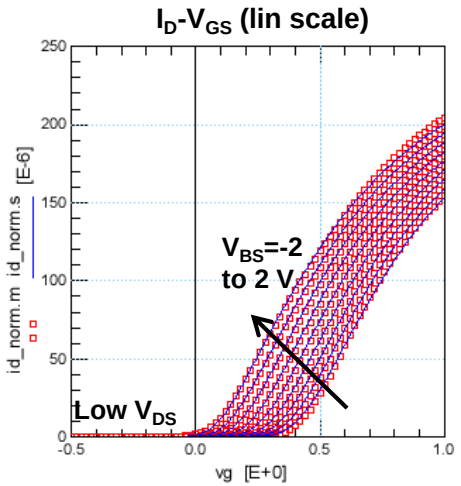
g_{msat}-V_{GS} (lin scale)

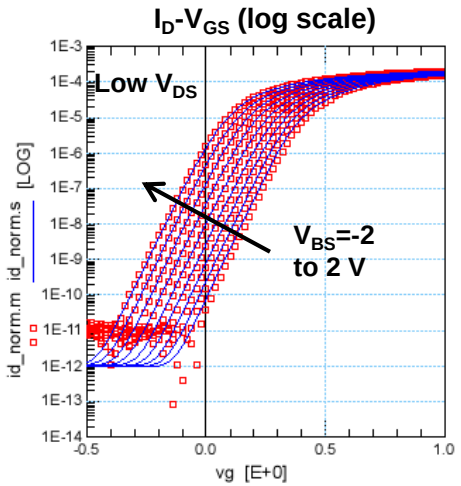


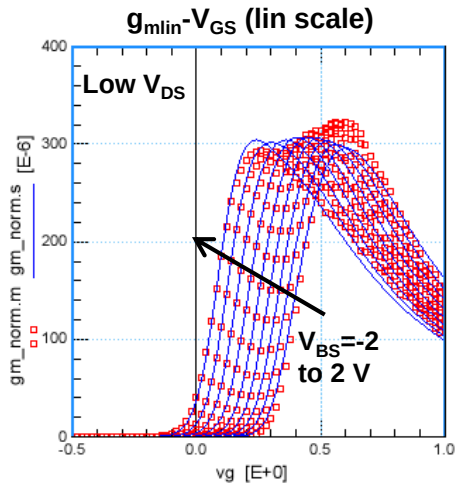
CORNERS DEVICES: DEVICE 9 AT AMBIENT TEMPERATURE

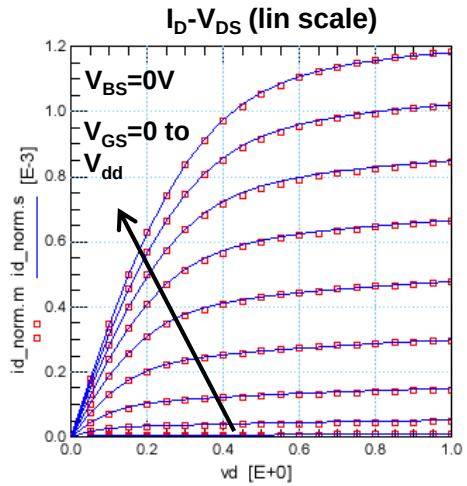
W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

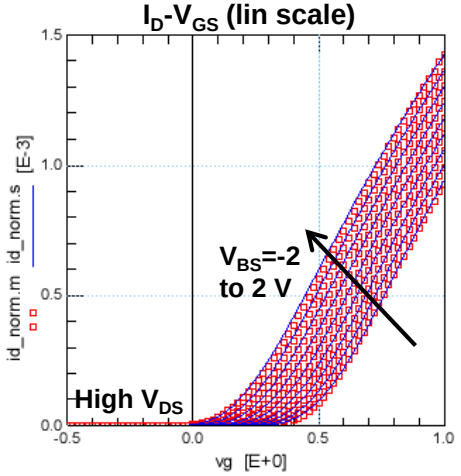
Dots: hardware
Lines: model

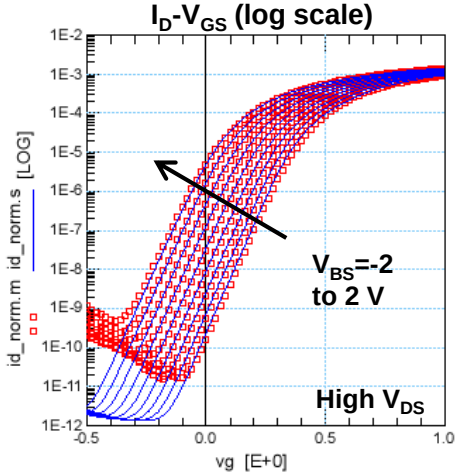


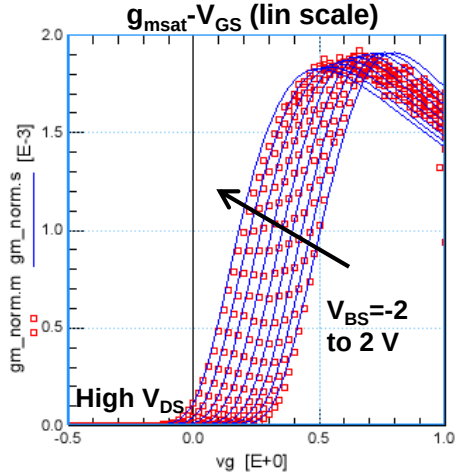


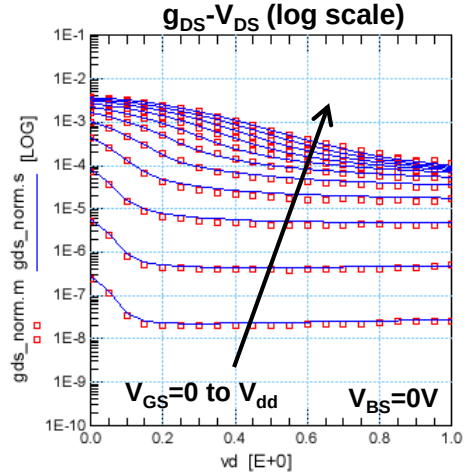










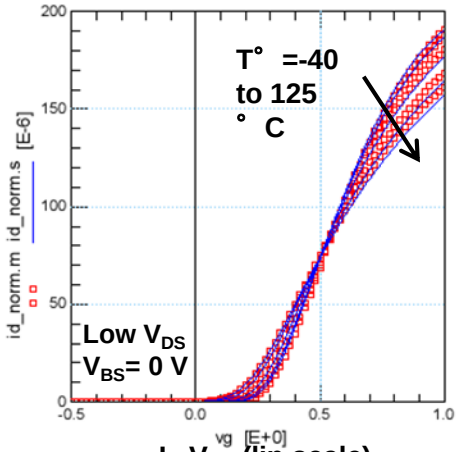


CORNERS DEVICES: DEVICE 9 VERSUS TEMPERATURE

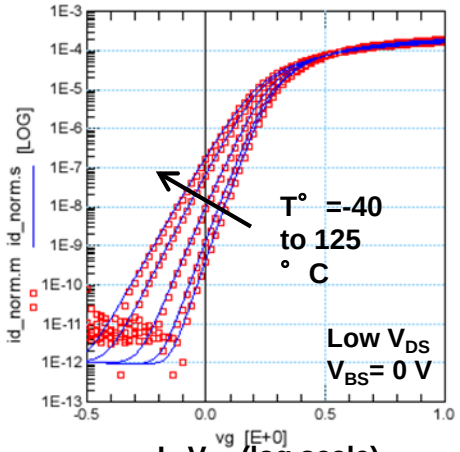
W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

Dots: hardware
Lines: model

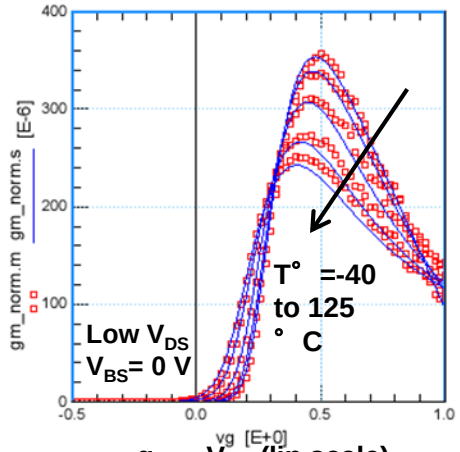
I_D-V_{GS} (lin scale)



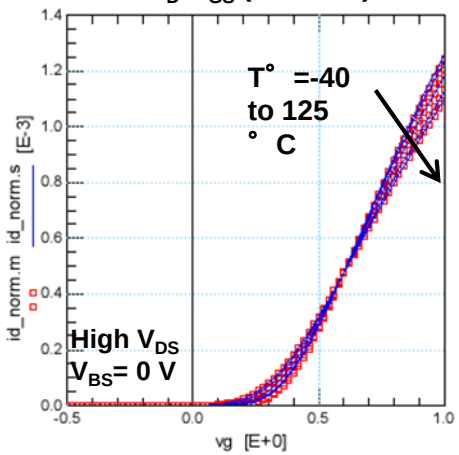
I_D-V_{GS} (log scale)



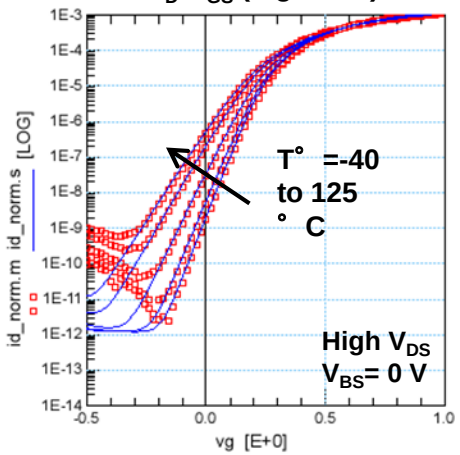
g_{mlin}-V_{GS} (lin scale)



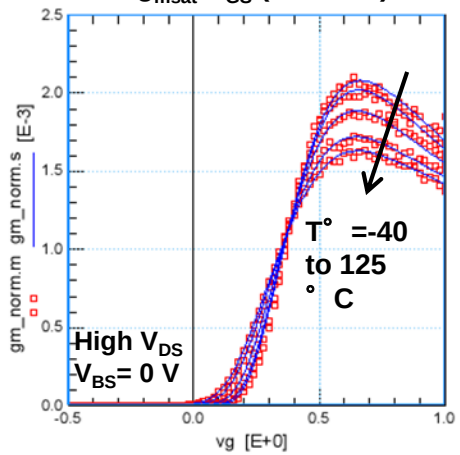
I_D-V_{GS} (lin scale)



I_D-V_{GS} (log scale)



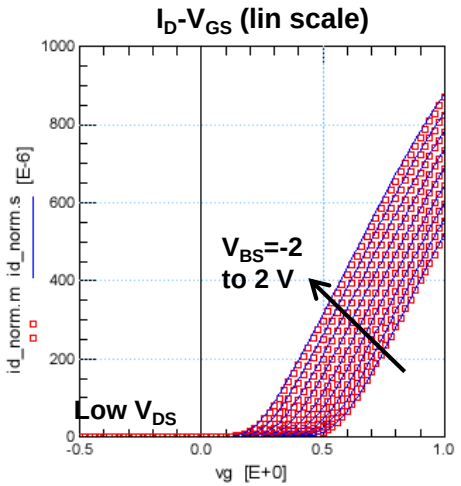
g_{msat}-V_{GS} (lin scale)

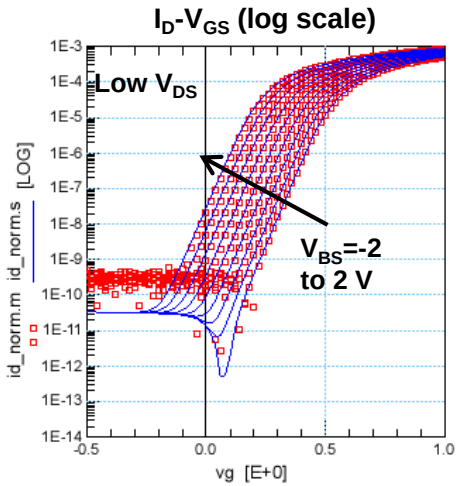


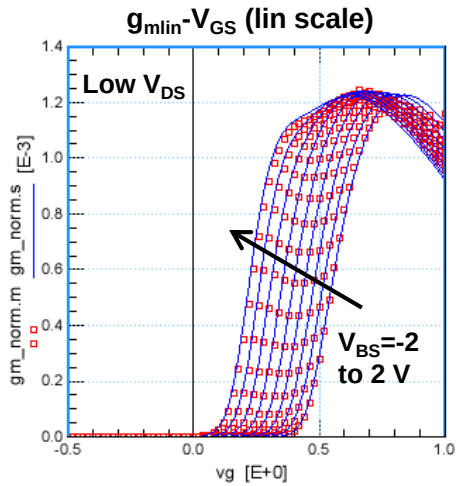
CORNERS DEVICES: DEVICE 12 AT AMBIENT TEMPERATURE

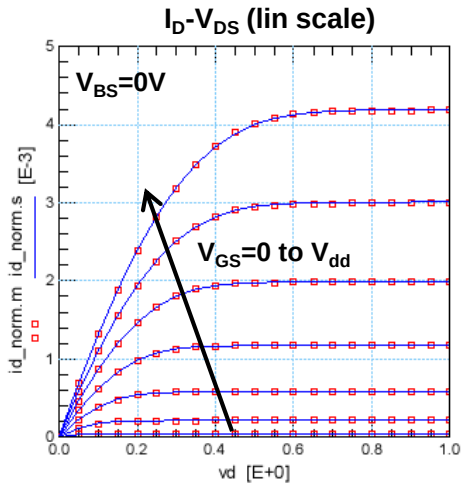
W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

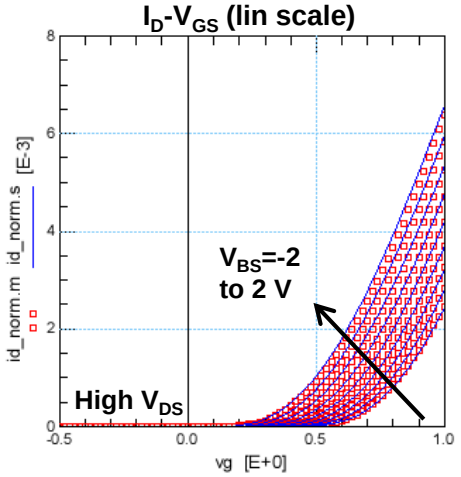
Dots: hardware
Lines: model

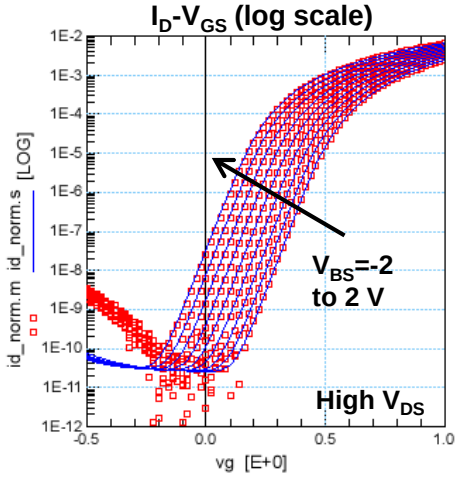


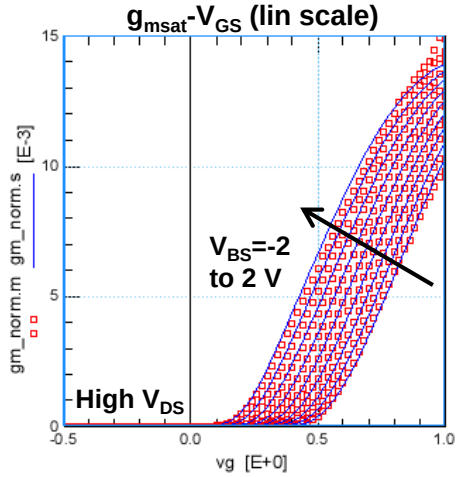


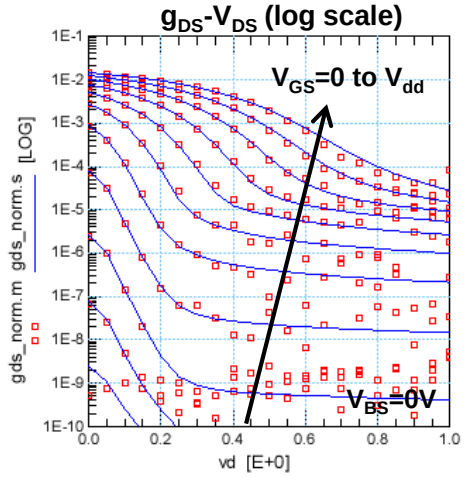










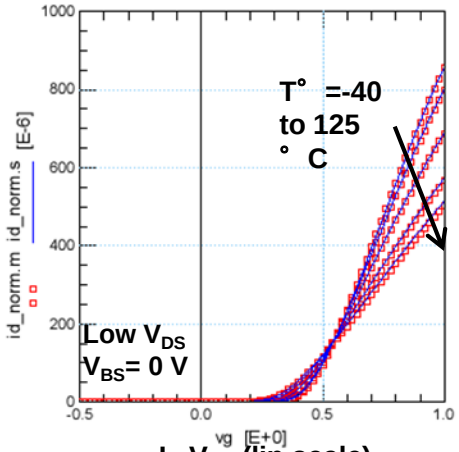


CORNERS DEVICES: DEVICE 12 VERSUS TEMPERATURE

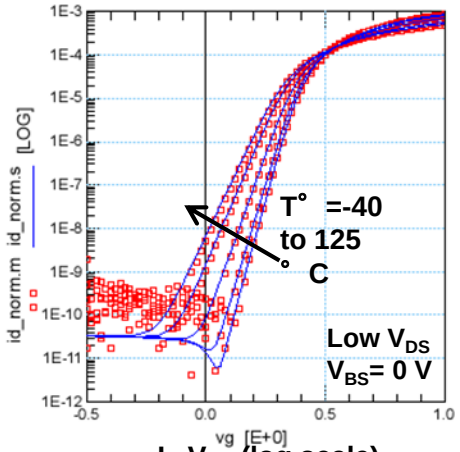
W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

Dots: hardware
Lines: model

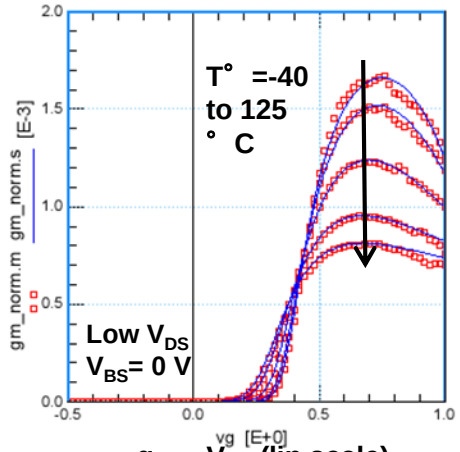
I_D-V_{GS} (lin scale)



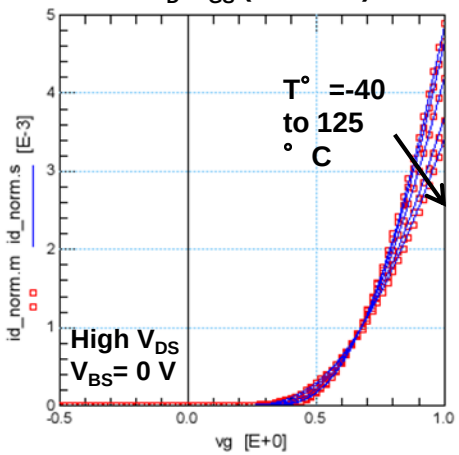
I_D-V_{GS} (log scale)



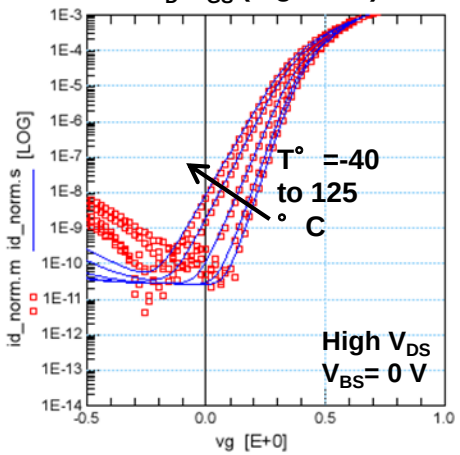
g_{mlin}-V_{GS} (lin scale)



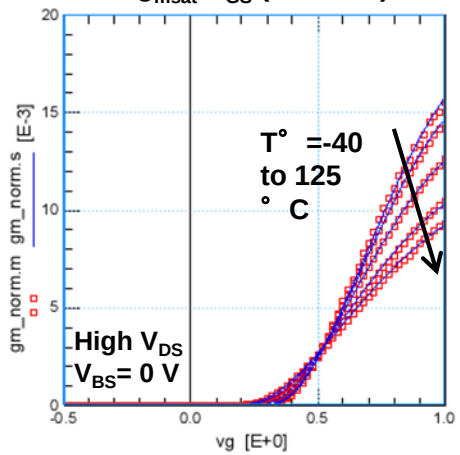
I_D-V_{GS} (lin scale)



I_D-V_{GS} (log scale)



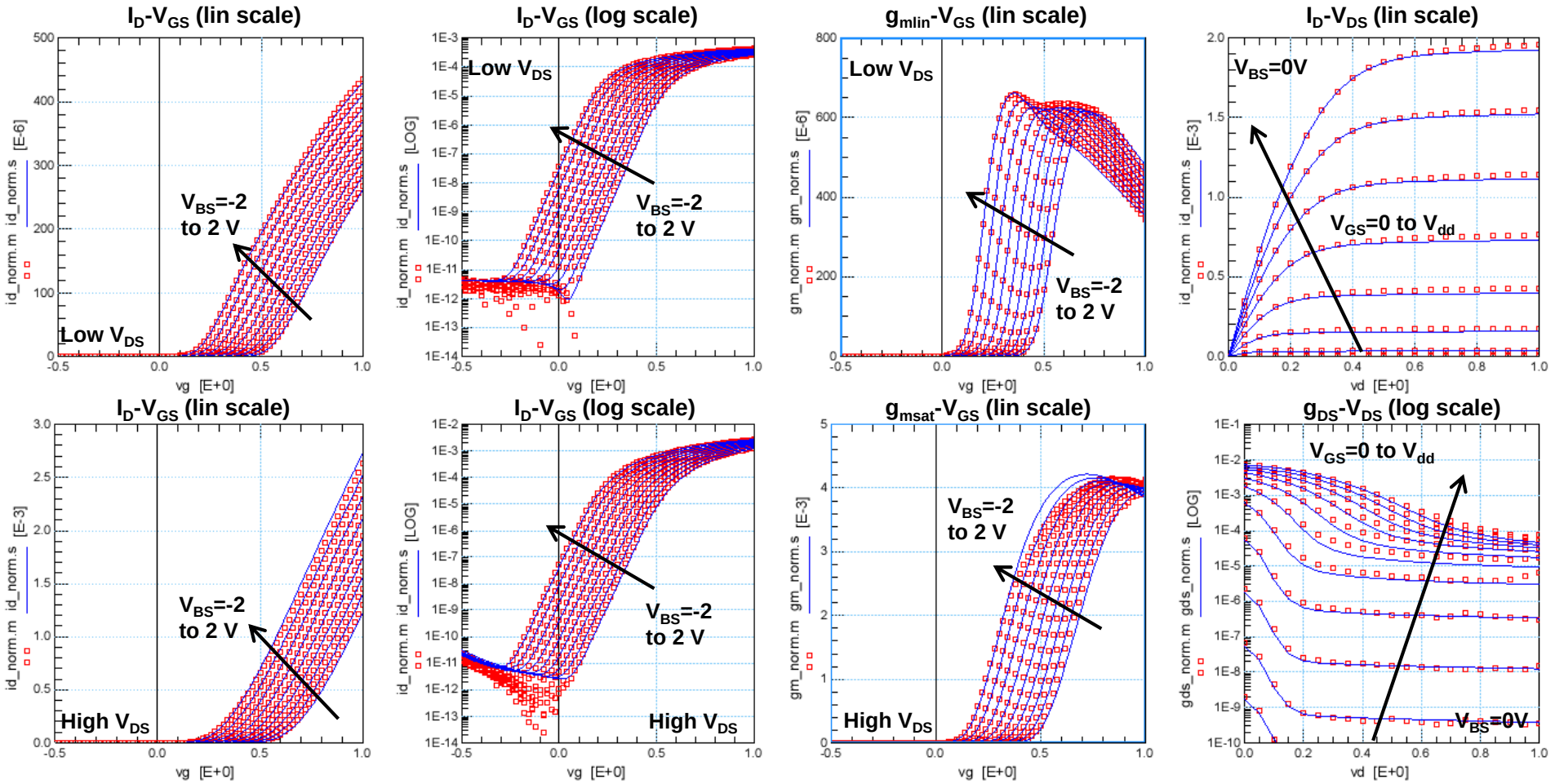
g_{msat}-V_{GS} (lin scale)



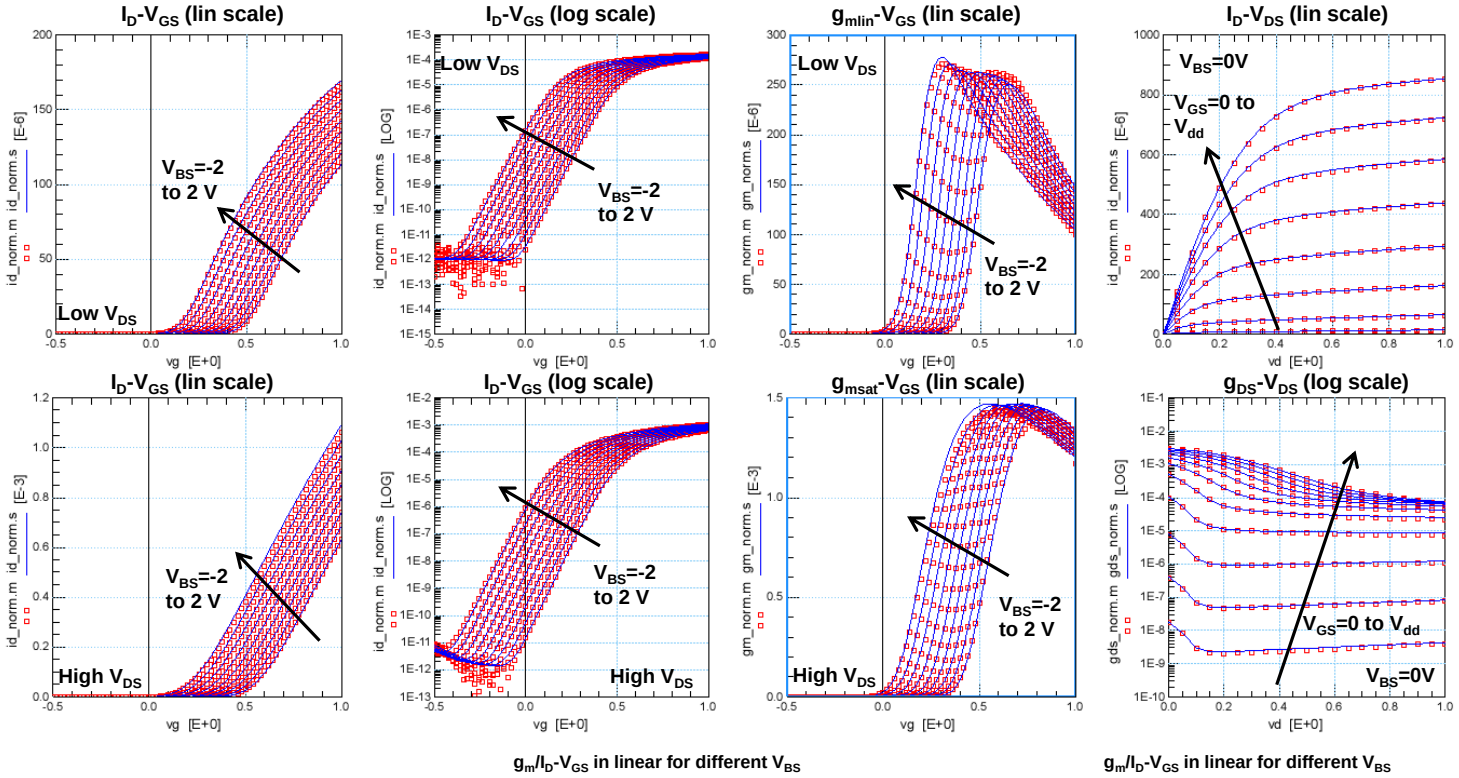
INTERMEDIATE: DEVICE 3 AT AMBIENT TEMPERATURE

W\L	Long	...	...	...	...	Short
Narrow	12					9
...	11					8
...	10					7
Wide	1	2	3	4	5	6

Dots: hardware
Lines: model



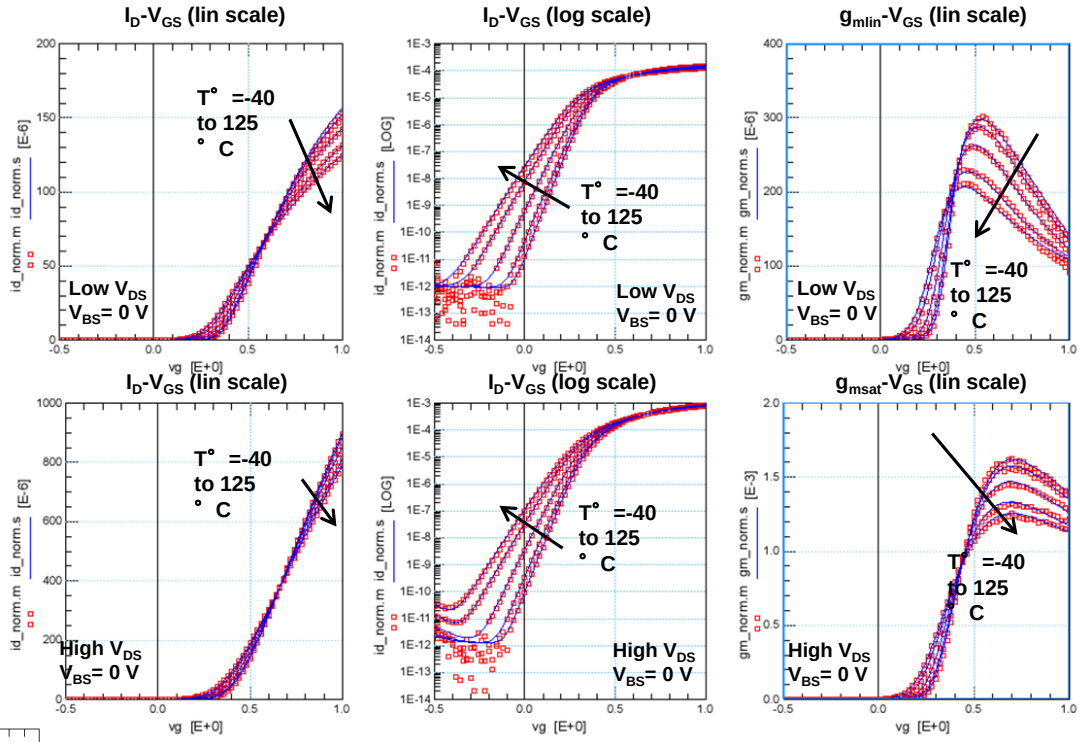
L-UTSOI MODEL EXTRACTION USING 28NM FDSOI TECHNOLOGY: IV ILLUSTRATION ON SHORT DEVICE

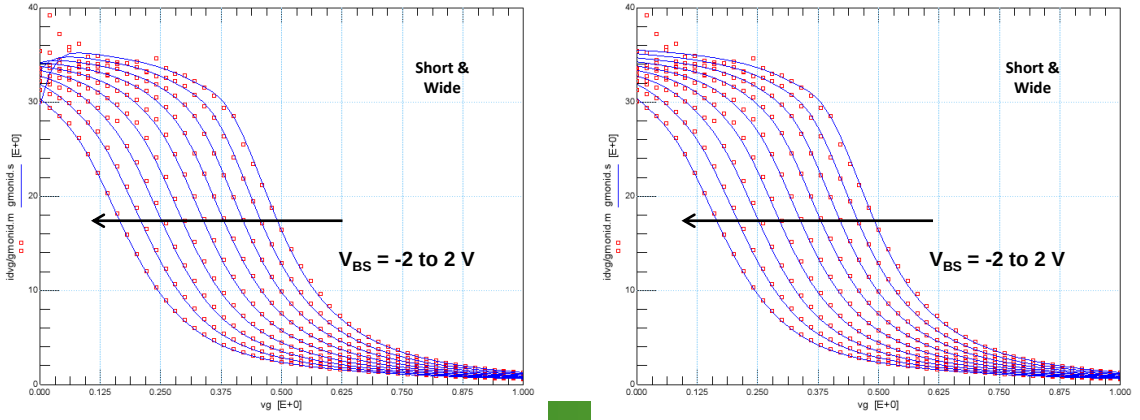


g_m/I_D-V_{GS} in linear for different V_{BS}

g_m/I_D-V_{GS} in linear for different V_{BS}

IV for different temperature model vs exp.





Gm/id curve in linear and saturate

This accuracy is obtained thanks to the activation of backplane depletion, quantum confinement, mobility distinction between front & back channels and physical effects detailed in previous parts.

Outline

- Status of L-UTSOI

- Recent mayor development in L-UTSOI
  - Gm/Id improvement
  - Impact ionization evidence and modeling
  - Accurate model for overlap gate current

- L-UTSOI model extraction using 28NM FDSOI technology

- Conclusions/perspectives

CONCLUSIONS / REMARKS

- We have presented the recent improvements brought to L-UTSOI model to improve its accuracy and predictability in moderate and weak inversion regions.

- By comparison with experimental data, we have illustrated the enhanced accuracy obtained on gm/Id thanks to the introduction of source/drain depletion effect, on the output conductance thanks to the implementation of the impact ionization effect, and on gate tunneling current, thanks to the adding of a Fowler-Nordheim component.

- L-UTSOI standard model (former Leti-UTSOI 2) is available in all major commercial SPICE simulators (SPECTRE, HSPICE, ELDO, ADS …).

- Future work is planned in the “whish list” of L-UTSOI Working Group (CMC):

https://si2.org/cmc/

https://si2.org/2020/03/10/lutsol/

MAIN REFERENCE PUBLICATIONS

Main Reference publications:

- **L-UTSOI 102.4.0 user's manual.**

"Leti-UTSOI2.1: A Compact Model for UTBB-FDSOI Technologies—Part I: Interface Potentials Analytical Model", T. Poiroux, Member, IEEE, O. Rozeau, P. Scheer, S. Martinie, M. A. Jaud, M. Minondo, A. Juge, J. C. Barbé, and M. Vinet. IEEE Transactions on Electron Devices (Volume: 62 , Issue: 9 , Sept. 2015)

https://ieeexplore.ieee.org/abstract/document/7185387

"Leti-UTSOI2.1: A Compact Model for UTBB-FDSOI Technologies—Part II: DC and AC Model Description", Thierry Poiroux, Member, IEEE, O. Rozeau, Patrick Scheer, Sébastien Martinie, Marie-Anne Jaud, M. Minondo, André Juge, J. C. Barbé, and Maud Vinet. IEEE Transactions on Electron Devices (Volume: 62 , Issue: 9 , Sept. 2015)

https://ieeexplore.ieee.org/abstract/document/7185413

"UTSOI2: A complete physical compact model for UTBB and independent double gate MOSFETs", T. Poiroux, O. Rozeau, S. Martinie, P. Scheer, S. Puget, M.A. Jaud, S. El Ghouli, J.C. Barbé, A. Juge, O. Faynot. 2013 IEEE International Electron Devices Meeting.

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6724616

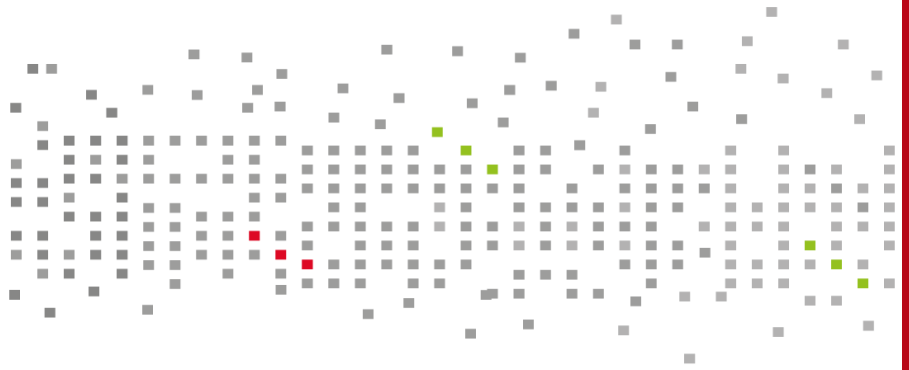
Presentation @ MOS-AK Grenoble 2015

http://www.mos-ak.org/grenoble_2015/presentations/T10_Poiroux_MOS-AK_Grenoble_2015.pdf

Presentation @ MOS-AK WashingtonDC 2013

http://www.mos-ak.org/washington_dc_2013/presentations/T9_Poiroux_MOS-AK_WashingtonDC_2013.pdf

Thank you for your attention



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