Latest developments of L-UTSOI: 
A compact model dedicated to low-power analog 
and digital applications in FDSOI technologies

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MOS-AK Compact Modeling Workshop 
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Status of L-UTSOI

Recent mayor development in L-UTSOI
- Gm/Id improvement
- Impact ionization evidence and modeling
- Accurate model for overlap gate current

L-UTSOI model extraction using 28NM FDSOI technology

Conclusions/perspectives
INTRODUCTION:
STRONG FORWARD BACK BIAS MANDATORY FOR FDSOI

• L-UTSOI is the first compact model able to describe FDSOI transistor behavior in all bias configurations, including strong forward back bias.
• But a model ignoring the formation of a strong inversion layer at the back interface lacks of accuracy in transistor electrostatics description
  - even at null back-bias in case of flip-well devices
  - inaccuracy gets worse as back-bias goes forward
  - inaccuracy not only on C(V) but also on Gm
➢ To be considered as a mandatory requirement for FDSOI technologies

INTRODUCTION: BRIEF MODEL HISTORY

- From 2013, the need to consider FDSOI transistor as a true independent double gate transistor, with possible conduction at both thin body interfaces, is fulfilled by Leti-UTSOI 2.x.x versions.
- Since 2013, the model has been further improved, based on industrial partner needs.
- Since 2020 L-UTSOI is a standard model.
Outline

☐ Status of L-UTSOI

☐ Recent mayor development in L-UTSOI
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☐ L-UTSOI model extraction using 28NM FDSOI technology

☐ Conclusions/perspectives
GM/ID IMPROVEMENT: INTRODUCTION OF EFFECTIVE DOPING

Starting from the surface potential accounting for SCE [1]:

\[ \psi_{2D(x)} = \psi_{1D} + (\psi_{\text{edge}} - \psi_{1D})e^{-x/\lambda_{2D}} + ((\psi_{\text{edge}} - \psi_{1D})e^{-(L-x)/\lambda_{2D}} \]

In the depleted S/D region, we simplify the 2D Poisson’s equation by considering that a fraction of the depletion charge \( \alpha \) acts on the longitudinal electric field:

\[
\begin{align*}
E_{x,\text{edge}} &= \pm (\psi_{\text{edge}} - \psi_{1D})/\lambda_{2D} \\
\varepsilon_{Si} E_{x,\text{edge}} &= q\alpha N_{sd} x_{\text{dep}} \\
\psi_{\text{electrode}} - \psi_{\text{edge}} &= E_{x,\text{edge}} x_{\text{dep}}/2
\end{align*}
\]

This effective doping \( \alpha N_{SD} \) is the model parameter to modulate the source/drain depletion. (implementation is detailed in the user’s manual [2])

where \( \psi_{1D} \) is a smooth minimum function between the long channel surface potential at the center and its threshold value (to extend the validity in moderate inversion) & \( \lambda_{2D} \) is the bi-dimensional characteristic length of the device

\[ \psi_{\text{edge}} = \psi_{1D} + \psi_{\text{dep}} \left[ \sqrt{1 + 2 (\psi_{\text{electrode}} - \psi_{1D})/\psi_{\text{dep}} - 1} \right] \]

\[ \psi_{\text{dep}} = q\alpha N_{SD}\lambda_{2D}^2 / \varepsilon_{Si} \]

GM/ID IMPROVEMENT: MODEL VS EXPERIMENT

Short channel on thin front oxide device @ 25°C

An accurate description of gm/Id is achieved thanks to implementation of S/D depletion
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Conclusions/perspectives
In FDSOI transistor, Impact ionization is more significant for thicker oxide transistors, featuring higher supply voltages, and only weak avalanche occurs.

This small impact ionization component increases source/drain current (in opposition to bulk MOSFET where impact ionization results in a bulk/drain current).

Inclusion of this model in term of physics and code implantation is close to that of PSP model [1]. For low-level avalanche multiplication, the avalanche current is [2]:

\[
I_{aval} = I_{DS} \cdot \int_{0}^{L} \alpha_n \cdot dx \sim A1. \Delta V_{sat}. I_{DS} \cdot e^{-\frac{a_2}{\Delta V_{sat}}}
\]

\[
\Delta V_{sat} = V_{DS} - A3. V_{DSsat}
\]

\[
a_2 = A2. (T_{KC}/T_{KR})^{STA2}
\]

where A1, A2, A3 and STA2 are related parameters.

IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT

Negative gm is the consequence of SHE
IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT

Short channel on thick front oxide device @ 25°C

Wo. Impact Ionization
IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT

$V_{BS} = -2 \text{ to } 2 \text{ V}$

Short channel on thick front oxide device @ 25°C

W. Impact Ionization
IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT

L scaling on thick front oxide device @ 25°C

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IMPACT IONIZATION EVIDENCE AND MODELING:
MODEL VS EXPERIMENT

We used here similar scaling law as PSP model with introduction of A1 (II prefactor), A2 (II exponent), A3 (Saturation-voltage dependence of II) and STA2 (temperature dependence of A2).

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Conclusions/perspectives
ACCURATE MODEL FOR OVERLAP GATE CURRENTS:
PHYSICAL FOUNDATION OF GATE CURRENT MODEL IN L-UTSOI 1/2

Fowler-Nordheim (FN) [1-2]:
- For MOS structures with a relatively thick oxide.
- Barrier is triangular.

Direct Tunneling (DT) [1-2]:
- Oxides have thicknesses in the order of a few nanometers.
- Barrier is not triangular, but approximately trapezoidal.

In view of reduction of oxide thickness and supply voltage Direct tunneling is sufficient to model at first order gate current.

ACCURATE MODEL FOR OVERLAP GATE CURRENTS:
PHYSICAL FOUNDATION OF GATE CURRENT MODEL IN L-UTSOI 2/2

Initially this model comes from PSP [1], where the integration over energy is skipped to obtain explicit function by assuming that all electrons have the same kinetic energy.

\[
J_g(x) = J_0 \int_0^\infty D_{(E,x)} \cdot F_s_{(E,x)} \cdot dy \sim J_0 \int_0^\infty D(x) \cdot F_s(x)
\]

where \( D_{(E,x)} \) is the transmission coefficient calculated in the WKB approximation, \( F_s_{(E,x)} \) is the supply function and \( x \) is the position along the channel.

where \( z_g \) is the voltage drop through the gate oxide normalized to the built-in voltage, \( J_0 \) and \( B_0 \) are constant related to the tunneling current.

\[
D(x) = e^{-B_0 \cdot f(z_g)}
\]

\[
f(z_g) = \frac{1 - (1 - z_g)^{1.5}}{z_g} \sim -\frac{3}{2} + G2 \cdot z_g + G3 \cdot z_g
\]

\[
\frac{B}{F_{ox}} \frac{\phi^{1/2} - (\phi_s - qV_{ox})^{1/2}}{\phi_s^{3/2}}
\]

\( G2 (0.375), G3 (0.063) \) is taylor expansion parameter.

In current version of L-UTSOI, this model is derived for "inversion" and "overlap" branch.

Discrepancy observed on gate current is evident for $V_{GS} << 0$ and $V_{DS} >> 0$. We observe 2 different behaviors at low and high $V_{GD}$ values.

We propose to add high electric field component close to Fowler-Nordheim (FN) equation:

$$J_g \sim J_0 \cdot F_{FN}(\chi) \cdot \left( e^{-B_0 \cdot f_{zg}} \right) + F_{NOV} \cdot e^{-B_0 \cdot G_{COVFN} \cdot zg}$$

We introduce 2 more parameters $F_{NOV}$ and $G_{COVFN}$.
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- Conclusions/perspectives
Following the model extraction strategy [1], we have realized a parameter extraction using 28nm FDSOI technology. L-UTSOI is able to model all the features of FDSOI transistor characteristics for any bias configuration, including the case of the strong forward back bias, where two channels take place at the front and back interfaces of the thin silicon body.

Both front and back channel modulates capacitance

Substrate depletion modulates CGB (here NSUB>0)

[1] L-UTSOI 102.4.0 user's manual.
CORNERS DEVICES: DEVICE 1 AT AMBIENT TEMPERATURE

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Dots: hardware
Lines: model
CORNERS DEVICES: DEVICE 1 VERSUS TEMPERATURE

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Dots: hardware
Lines: model
CORNERS DEVICES: DEVICE 6 AT AMBIENT TEMPERATURE

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Dots: hardware
Lines: model
CORNERS DEVICES: DEVICE 6 VERSUS TEMPERATURE

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Dots: hardware
Lines: model

\(T^* = 40^\circ\text{C to } 125^\circ\text{C}\)
CORNERS DEVICES: DEVICE 9 AT AMBIENT TEMPERATURE

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Dots: hardware
Lines: model
Corners Devices: Device 9 Versus Temperature

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Dots: hardware
Lines: model

\[ T^* = -40 \text{ to } 125 \ ^\circ C \]

\[ V_{DS} = 0 \text{ V} \]

\[ V_{BS} = 0 \text{ V} \]

\[ V_{DS} = 0 \text{ V} \]

\[ V_{BS} = 0 \text{ V} \]
CORNERS DEVICES: DEVICE 12 AT AMBIENT TEMPERATURE

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CORNERS DEVICES: DEVICE 12 VERSUS TEMPERATURE

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Dots: hardware
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V_{BS} = -2 to 2 V
V_{GS} = 0 to V_{dd}

Dots: hardware
Lines: model
L-UTSOI MODEL EXTRACTION USING 28NM FD-SOI TECHNOLOGY: IV ILLUSTRATION ON SHORT DEVICE

**This accuracy is obtained thanks to the activation of backplane depletion, quantum confinement, mobility distinction between front & back channels and physical effects detailed in previous parts.**
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Conclusions/perspectives
CONCLUSIONS / REMARKS

• We have presented the recent improvements brought to L-UTSOI model to improve its accuracy and predictability in moderate and weak inversion regions.

• By comparison with experimental data, we have illustrated the enhanced accuracy obtained on gm/Id thanks to the introduction of source/drain depletion effect, on the output conductance thanks to the implementation of the impact ionization effect, and on gate tunneling current, thanks to the adding of a Fowler-Nordheim component.

• L-UTSOI standard model (former Leti-UTSOI 2) is available in all major commercial SPICE simulators (SPECTRE, HSPICE, ELDO, ADS ...).

• Future work is planned in the “whish list” of L-UTSOI Working Group (CMC):
https://si2.org/cmc/
https://si2.org/2020/03/10/lutsol/
Main Reference publications:

- **L-UTSOI 102.4.0 user’s manual.**

  

  

  
  https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6724616

Presentation @ MOS-AK Grenoble 2015


Presentation @ MOS-AK WashingtonDC 2013

Thank you for your attention