LDMOS COMPACT MODELING AND THE PSPHV MODEL

Kejun Xia and Colin McAndrew

MOS-AK Compact Modeling Workshop
at ESSCIRC-ESSDERC 2020 Virtual Educational Event

Sep 15, 2020

SECURE CONNECTIONS FOR A SMARTER WORLD

EXTERNAL

NXP, THE NXP LOGO AND NXP SECURE CONNECTIONS FOR A SMARTER WORLD ARE TRADEMARKS OF NXP B.V.
ALL OTHER PRODUCT OR SERVICE NAMES ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS. © 2020 NXP B.V.

CONTENT

- Brief review of BCD technologies
- LDMOS structure
- LDMOS modeling
- JFETIDG model for the drift region
- PSPHV model (PSP for HV)
- PSPHV model extraction
- Conclusions

HIGH VOLTAGE BCD TECHNOLOGY

Tech

- Bipolar
- Cmos
- DMOS for HV
- OTP
- Flash
- MIM/MOM
- Resistors

Why

- Foundry to re-use baseline IP & Fab
- Huge market

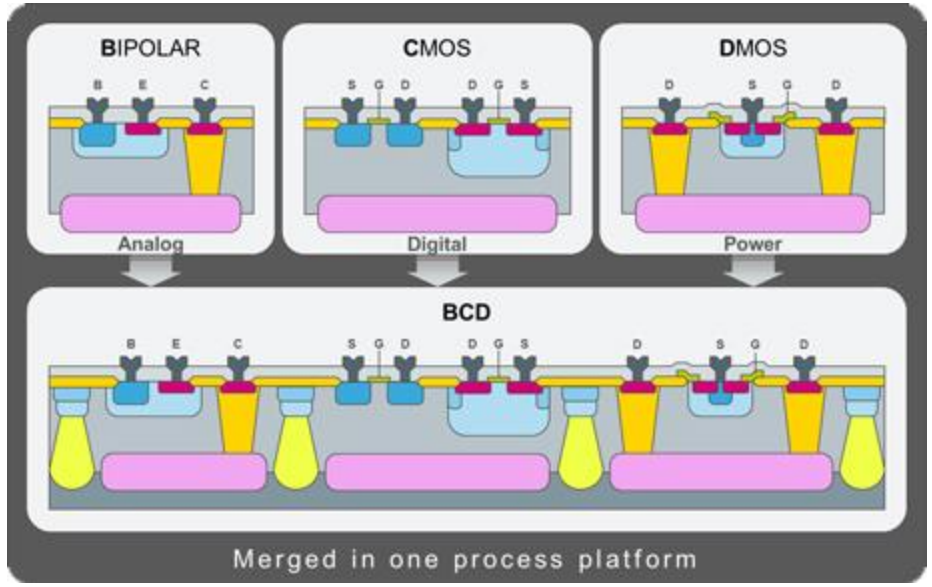
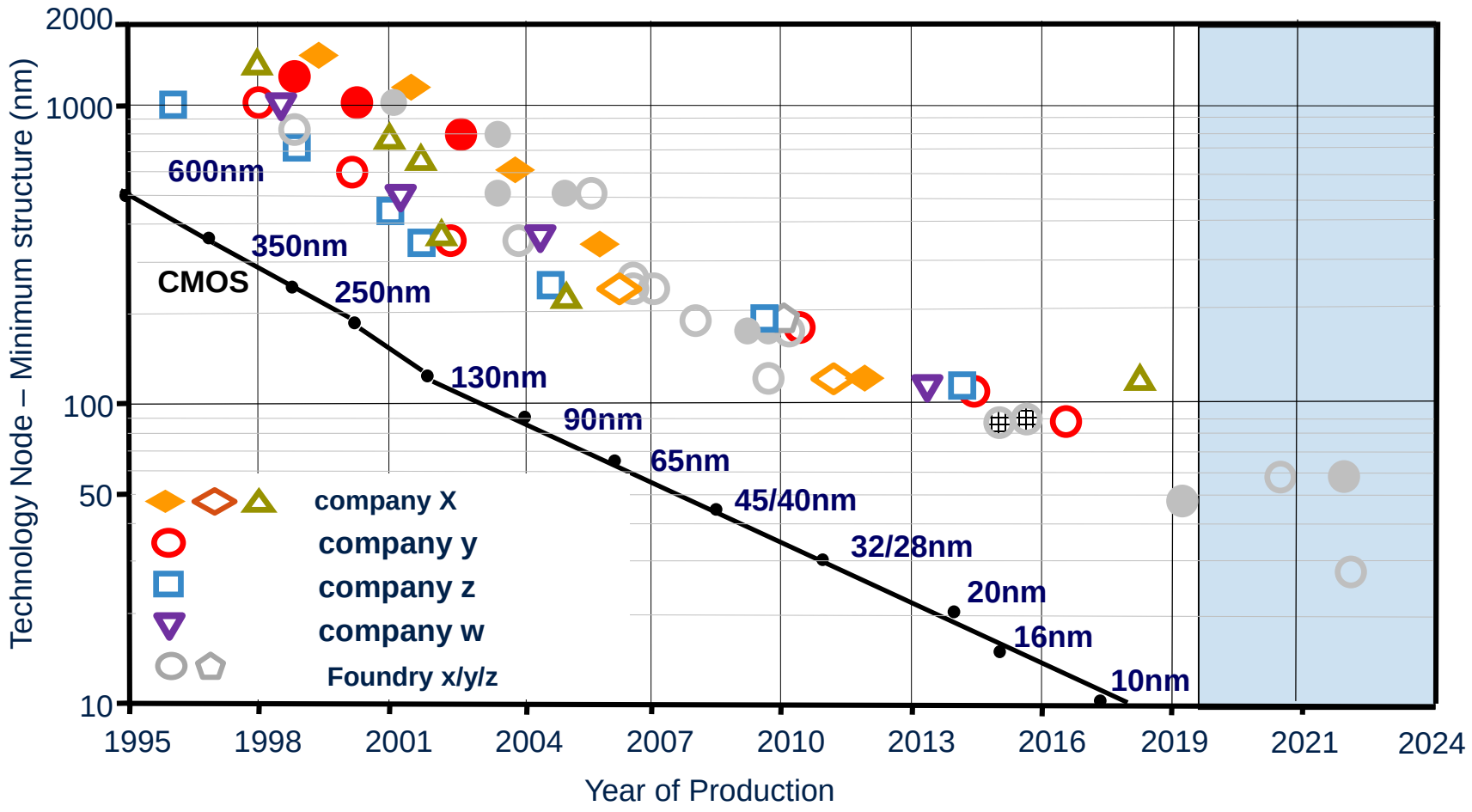


Image From ST web

BCD FOLLOWS BASELINE
ONLY FOUNDRIES BEYOND 90NM



(Full symbol = SOI, empty symbol = bulk)

3.

CONTENT

- Brief review of BCD technologies
- LDMOS structure
- LDMOS modeling
- JFETIDG model for the drift region
- PSPHV model for LDMOS
- PSPHV model extraction
- Conclusions

DMOS AND LDMOS

- DMOS: Double-diffused MOS
  - Current in both lateral and vertical
  - Discrete device
- LDMOS: Laterally-diffused MOS
  - Also known as DEMOS
  - Current in lateral
  - Integrated circuit
  - Key components in BCD

Figure 1: Basic DMOS Structure

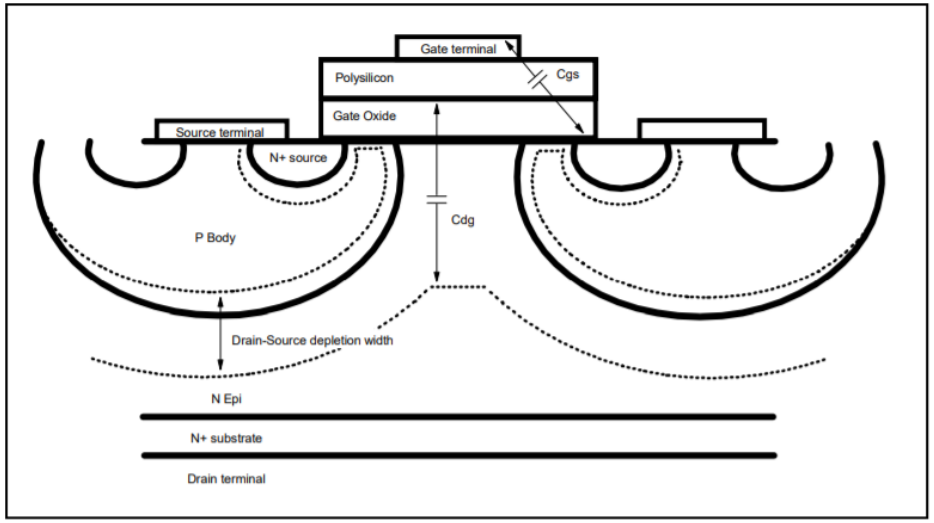
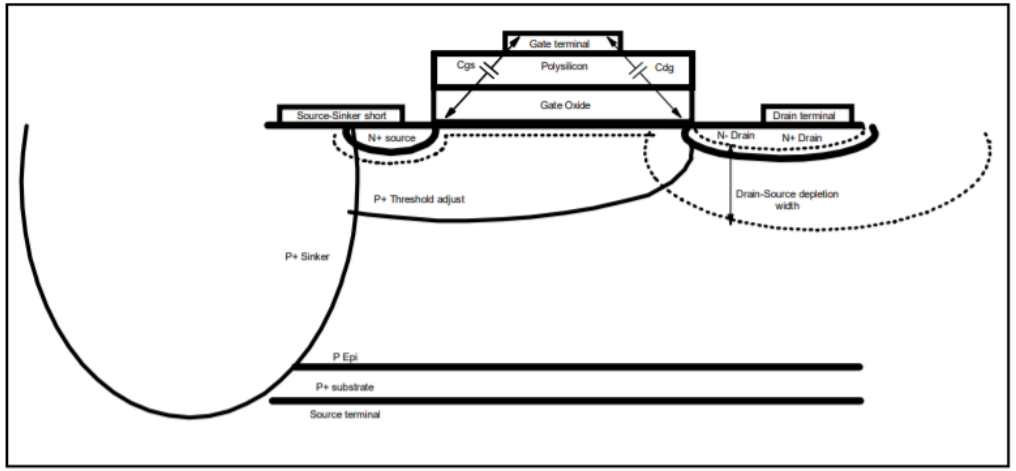


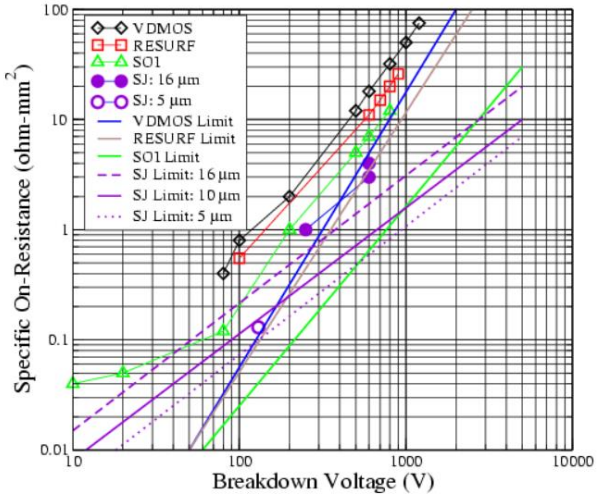
Figure 2: Basic LDMOS Structure



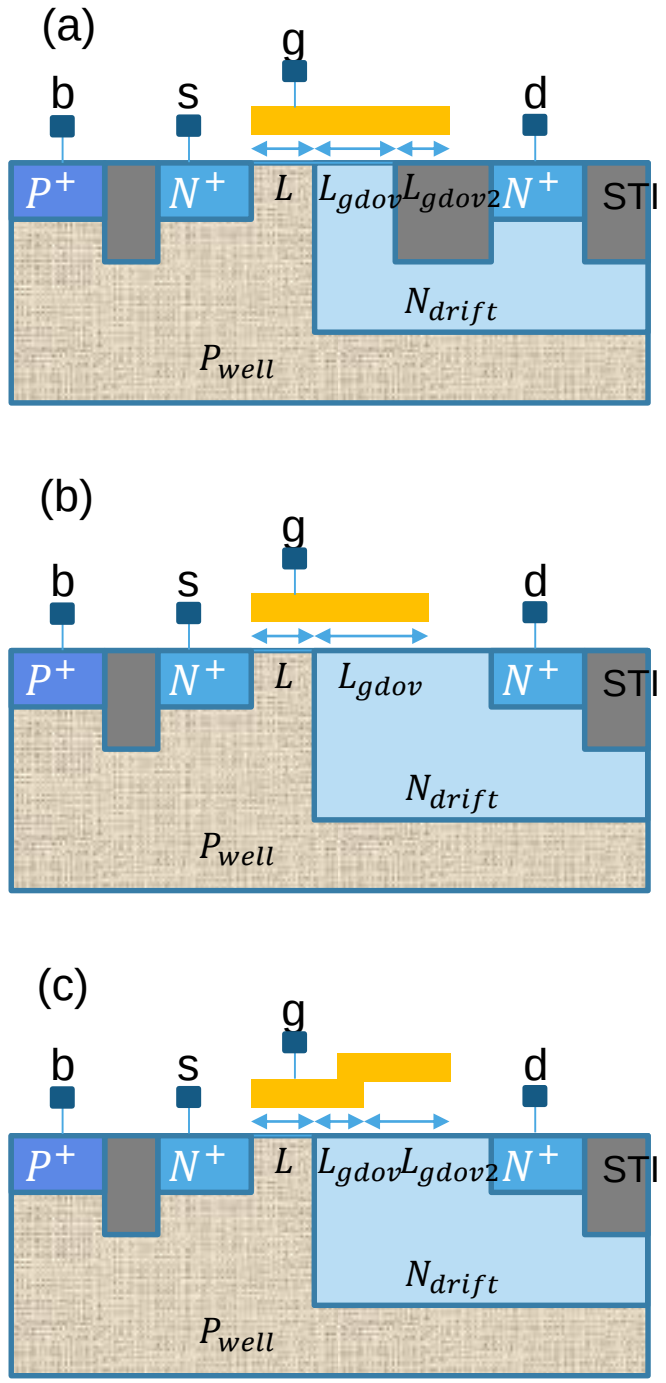
Source https://www.st.com/resource/en/application_note/cd00004124-understanding-ldmos-device-fundamentals-stmicroelectronics.pdf

LDMOS FOM AND STRUCTURES

- The key design parameters for power switch applications
  - Specific on-resistance (Rsp=Ron*A)
  - BV and SOA
  - Power handling capability
  - Reliability (HCI, HCI TDDB, HTRB, etc)
- Device design techniques
  - Field plate design for the drift region
  - Resurf (Reduced surface field)
  - Super junction



Jong M. Park dissertation, 2004, Fig. 3.11



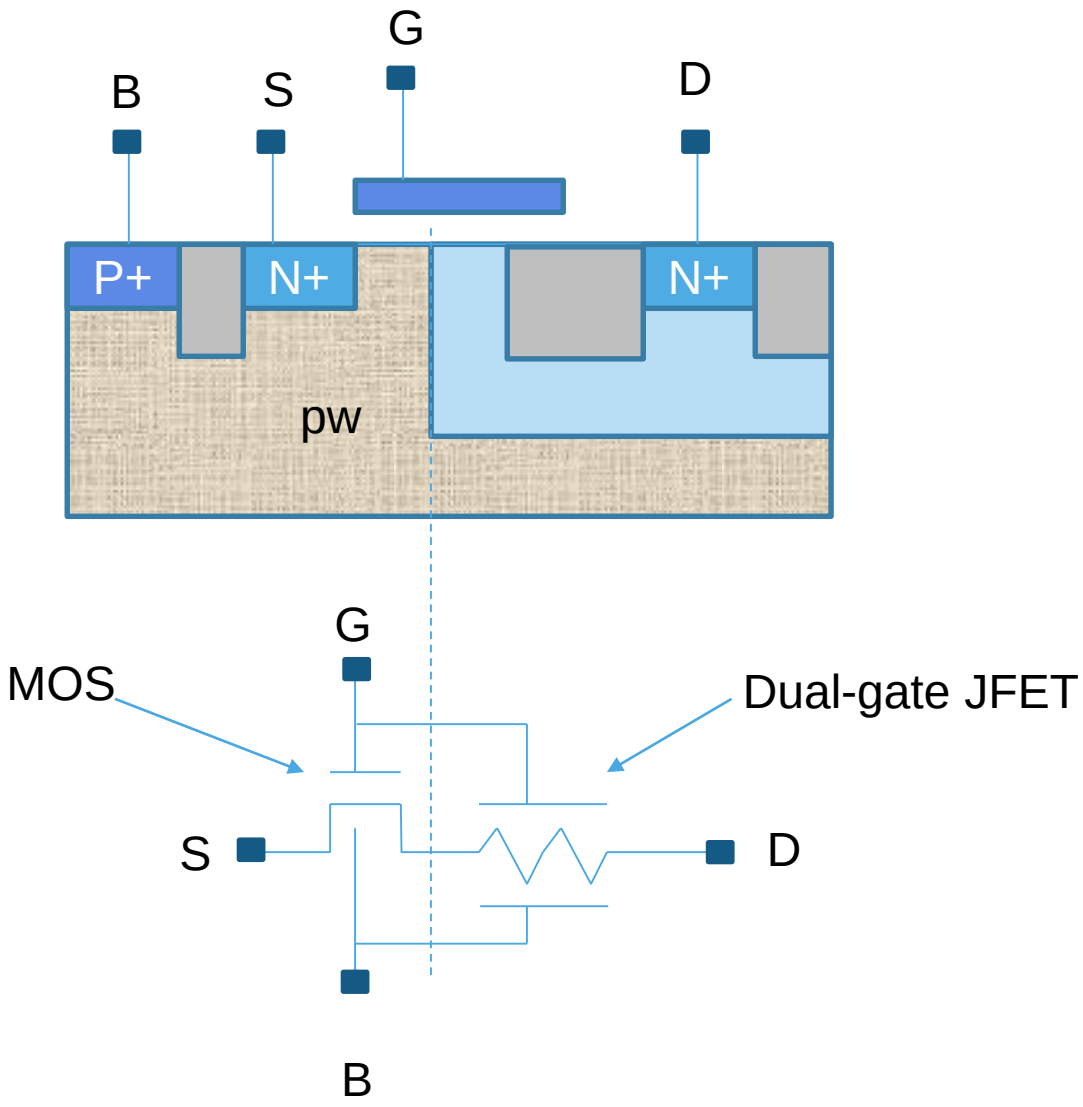
CONTENT

- Brief review of BCD technologies
- LDMOS structure
- LDMOS modeling
- JFETIDG model for the drift region
- PSPHV model for LDMOS
- PSPHV model extraction

LDMOS & ITS EQUIVALENT CIRCUIT

Key characteristics to model

- Drift region resistance
- Quasi-saturation
- Self-heating
- Gate and drain charging
- Diode reverse recovery



LDMOS MODELS

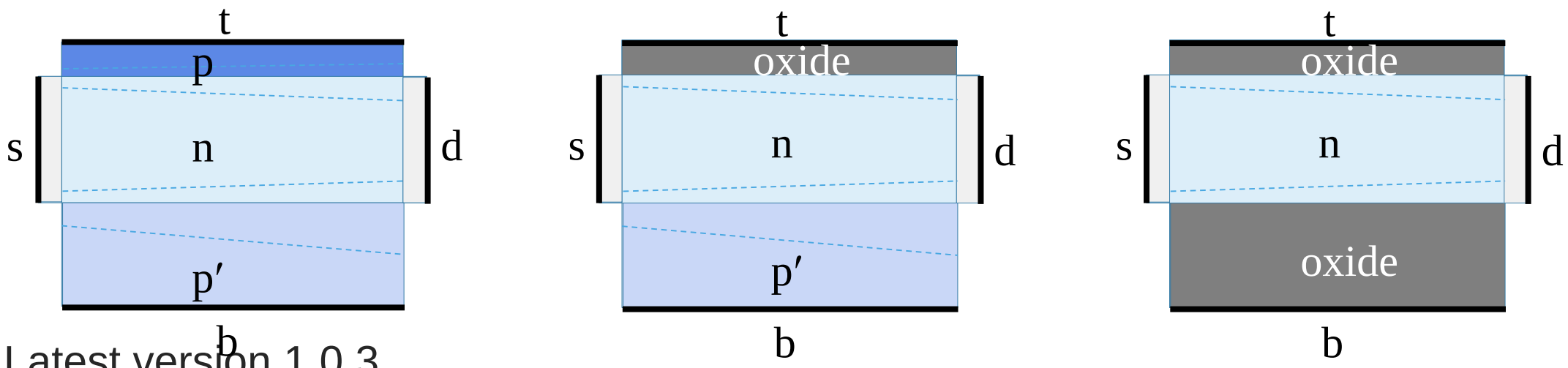
	Subckt based eg: BSIM3+Res	HiSIM_HV	BSIM-HV	PSPHV (This talk)
Openness	Public	CMC standard	Public	Public
DC Core	BSIM3	HiSIM	BSIMBulk	PSP
Drift Cap	Another Cap	Another Cap	Another Cap	Another Cap
Drift Res	Resistor	Bias dependent Res	Bias dependent Res	JFETIDG
Drift avalanche	Non-physical	Non-physical	Not clear	Physical
Drain expansion	No	No	No	Yes
Drain-body reverse recovery	No	Yes	Not clear	Yes
Self heating	No	Yes	Yes	Yes
Compactness	Complicated subckt	Very compact	Very compact	Very compact

CONTENT

- Brief review of BCD technologies
- LDMOS structure
- LDMOS modeling
- JFETIDG model for the drift region
- PSPHV model for LDMOS
- PSPHV model extraction
- Conclusions

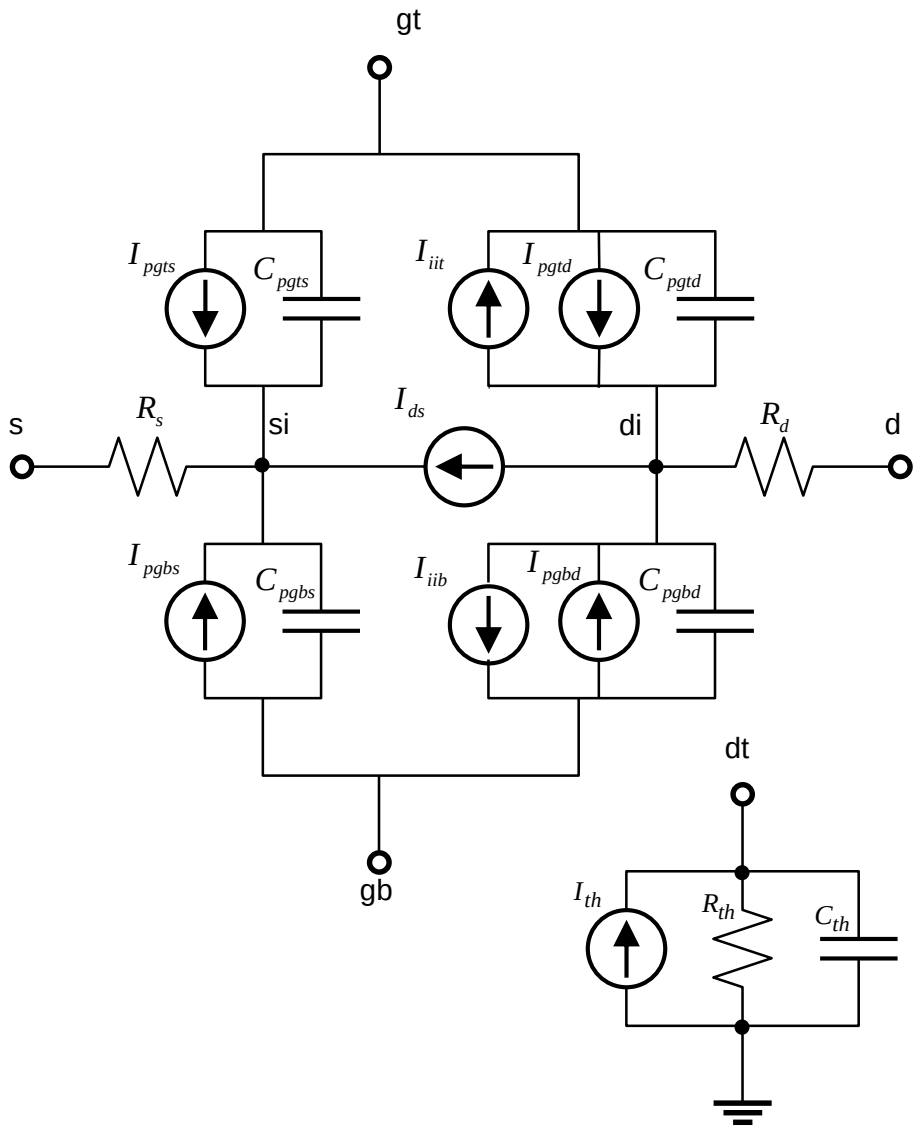
JFETIDG MODEL OVERVIEW

- JFETIDG: Model for junction FETs with Independent Dual Gates
  - Generalized to include both MOS gate and pn-junction gate



- Latest version 1.0.3
- Public
  - Manual IEEE TED 2018, Vol. 65, No. 2 https://ieeexplore.ieee.org/document/8249759
  - Verilog-A Code on Purdue NEEDS website https://nanohub.org/publications/173/2
    - 1009 downloads
  - Included in public Simkit 5.2, integrated into Cadence simulator spectre

JFETIDG EQUIVALENT CIRCUIT



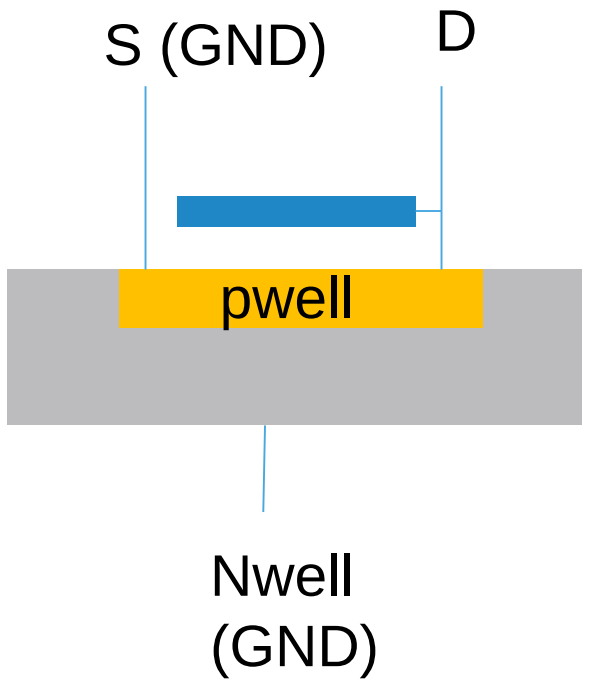
- Case I: 2 pn junction gates
  - Dual-gate JFET per si
  - Collector resistance of 4-terminal vertical bipolar transistors
- Case II: 1 pn junction + 1 MOS gates
  - Resistors (diffused or polysilicon) with metal shields
  - Drift region of LDMOS transistors with field plates
- Case III: 2 MOS gates
  - Junctionless MOSFETs

JFETIDG KEY MODEL FEATURES

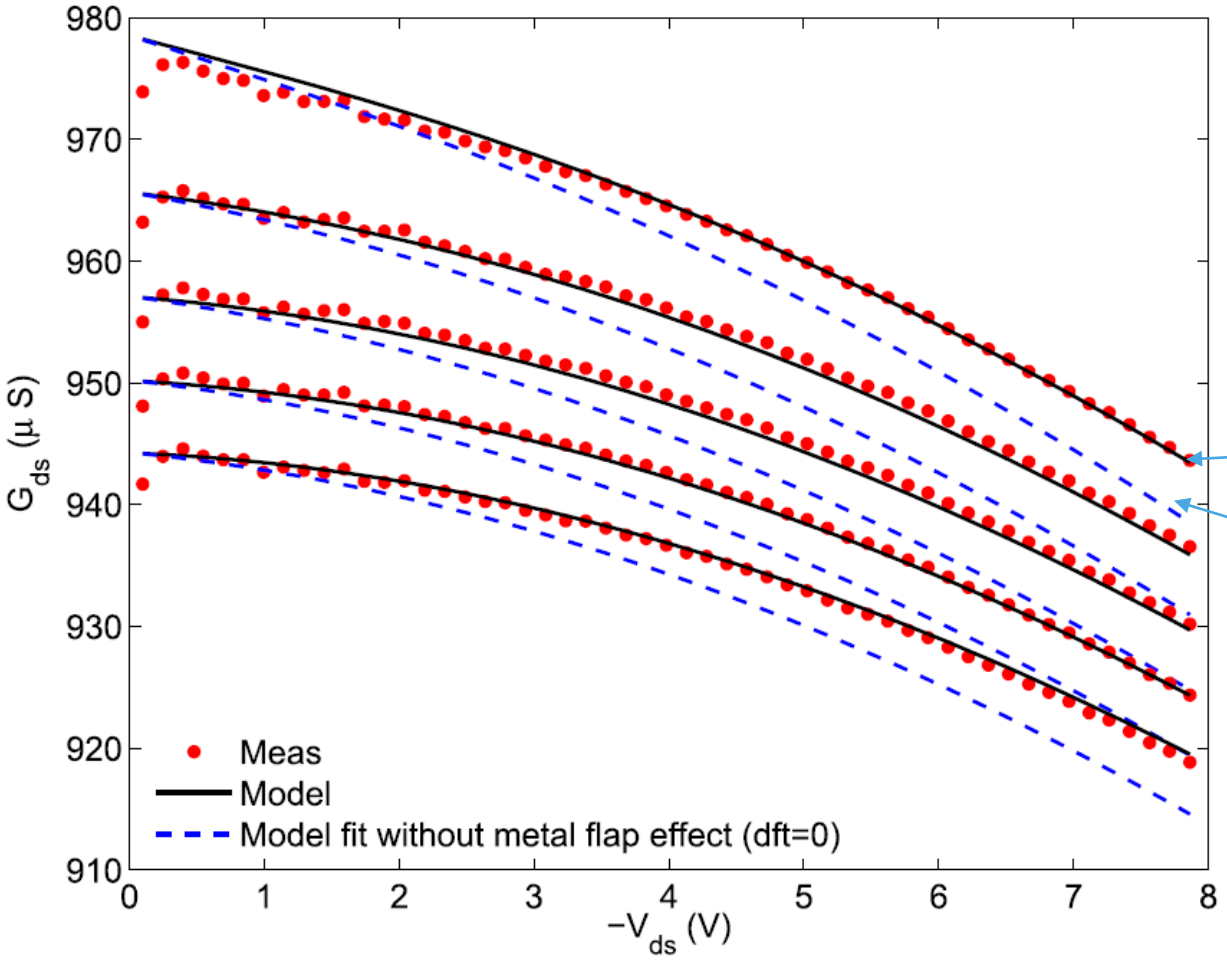
- Support of both depletion mode and enhance mode channels.
- Full geometry and temperature dependencies.
- Global and local statistical variations.
- Coupling between two gates.
- Velocity saturation.
- Drain Induced Barrier-Lowering effect (DIBL).
- Channel Length Modulation effect (CLM).
- Impact ionization (i.e. weak avalanche).
- Thermal and flicker noise from channel current.
- Self-heating, modeled via an RC thermal network.

EXAMPLE: PWELL RESISTOR WITH METAL SHIELD

- 1 pn junction + 1 MOS gates



Gds=Ids/Vds



JFETIDG

This is equivalent to R3 model which cannot fit Vg and Vd dependence simultaneously due to metal shield.

CONTENT

- Brief review of BCD technologies
- LDMOS structure
- LDMOS modeling
- JFETIDG model for the drift region
- PSPHV model for LDMOS
- PSPHV model extraction
- Conclusions

PSPHV MODEL OVERVIEW

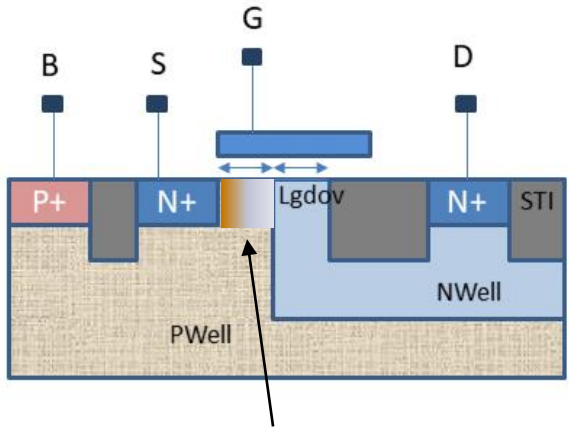
- PSPHV: PSP based HV Model for LDMOS

- Latest version 1.0.4

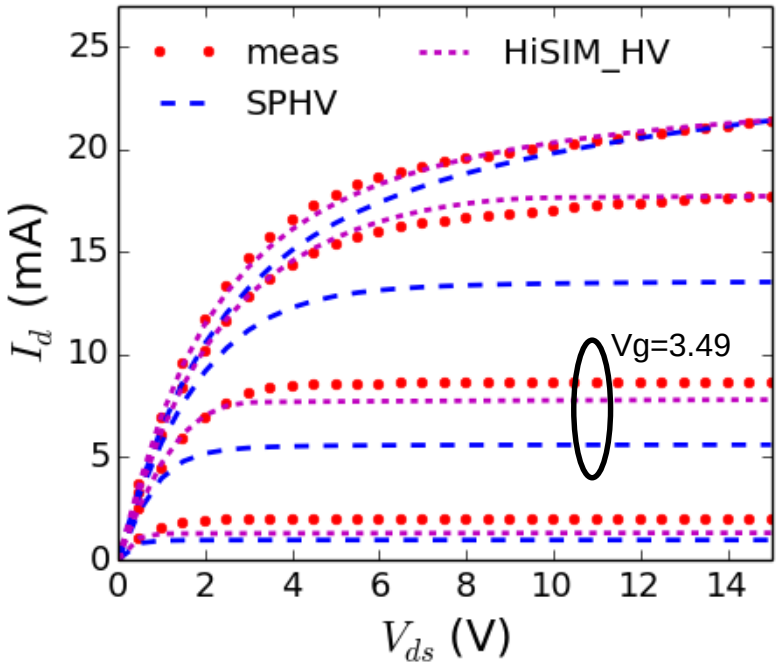
- Public
  - Introduction: IEEE TED 2018, Vol. 66, No. 12, https://ieeexplore.ieee.org/document/8886601
  - Extraction: IEEE J-EDS 2020 (OA), https://ieeexplore.ieee.org/document/9146541
  - Verilog-A Code on Purdue NEEDS website https://nanohub.org/publications/347/2
  - Will be included in public Simkit 5.3 and integrated into Cadence simulator spectre

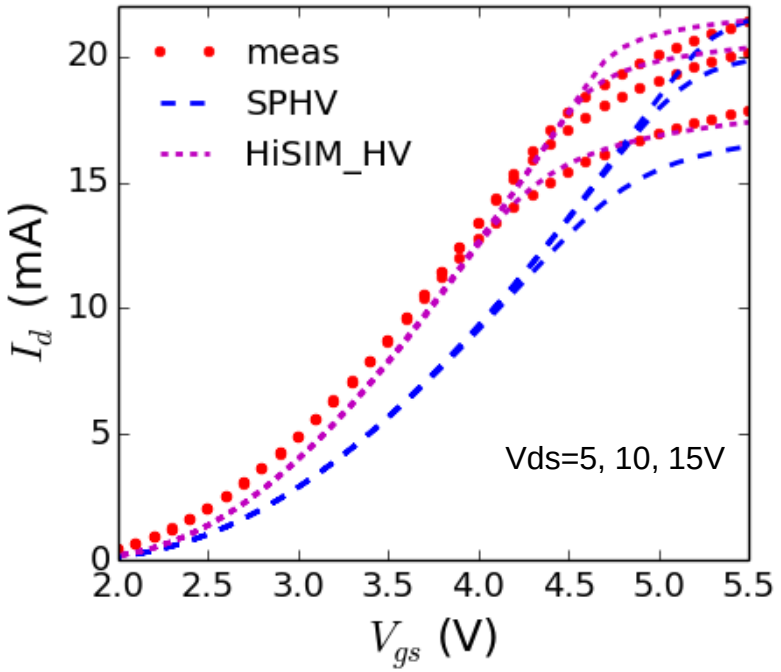
MOTIVATION OF PSPHV

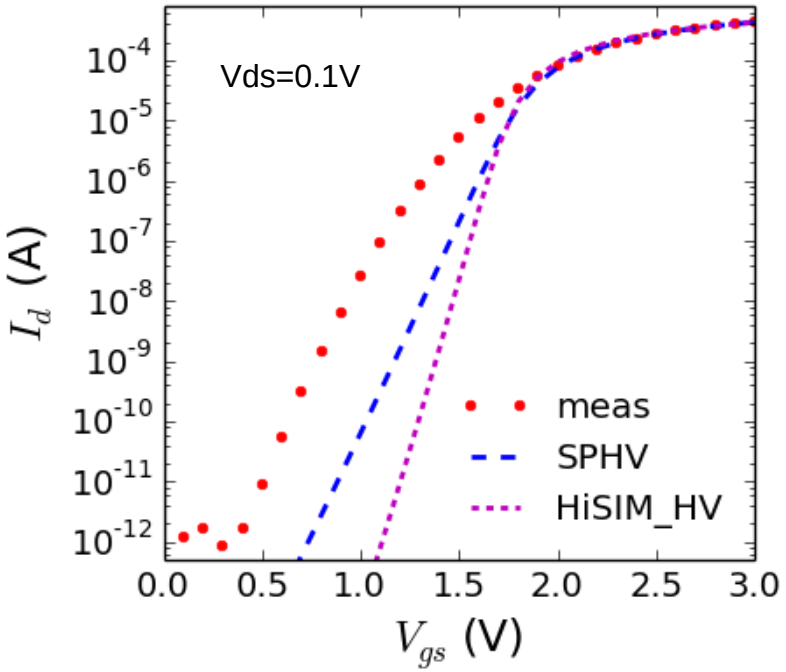
- LDMOS naturally has non-uniform lateral channel doping (out-diffusion, halo doping)
- Existing surface potential based models such as SPHV and HiSIM_HV assume uniform doping in the core model formalism
- We find modeling difficulties associate with this
  - Vdsat and Idsat are under-estimated
  - Gradual turn-off behavior in moderate and weak inversion cannot be modeled accurately



non-uniform doping



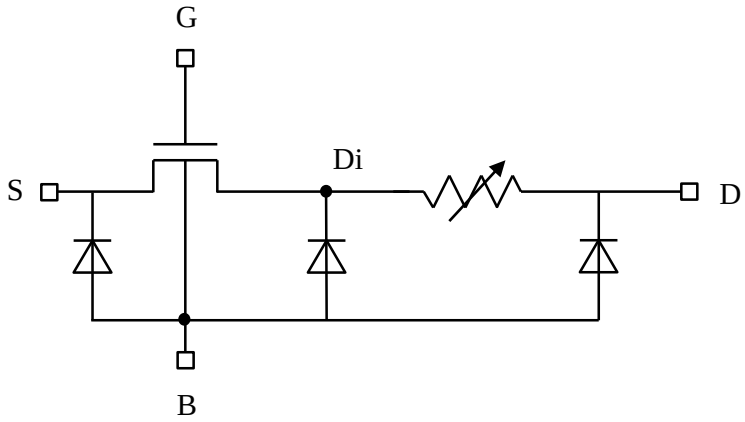


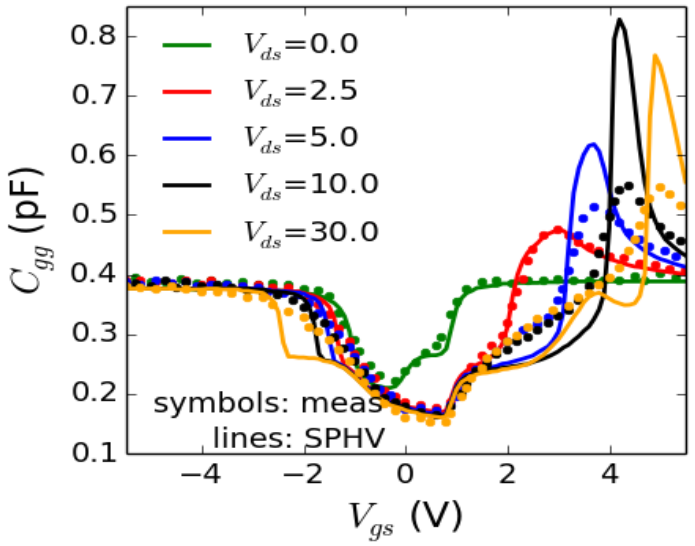


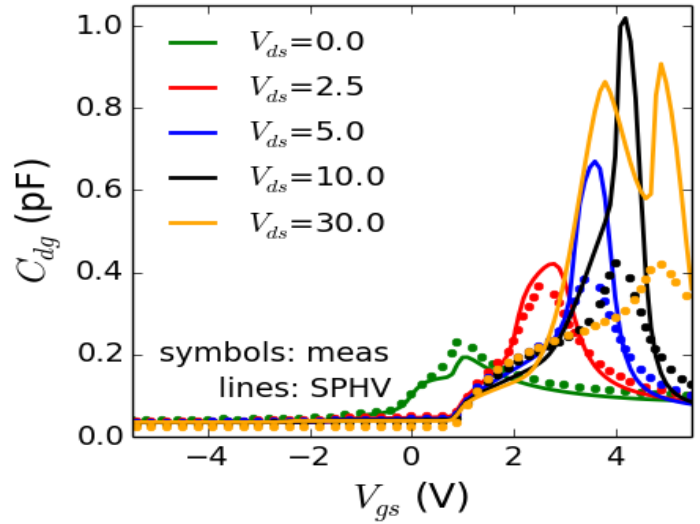
(data on this page are from device A)

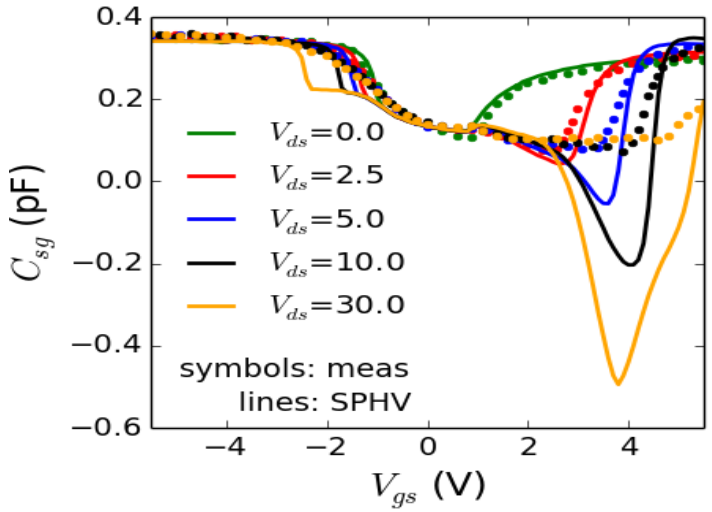
MOTIVATION OF PSPHV CONT'D

- LDMOS is typically modeled as a MOS transistor in series with a variable resistor
- Modeling issues
  - When Vgs is low, MOS transistor is off, V(Di, S)=V(D,S)
    - This is completely unphysical as gate oxide cannot handle Vdmax
    - The drift region is fully depleted, no longer a resistor
  - When Vgs increases, MOS transistor is on, V(Di,S) quickly decreases to very low voltage
    - Such rapid change induces spikes in capacitance





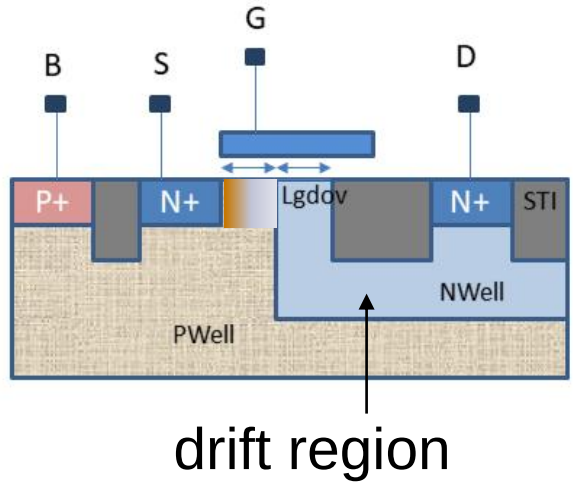


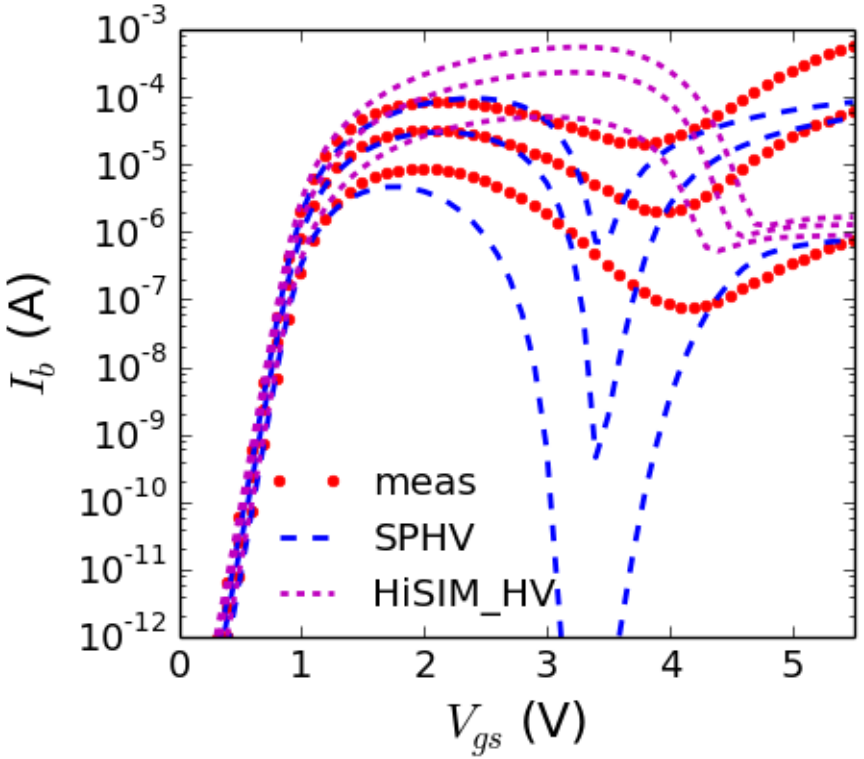


(data on this page are from device B)

MOTIVATION OF PSPHV CONT'D

- Kirk effect: The drift region is modulated by current. When current exceeds a threshold value, the peak E position moves towards the end of drift region.
- The avalanche current in the drift region should capture such effect. However, this is not done in current models.





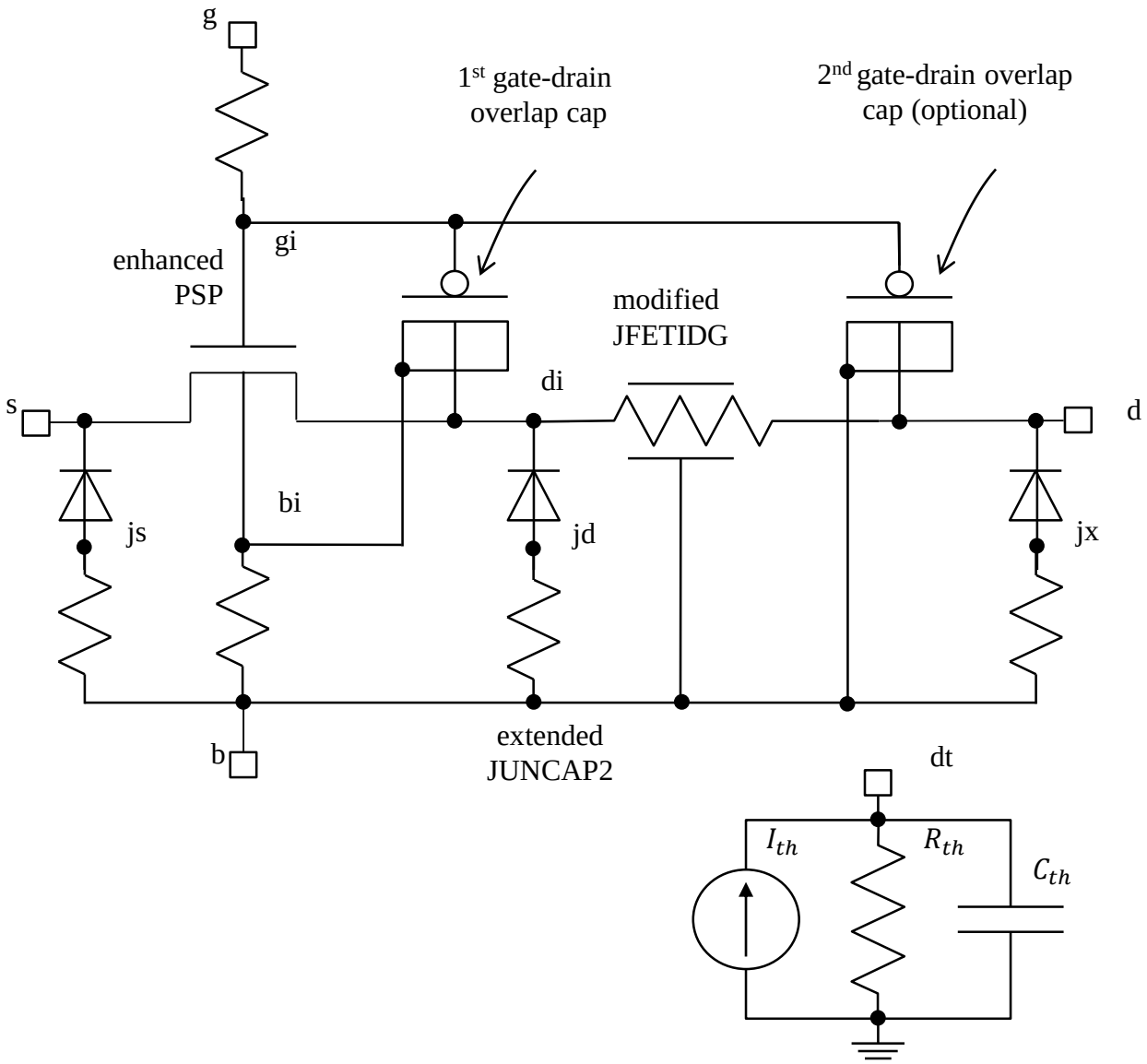
Vds=20,28,36V

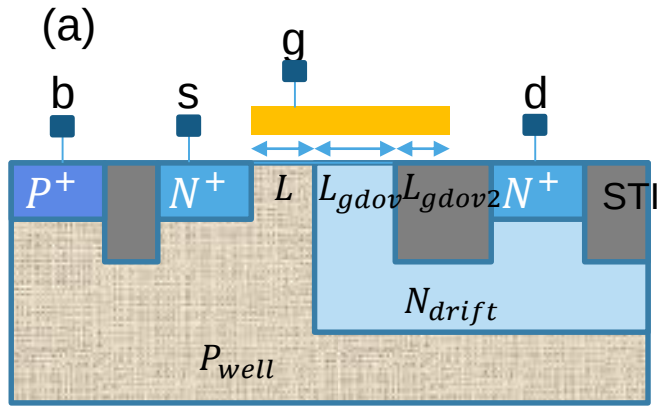
(data on this page are from device B)

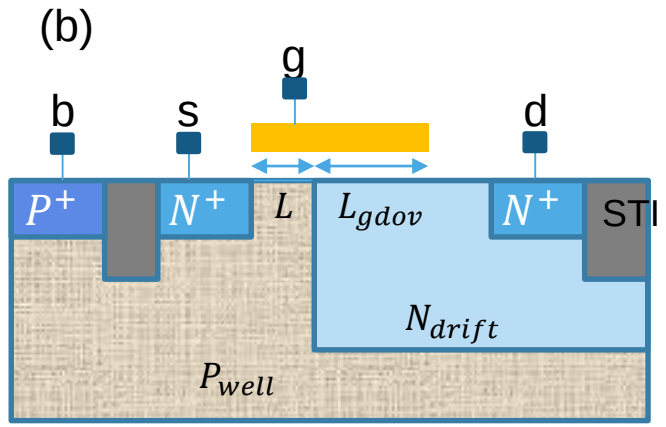
PSPHV KEY MODEL FEATURES

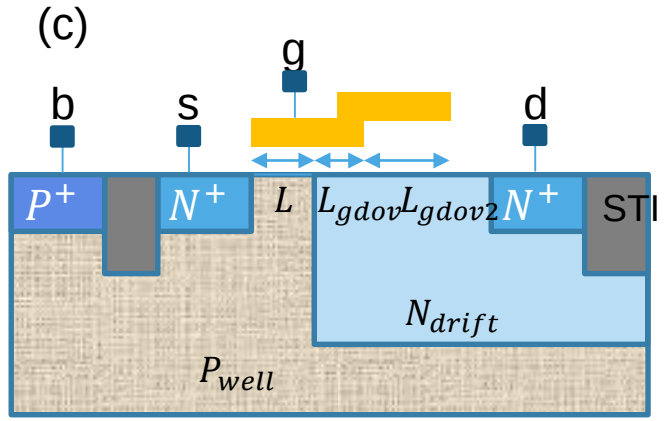
- All features covered by PSP model (W and L scalable)
- Models nonuniform lateral doping
- Models gradual channel turn-on
- Quasi-saturation
- Avalanche current model
- Sub-vt kink
- Self-heating
- As an option, can remove unphysical spikes in capacitance
- As an option, can model the second field plate as a MOS
- As an option, can include reverse recovery modeling for the junction diodes

PSPHV EQUIVALENT CIRCUIT









VDSI SCALING TECHNIQUE

- Scale Vdsi =V(Di,S) to address the Vdsat and Idsat under-estimation issue
- First, scale Vdsi down by a factor γ
- Then use PSP to calculates Ids
- Finally, scale Ids up by the factor γ

Without scaling

$$I_{ds} = \beta\left(V_{gt} - \alpha V_{dsi}/2\right)V_{dsi}$$

body factor

With scaling

$$I_{ds,scaled} = \beta\left(V_{gt} - \alpha(V_{dsi}/\gamma)/2\right)(V_{dsi}/\gamma)\cdot\gamma$$

$$= \beta\left(V_{gt} - (\alpha/\gamma)V_{dsi}/2\right)V_{dsi}$$

body factor scaled down by γ to account the lower doping level towards drain end

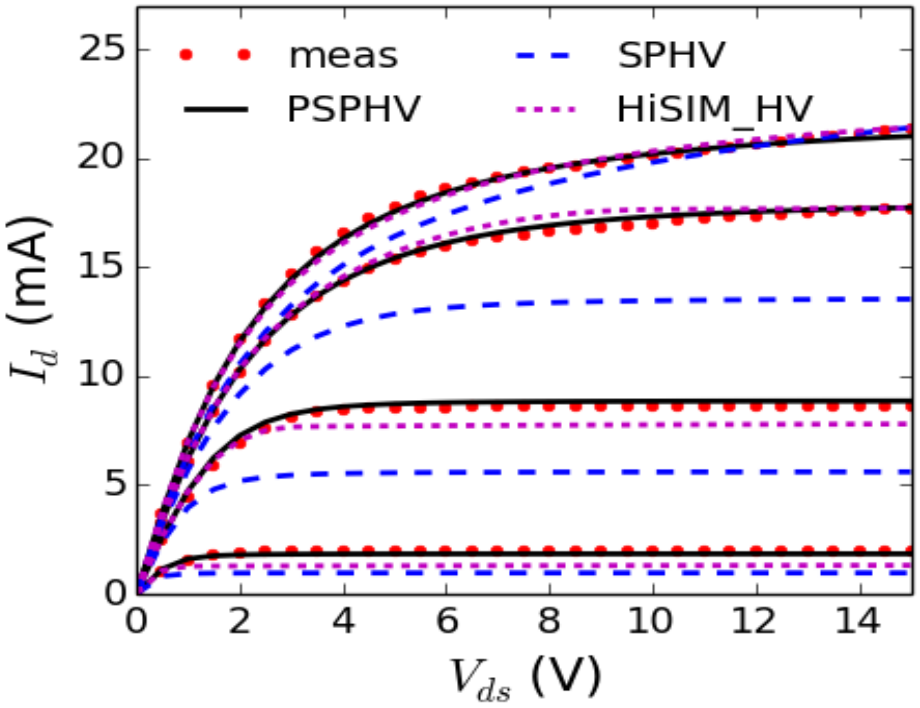
Consequently

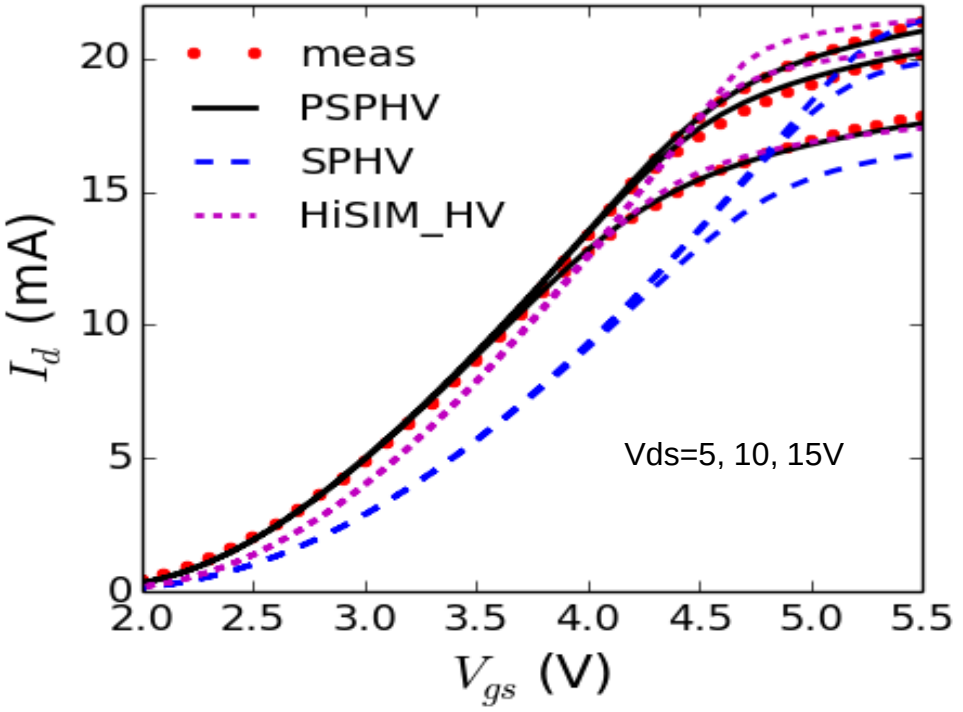
$$V_{dsat,scaled} = \gamma V_{gt}/\alpha = \gamma V_{dsat}$$

$$I_{dsat,scaled} = \gamma I_{dsat}$$

VDSAT AND IDSAT IMPROVEMENT

Both idvd and idvg curves can be accurately fitted.

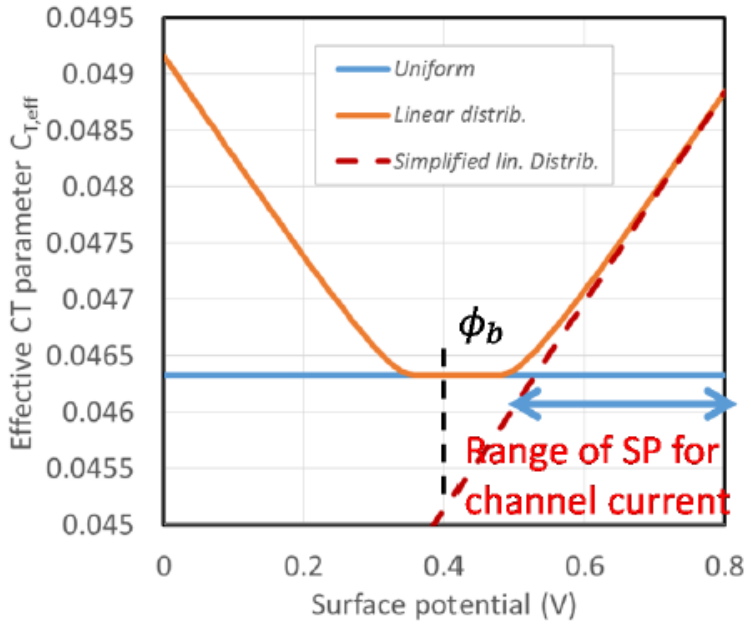




(data on this page are from device A)

CTG IN PSP FOR GRADUAL CHANNEL TURN OFF

- PSP 103.6 introduced gate dependent interface charge CTG to improve gm/id modeling. We found it can also be used to model gradual channel turn-off.

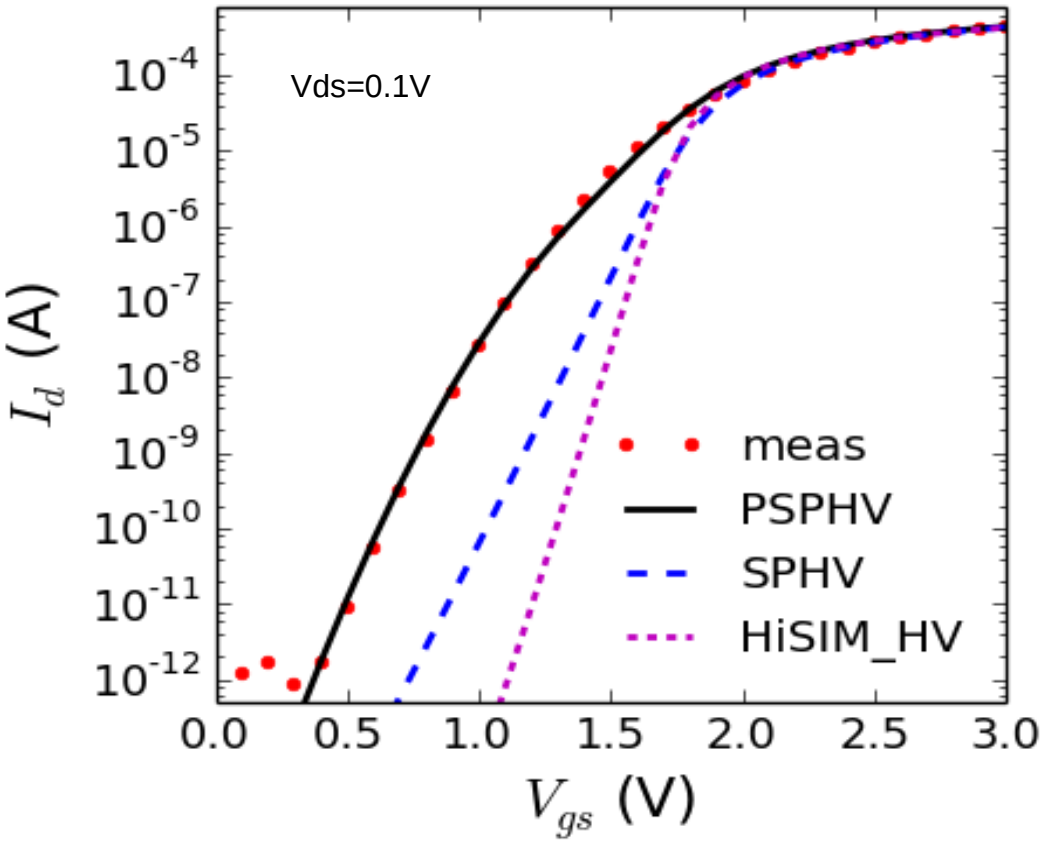


$$C_{T,eff}(\psi_s) = CT \cdot e^{\left(CTG \cdot \frac{T_{KD}}{T_{KR}} \left(\frac{\psi_s}{\phi_T} - (1+CTB)\frac{\phi_b}{\phi_T}\right)\right)}$$

CT modulates sub-vt slope.
CTG then makes the slope bias dependent.

Ref: Sebastien Martinie et. al, “new physical insight for analog application in PSP bulk compact model”. SISPAD 2018.

GRADUAL CHANNEL TURN OFF NOW MODELED



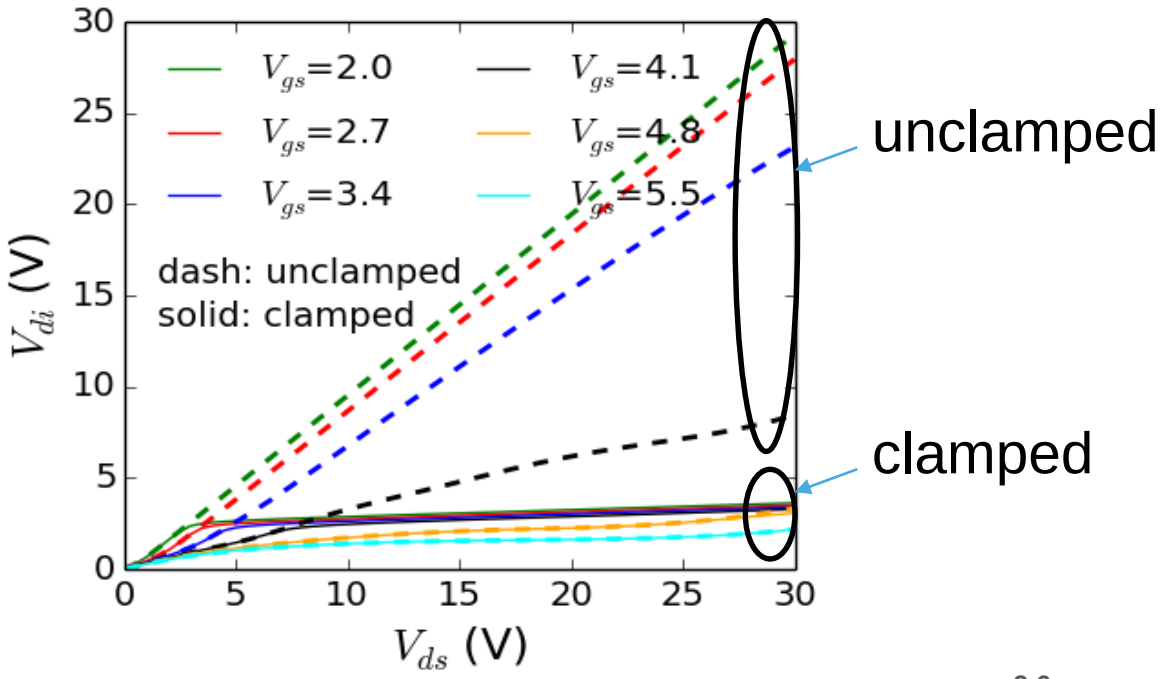
(data on this page are from device A)

VDI CLAMPING FOR CAPACITANCE SPIKE ISSUE

- For a good LDMOS with Vgmax=5V, Vdi (=V(Di,S)) does not exceed 5V because of depletion in the drift region.
- Not easy to model the lateral depletion effect in compact model context.
- Instead, we empirically clamp Vdi by exponentially increasing the drift region resistance when Vdi exceeds certain value.

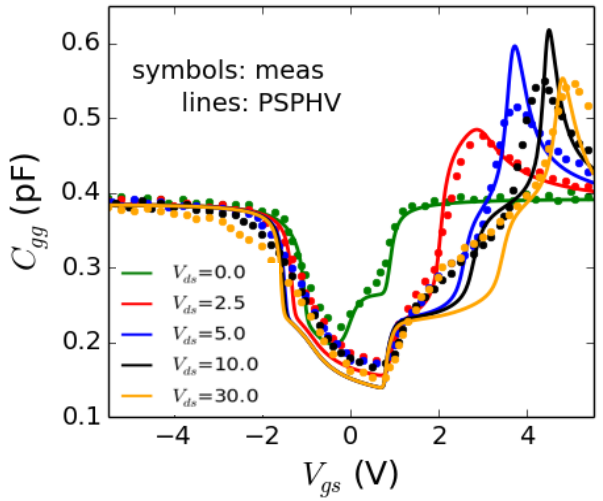
$$I_{dr,clamped} = I_{dr} \Big/ \left[1 + exp\left(\frac{V_{di} - V_{dicl}}{V_{sm}}\right)\right]$$

$$V_{dicl} = V_{di0} + K_{Vdi0} V_{ds}$$

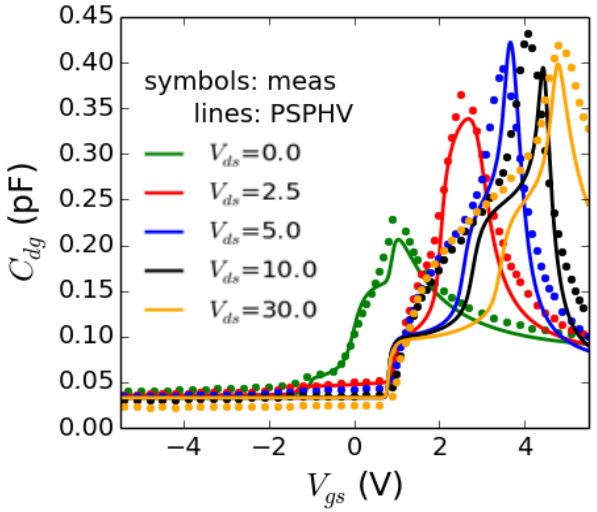


CAPACITANCE IMPROVEMENT – SPIKE REMOVED

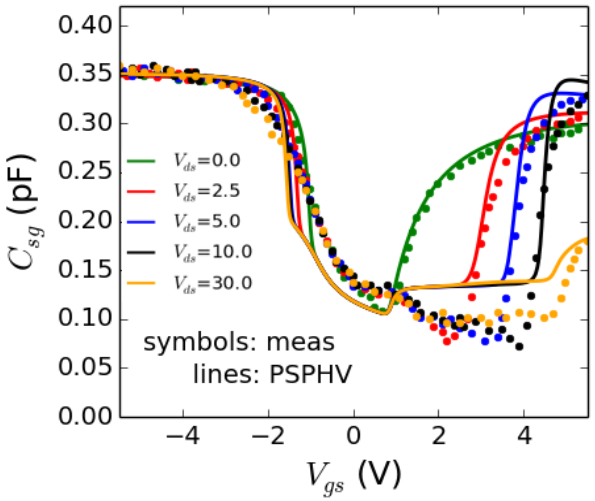
PSPHV Cgg



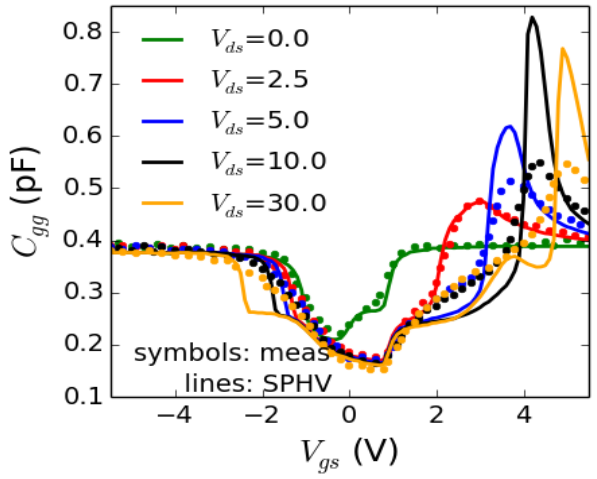
PSPHV Cgd



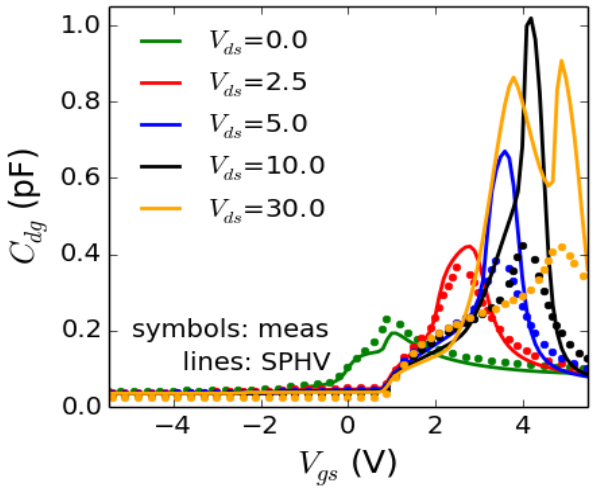
PSPHV Csg



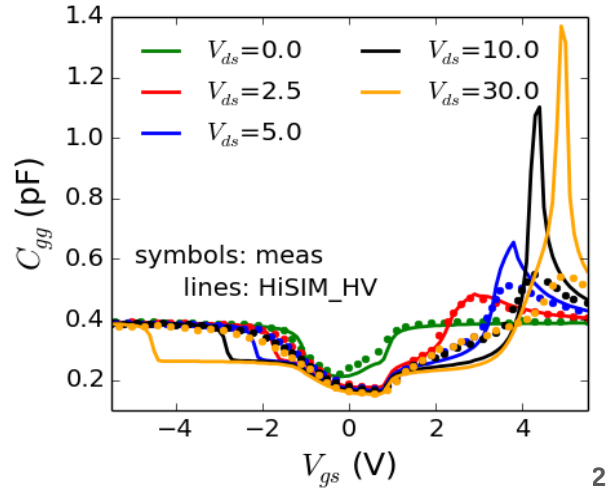
SPHV Cgg



SPHV Cgd



HiSIM_HV Cgg



IMPROVED AVALANCHE MODEL IN CHANNEL REGION

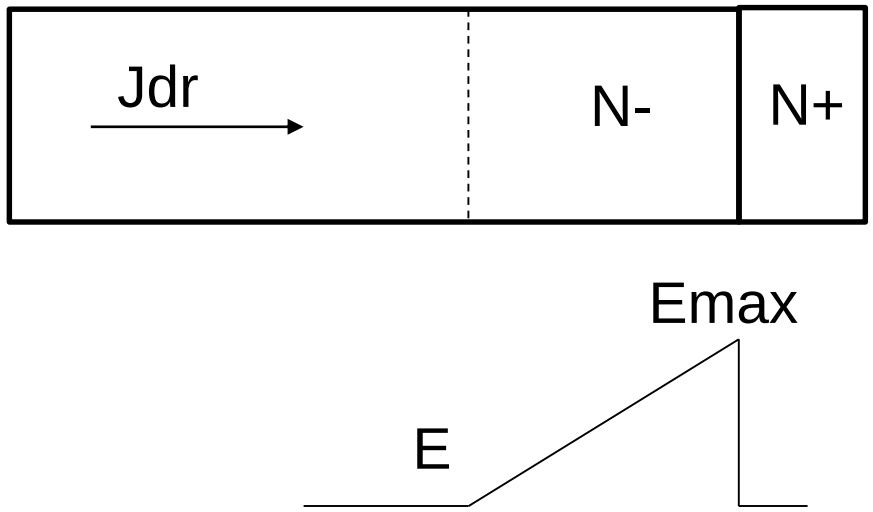
$$I_{avl} = I_{ds}\left[\alpha \cdot \Delta V \cdot exp\left(\frac{-\beta}{\Delta V}\right)\right]$$

In channel region, we do not use Vdsi as in PSP, but the following

$$\Delta V = V_{ds} - (A_3 + C_{A3}V_{ds})V_{dsat,MOS}$$

IMPROVED AVALANCHE MODEL IN DRIFT REGION

When Jdr>Jhc, Kirk effect happens



ΔV in avalanche equation is essentially Emax.

Ignore the built-in potential, we have

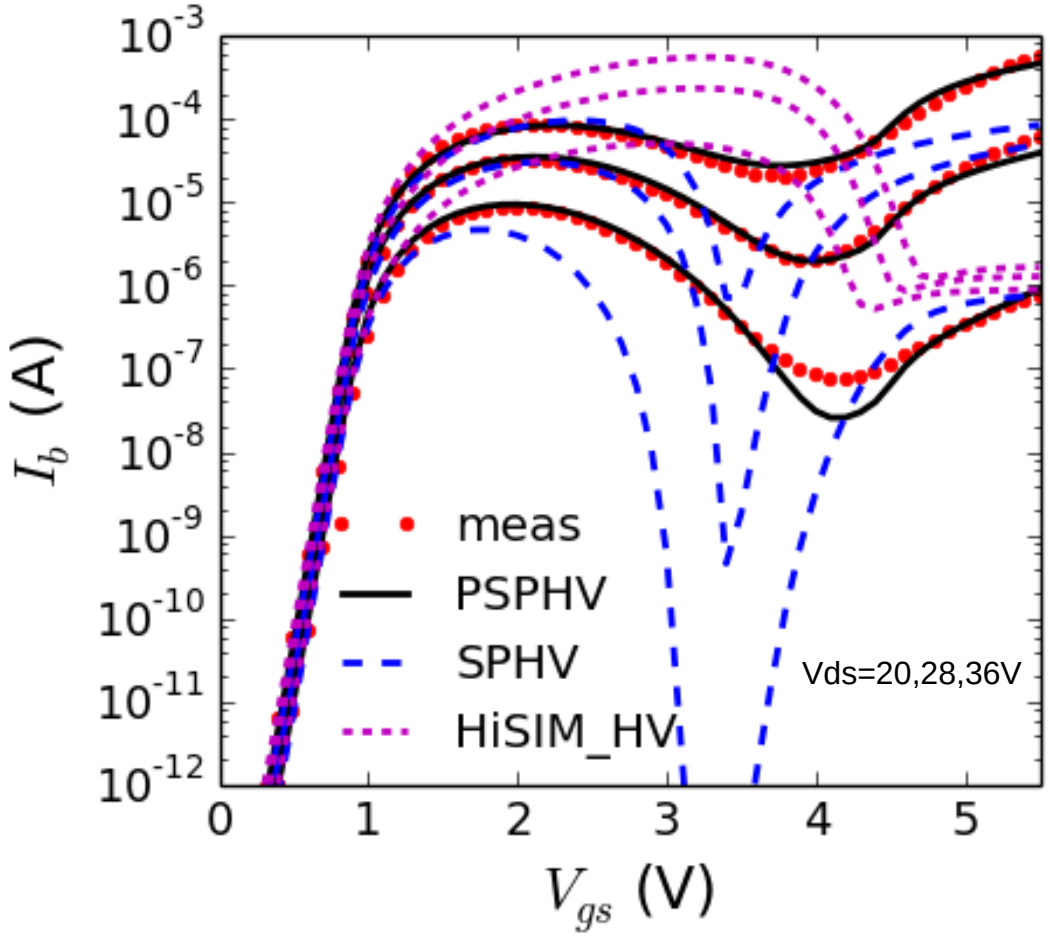
$$\mathrm{n} = \frac{J_{dr} - J_{hc}}{qV_{sat}}$$

$$E_{max} = \sqrt{\frac{2nV_{dr}}{\varepsilon_{si}}} = \sqrt{\frac{2(J_{dr} - J_{hc})V_{dr}}{q\varepsilon_{si}V_{sat}}}$$

Therefore, we model with the following

$$\Delta V = \left[Maxa\left(\frac{I_{dr}}{W} - J_{hc}, 0, \frac{J_{hc}}{1000}\right) \cdot V_{dr} \right]^{m}$$

IMPROVED AVALANCHE MODEL

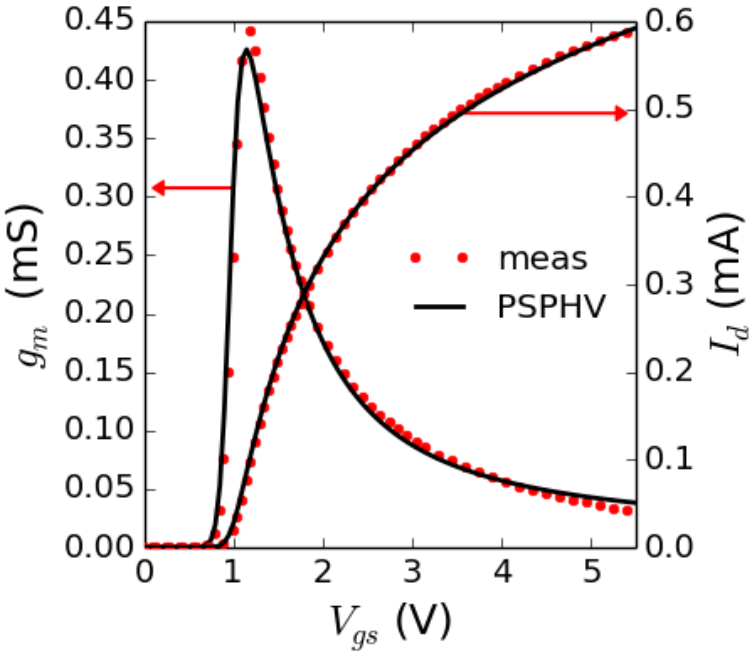


(data on this page are from device B)

OTHER FITTINGS FOR THE SAME DEVICE

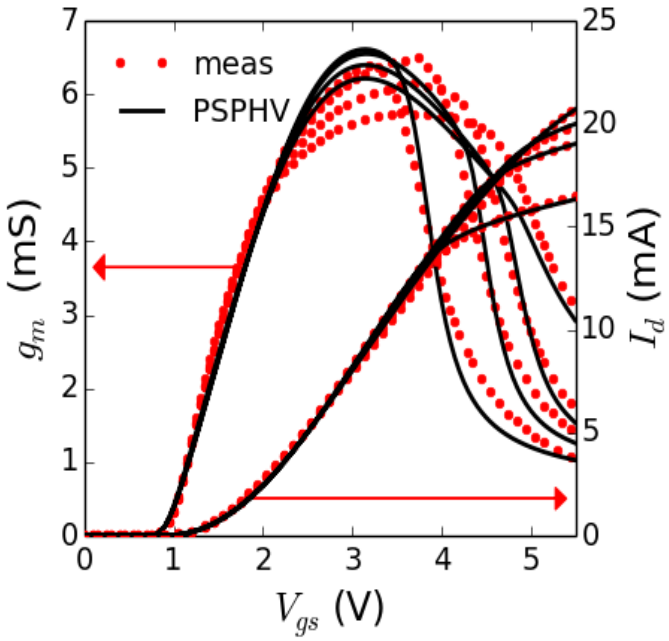
Idvg_lin

Vds=0.1V



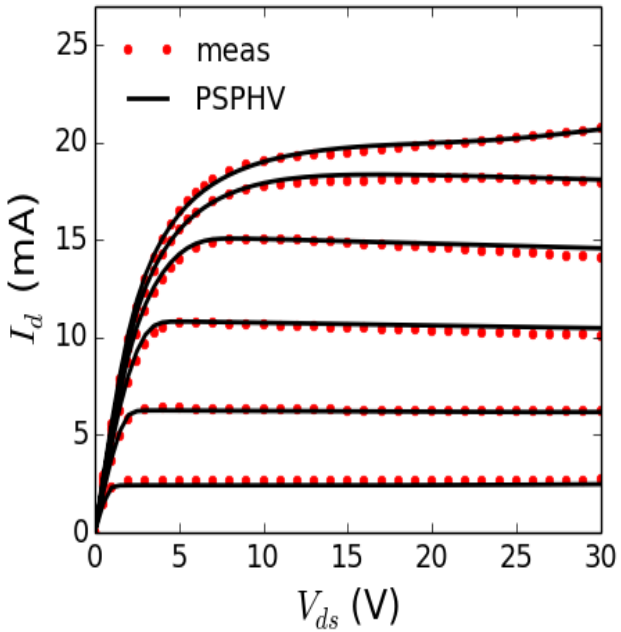
Idvg_sat

Vds=5,10,20,30V



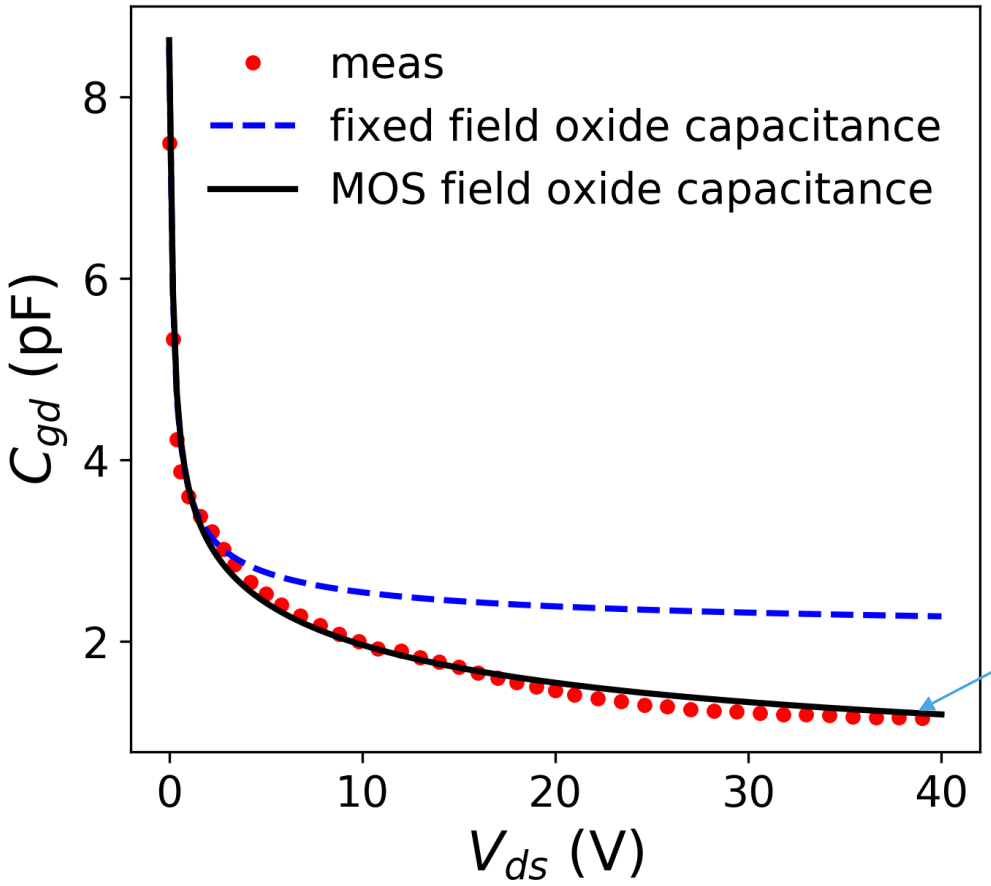
Idvd

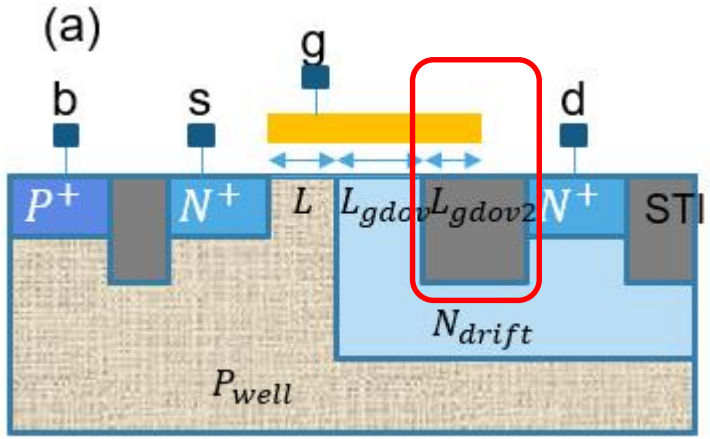
Vgs=2 to 5.5 by 0.7



(data on this page are from device B)

CDG IMPROVEMENT USING 2ND GATE-DRAIN OVERLAP CAPICATOR





Using the 2nd gate-drain overlap cap model significantly improves Cdg

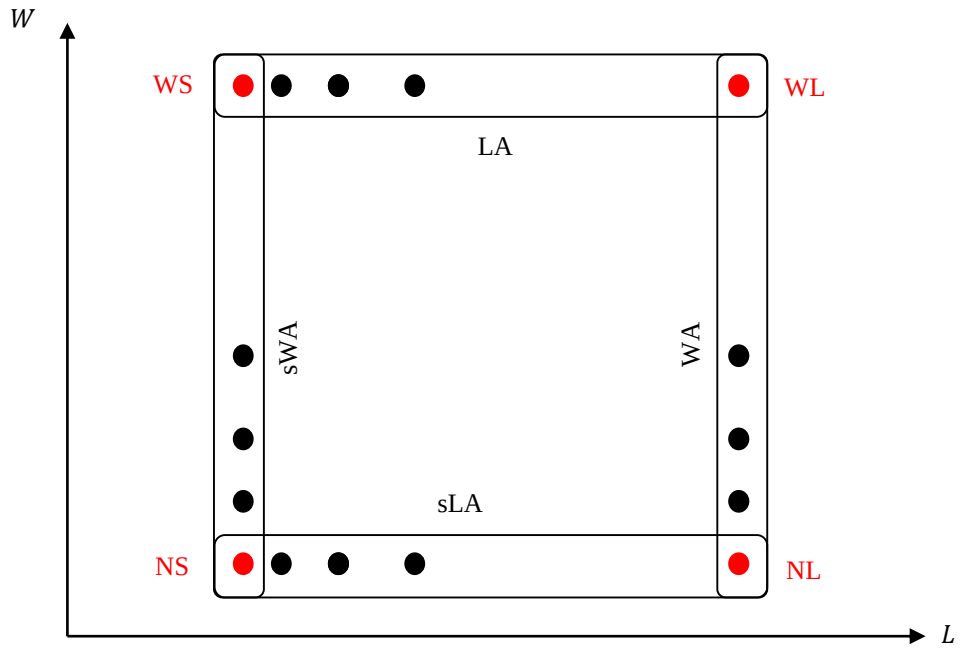
(data on this page are from device B)

CONTENT

- Brief review of BCD technologies
- LDMOS structure
- LDMOS modeling
- JFETIDG model for the drift region
- PSPHV model
- PSPHV model extraction
- Conclusions

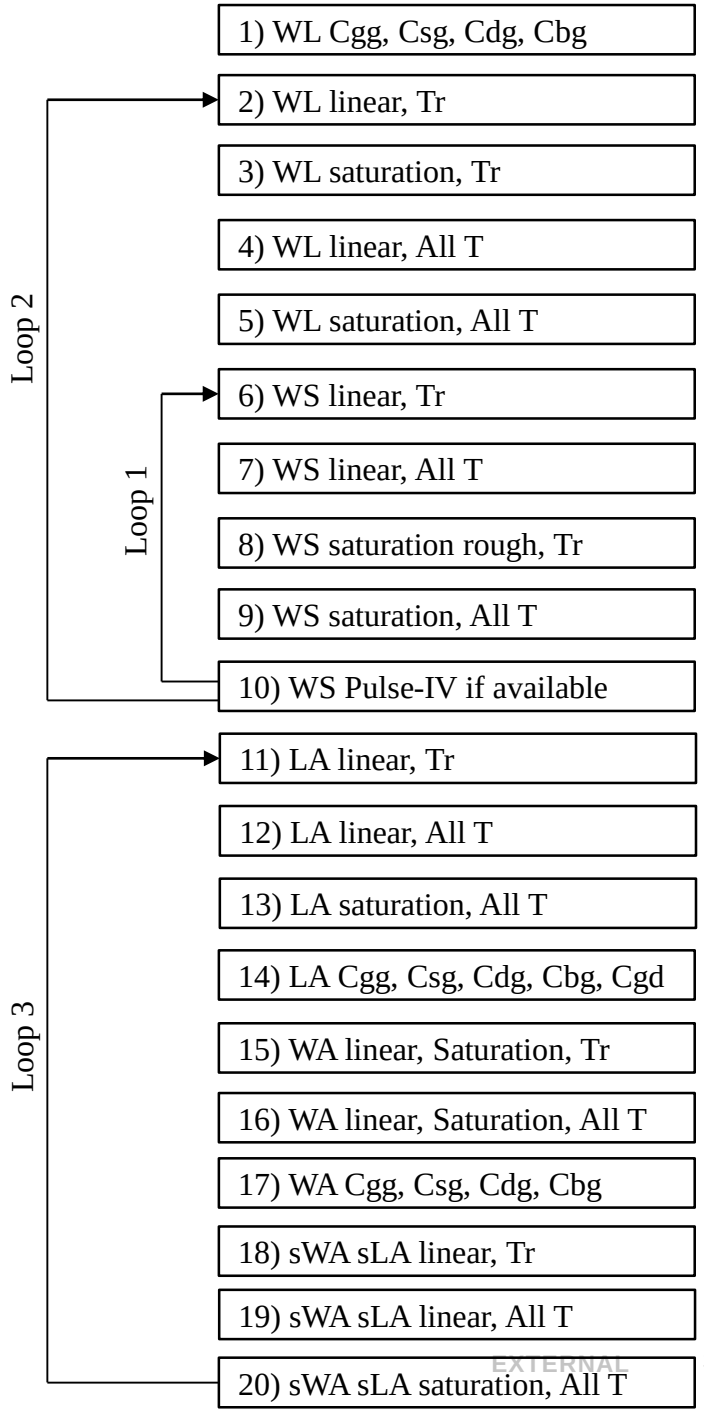
MEASUREMENT DATA NEEDED

- DC data (all geometries and temperatures)
  - Idvg_lin
  - Idvg_sat
  - Idvd
- CV data for WL, WS, NL, NS devices at room T
  - Cxg
  - Cgd
- Optional s-param for WS
  - Y22 to extract Cth
  - Cxg to extract Vdi clamping
- Optional pulse IV
  - Idvd to check model without self-heat

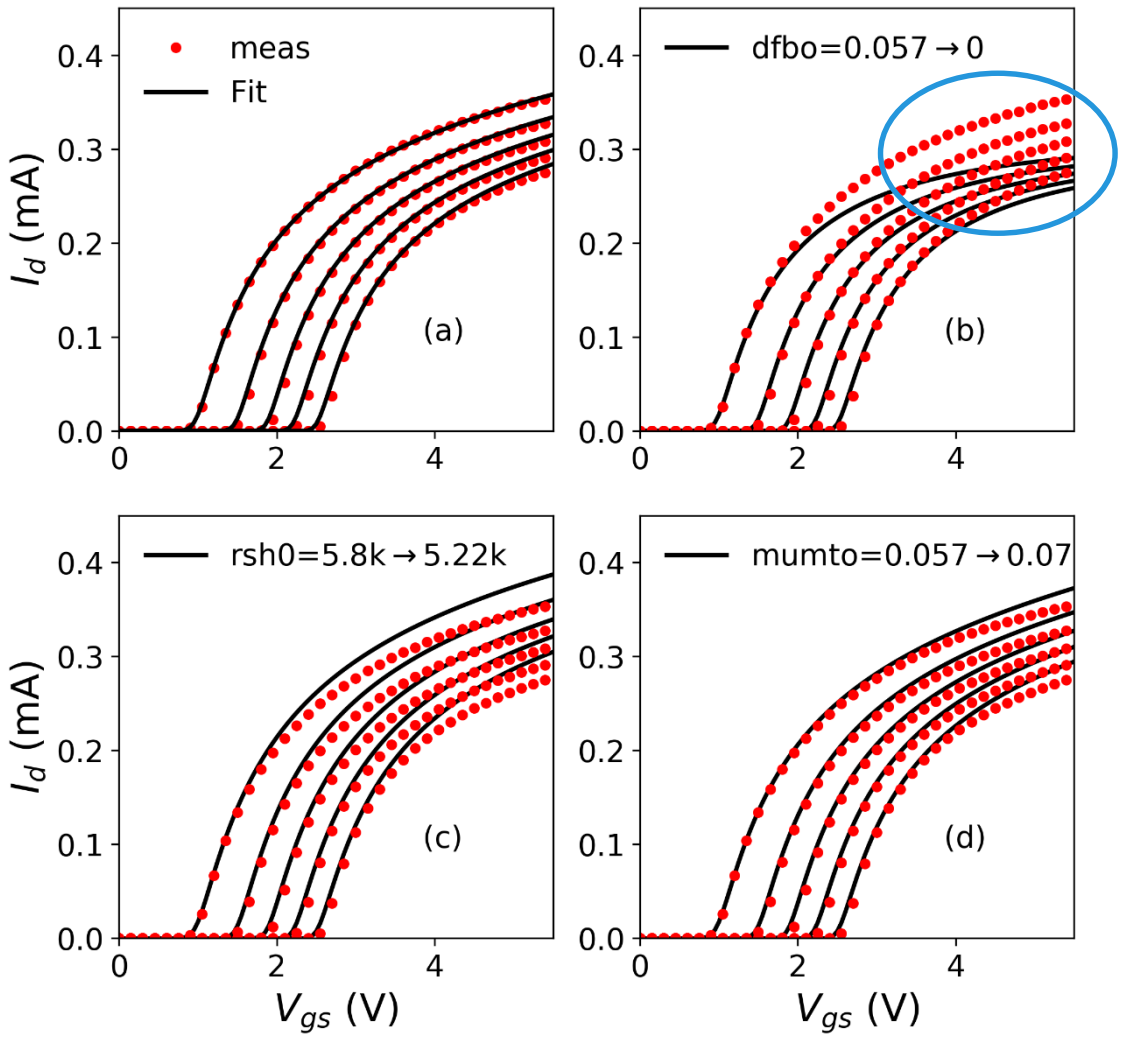


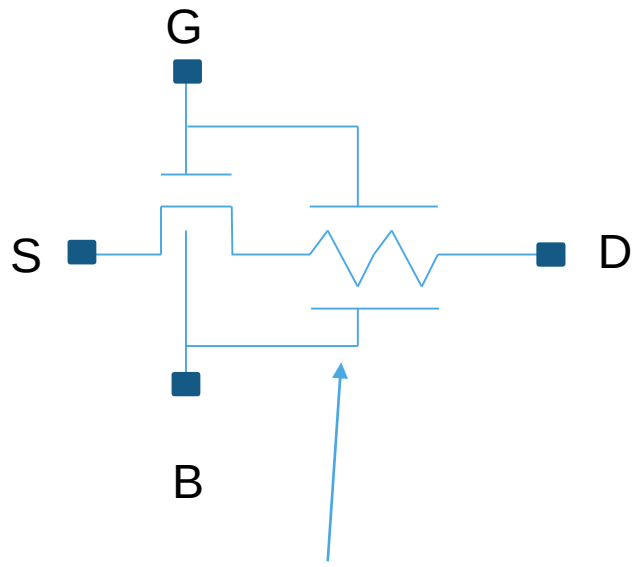
PSPHV EXTRACTION FLOW

- The detail is documented by IEEE J-EDS 2020 (OA) https://ieeexplore.ieee.org/document/9146541
- The difficult part is short channel idvd fitting where quasi-saturation, avalanche, and self-heating all come into play
- We will show some parameters and impacts here



BOTTOM PN-JUNCTION IMPACT

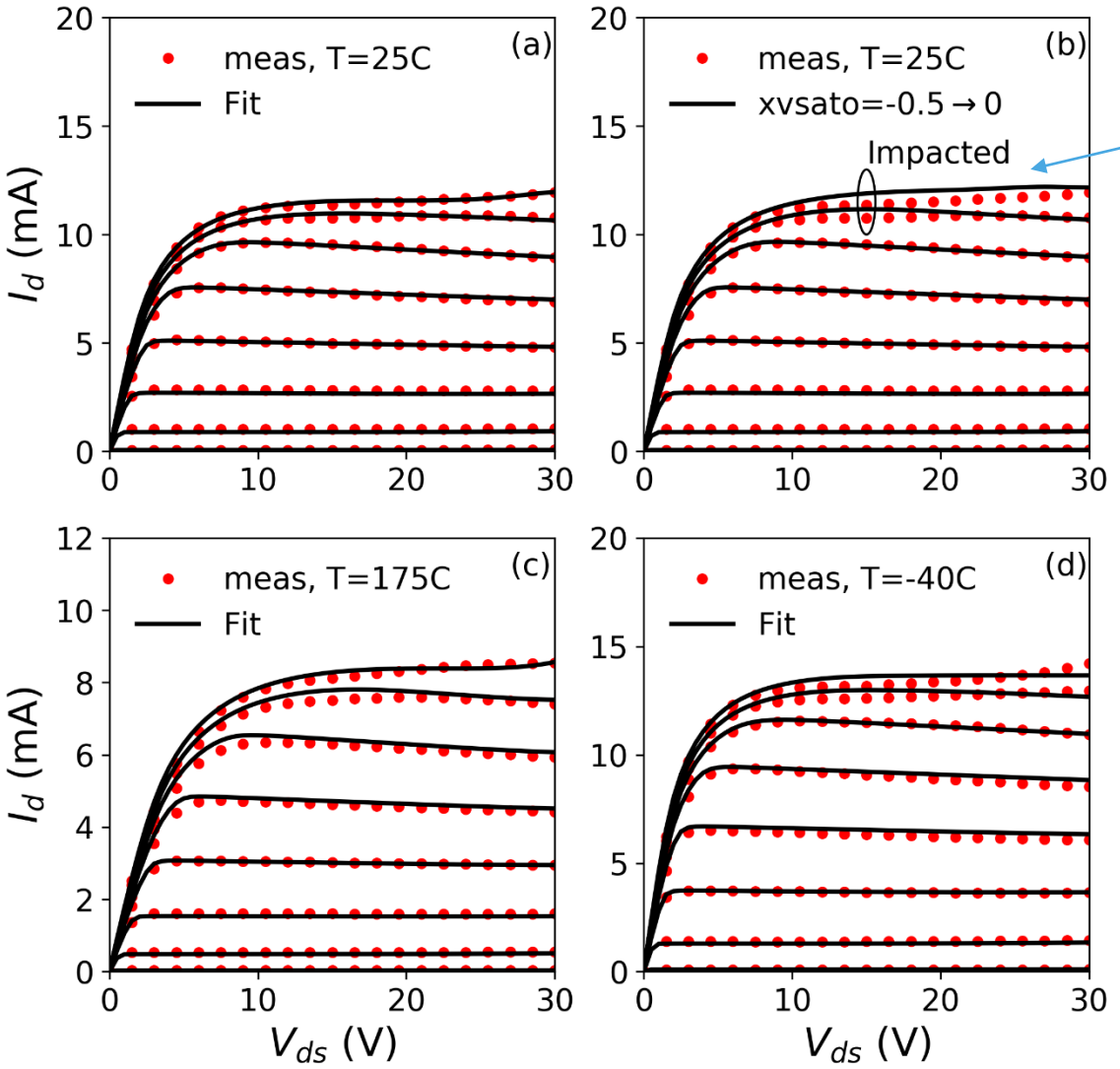




JFET
Bottom pn-junction modulation effect.
Param: dfbo

(data on this page are from device B)

ROOM TEMPERATURE IMPACTED BY TEMPERATURE COEFFICIENT

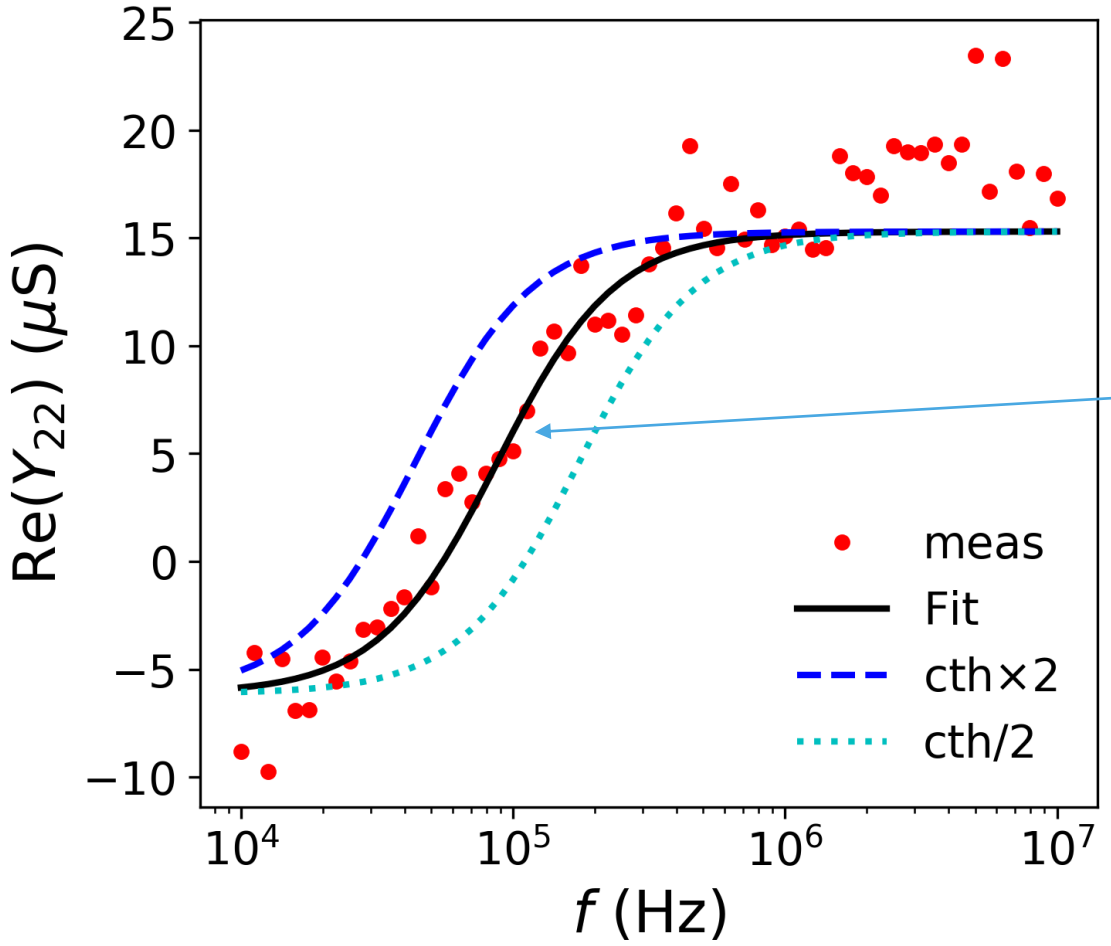


Due to self heating effect, the temperature dependence of model parameter will impact room temperature characteristics.

xvsat is the temperature coefficient of saturation velocity for the drift region.

(data on this page are from device B)

THERMAL CAPACITANCE (CTH) EXTRACTION

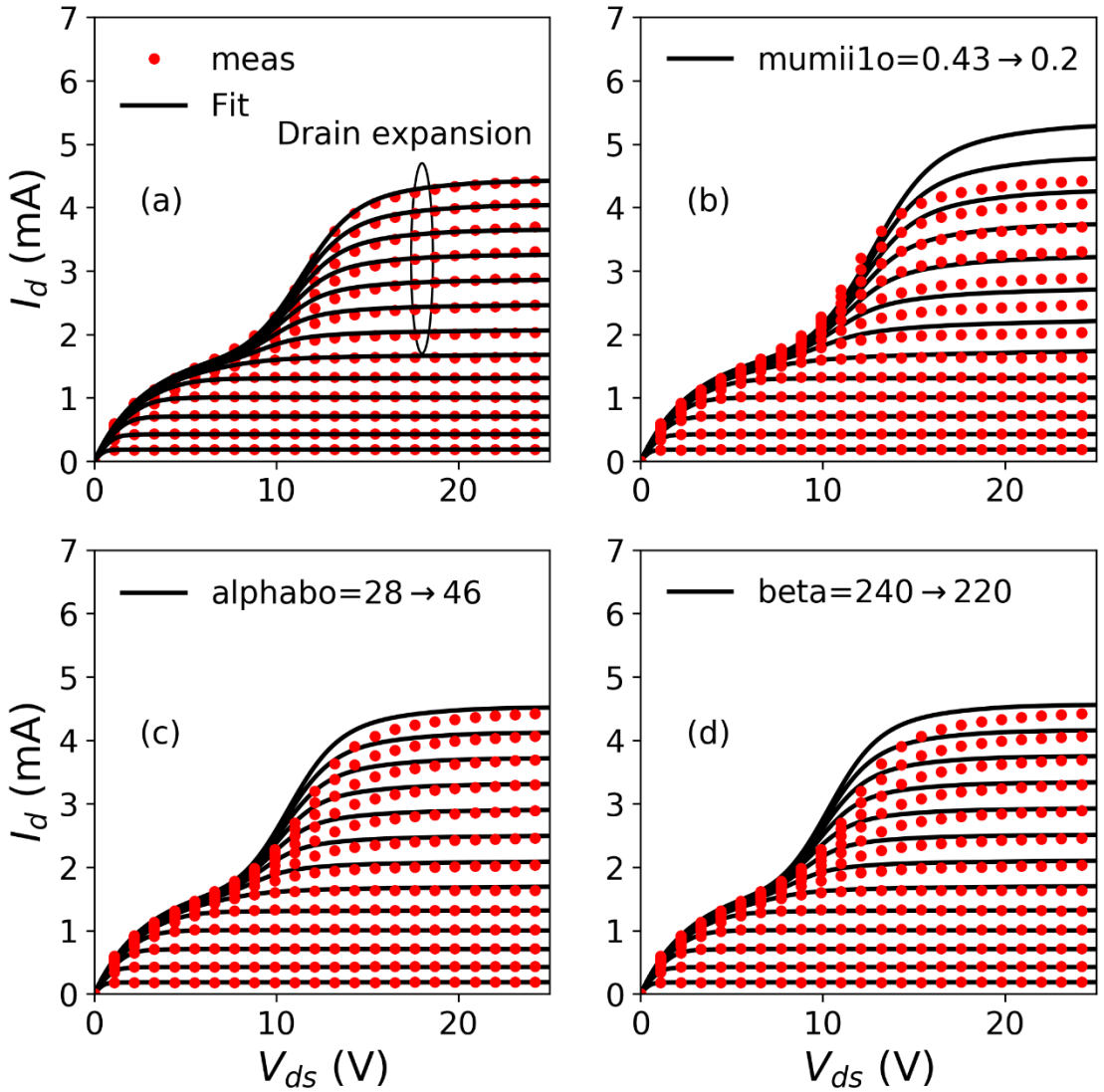


Full scaling of thermal resistance (RTH) should be first extracted from idvd and then verified with Re(Y22) at low freq.

CTH can be extracted from the transition freq.

(data on this page are from device B)

DRAIN EXPANSION



The avalanche current in the drift reduces its resistivity. It can even pull device out of quasi-saturation and increases drain current significantly.

(data on this page are from device C)

CONCLUSIONS

- BCD technologies have enabled many power related ICs. LDMOS is the key component.
- LDMOS can be modeled as a MOS in series with a dual-gate JFET.
- PSPHV can accurately model LDMOS.
- PSPHV is publicly available.

SECURE CONNECTIONS
FOR A SMARTER WORLD

NXP, THE NXP LOGO AND NXP SECURE CONNECTIONS FOR A SMARTER WORLD ARE TRADEMARKS OF NXP B.V. ALL OTHER PRODUCT OR SERVICE NAMES ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS. © 2020 NXP B.V.