Aging Effects and Modeling Researches on 22nm FDSOI MOSFETs

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Reliability has become one of the most important design indicators of ICs.

<table>
<thead>
<tr>
<th></th>
<th>Consumer</th>
<th>Industrial</th>
<th>Automotive</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>0°C → 40°C</td>
<td>-10°C → 70°C</td>
<td>-40°C → 85°C/155°C</td>
</tr>
<tr>
<td>Lifetime</td>
<td>1-3 years</td>
<td>5-10 years</td>
<td>&gt; 15 years</td>
</tr>
<tr>
<td>Test Coverage</td>
<td>~ 95%</td>
<td>~99%</td>
<td>Target = 0 dppm</td>
</tr>
<tr>
<td>Safety Rating</td>
<td>-</td>
<td>ASIL B</td>
<td>ASIL C, D</td>
</tr>
</tbody>
</table>

*Semiconductor Requirements for Heterogenous Applications By market segment (cadence)*

- Multiple effects
- Hard to characterize

Automotive puts forward more stringent reliability requirements for ICs.

Accurate prediction of device performance vs. time.
Backgrounds

### Cadence Legato
- **Model Lib**: Input Netlist
- **Input Netlist**: Input
- **URI DLL**: RelXpert

### Synopsys MOSRA
- **Model Lib**: Input Netlist
- **Input Netlist**: input.p1

### TSMC TMI
- **Model Lib**: Input Netlist
- **Input Netlist**: input.raw/canal name.tran

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**Commercial reliability simulation software**

<table>
<thead>
<tr>
<th>Process</th>
<th>FAB</th>
<th>Kernel</th>
<th>Process Model</th>
<th>Aging Effect</th>
<th>Self-heating Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>130nm PD SOI</td>
<td>GSMC</td>
<td>BSIMSOI</td>
<td>5 Corner/Mismatch</td>
<td>N/A</td>
<td>√</td>
</tr>
<tr>
<td>22nm BULK</td>
<td>HLMC</td>
<td>BSIMBULK</td>
<td>9 Corner/Mismatch/Monte Carlo</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>22nm FD SOI</td>
<td>GF</td>
<td>BSIMIMG</td>
<td>9 Corner with SOA/Mismatch/Monte Carlo</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>7nm FinFET</td>
<td>TSMC</td>
<td>BSIMCMG</td>
<td>11 Corner with SOA/Mismatch/Monte Carlo</td>
<td>√</td>
<td>√</td>
</tr>
</tbody>
</table>

- **No domestic alternative solutions**
- **Commercial IPs**: expensive licensing fee increases the R&D cost
FDSOI: High speed
Thin oxide, low parasitic capacitance
Low power consumption
No substrate leakage
High reliability
Low random doping distribution

FDSOI is more advantageous in Vehicle electronics, IoT, and RF communications
Outlines

1. Backgrounds
2. Aging Effects Modeling
3. Dynamic Voltage Stress
4. SMI Simulator
5. Summary
Characterization of Aging Effects

What is aging?

- Time dependent dielectric broken, (TDBD)
- Electron migration, (EM)
- Bias temperature instability, (BTI)
- Hot carrier injection, (HCl)

Reach lifetime limit, no need to characterize

No recovery

Negative / Positive

R-D model Recovery

NBTI on PMOS

PBTI on NMOS
Static Aging Characters

NBTI on PMOS

- $V_{th}$ shift
- $Gm_{\text{max}}$ decreases
- SS increases

Holes can be captured and released, forms equivalent interface capacitance

PBTI on NMOS

- $V_{th}$ shift
- Only affect $V_{th}$

Electrons is hard to be captured, forms fixed charges

R-D model
3 methods to extract threshold voltage $V_{th}$:

- On The Fly (OTF), can be affected by mobility degradation;
- Constant current (Icon), can be affected by SS increase;
- Extrapolation in the linear region (ELR) at $G_{m_{max}}$, closest to actual physics.

Lifetime Prediction

Lifetime prediction summary:

- OTF: 63000 s
- ELR: 7200 s
- Constant current: 11000 s

Even mV error can result in multiple lifetime prediction difference.
Unified Aging Model

- **HCI shows correlation with BTI**

  **BTI**: $V_{th}$, mobility(scattering) degradation

  **HCI**: intrinsic mobility degradation

  BTI: SS degradation

  HCl: intrinsic mobility degradation

  The influence of HCl can be extracted based on proper extraction of BTI

  **Unified model**: \[ \frac{1}{u_{tot}} = \frac{1}{u_p} + \frac{1}{u_p/\alpha_{co}} + \frac{1}{u_p/\alpha_{ph}} + \frac{1}{u_p/\alpha_{ro}} \]

  Matthiessen Rule

Vth and SS Modeling

- Performance in subthreshold region can be described by interface charges.
- Model includes the influence of gate/drain voltage and temperature.

**V \(_{th}\) model:**

\[
\Delta V_{th} = \frac{q \cdot (1 + k) \Delta N_{it}}{C_{ox}}
\]

\[
\Delta N_{it} = B \cdot \exp \left( C_g V_{gs} + C_d V_{ds} - \frac{E_a}{k_B T} \right) \cdot t^n
\]

- Voltage stress: 0.1 V
- Temperature: 50 °C

**SS model:**

\[
\Delta SS = 2.3 \cdot \frac{kT}{q} \left( 1 + \frac{C_{dep}}{C_{ox}} + \frac{\Delta C_{it}}{C_{ox}} \right)
\]

- The performance degradation in subthreshold region can be described by this model accurately.
Mobility Degradation Modeling

- Low Vg: $\mu$ decreases significantly after aging. Coulomb scattering is enhanced by interface traps.
- High Vg: no evident change. Aging doesn’t affect surface scattering (different with bulk).

Coulomb scattering model:

$$\mu = \frac{\mu_0}{[1 + \alpha \cdot \frac{Q_{it}}{(\beta + Q_{inv})}]}$$

Mobility approximate formula:

$$\frac{\Delta \mu}{\mu} = 1 - \frac{I_{ds,hf}}{I_{ds,hf0} + V_{gs,hf} - V_{th0} \cdot \Delta V_{th, hf} + I_{ds,hf0}}$$
Outlines

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4. SMI Simulator
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Dynamic Voltage Stress (DVS)

- Static model cannot describe dynamic aging

Correlation with stress sequence:
The recovery will affect follow-up aging characters

Correlation with bias voltage:
Voltage stress in recovery cycle may be different

Important factors to be considered:
Recovery voltage, recovery time, duty cycle, number of cycles, etc.
Saturation in DVS

- $V_{th}$ degrades exponentially:
  \[ \Delta V_{th} = C \cdot t^n \]
  \[ \Delta V_{th}^{1/n} = C^{1/n} \cdot t \]

Changes linearly with time

- Recovery effects will increase the follow-up aging rate, saturates after 3 cycles
- No saturation in high $V_{rec}$ (not shown)

Make DVS model complex!
Various charge based models have been investigated:

- **Bias dependency** × multiple cycles ×

### Fixed charge model:

\[
Q_f = \min(\gamma Q_t \left[ 1 - \Delta V(A_0 + B_0 Q_{f0}) \cdot t_r^\beta \right], Q_{f_{\text{max}}})
\]

### Interface charge model:

\[
Q_t = (A_i + B_i Q_f) \cdot t_S^\alpha
\]

### Vth model:

\[
\Delta V_{\text{th}} = \frac{(Q_t + Q_f)}{C_{\text{ox}}}
\]

**Stress cycle:**
- Produce interface charges
- Stress cycle: charges captured

**Recovery cycle:**
- Capture fixed charges
- Recovery cycle: charges transfer to saturation

DVS model can fit the experimental data under various conditions in high accuracy, reaches mV level
Outlines

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What does the simulator do?

- SPICE model coverage
- SPICE model coverage after aging
- Device performance after aging

Aging effects can cause the device performance move to SS corner.

Precisely describe aging effects → Precisely predict lifetime.
Circuit Level Aging Simulation

Why we need a simulator?

1. The SPICE model cannot characterize aging effects directly
2. For circuit level applications, different function units have different aging characters

Typical ASIC Chip

- Analog (HCl)
- SRAM (BTI)
- Digital (HCl&BTI)

The aging characters of each device need to be calculated separately
SMI Simulator

- Local sampling and extrapolation

![Graph showing MOSFETs aging vs time with linear extrapolation and integral calculation of device aging effects.]

- SMI has already been embedded into the EDA software ALPS/Xmodel of Empyrean Corporation for commercial applications

Workflow:

1. Netlist Analyze
2. Transient simulation
3. Activate aging model
   - Y: Continue
   - N: Finish
4. SPICE Simulator
5. Invocation Procedure:
   - Recognize nodes voltages
   - Activate aging model
   - Integral calculation
   - Extrapolation calculation
   - Aging calculation

Return Procedure:

SMI Simulator
## SMI Simulator

<table>
<thead>
<tr>
<th>Feature</th>
<th>MOSRA</th>
<th>SMI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integration</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Extrapolation</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>BTI_Core</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>HCI_Core</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Annealing</td>
<td>✓</td>
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<tr>
<td>Temperature behavior</td>
<td>×</td>
<td>✓</td>
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<tr>
<td>Extraction Flow</td>
<td>×</td>
<td>✓</td>
</tr>
<tr>
<td>Failure Criteria</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Lifetime Prediction</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Self-heating Model</td>
<td>×</td>
<td>✓</td>
</tr>
<tr>
<td>DVS Model*</td>
<td>×</td>
<td>✓</td>
</tr>
</tbody>
</table>

- Ring oscillator simulation results of SMI are highly consistent with Synopsys MOSRA under different voltages, sizes and temperatures.
1. Aging effects including BTI and HCI of 22 nm FDSOI devices were systematically studied;

2. A novel model, as well as a simulator (SMI) supporting both SVS and DVS aging conditions, were investigated;

3. This model can precisely predict key parameters of MOSFETs degrading with time in high accuracy;

4. The model accuracy is highly consistent with MOSRA and meet the industrial standard;

5. The SMI simulator has already been embedded into the EDA software ALPS/Xmodel of Empyrean Corporation and realized commercial applications.
Thank you!