OVERVIEW AND LATEST UPDATES OF L-UTSOI, STANDARD MODEL DEDICATED TO FDSOI TECHNOLOGIES

Invited talk: MOS-AK guangzhou
https://www.mos-ak.org/guangzhou_2022/

August, 2022

L-UTSOI model developers
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• Introduction

• Main feature 102.4: “parasitic current” (Impact Ionization & gate current)
• Main feature 102.5: “doping management” (Substrate depletion & Poly-Depletion)
• Main feature 102.6: “first order NQS model”

• Conclusion
2D electrostatic description (from depletion to inversion/accumulation) is a complex problem. Usually, we model 1D electrostatic (long & wide) by including the other effects like a correction.

Core’s model
Long channel transistor

Following industrial expectation, compact model is continually improves.

PSP, BSIM-Bulk, BSIM4 …

BSIM-CMG, Leti-NSP …

Following industrial expectation, compact model is continually improves.

But core remains generally the same. Thus, all new items is see as an “add on”.

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[1] https://si2.org/cmc/

INTRODUCTION: COMPACT MODEL POINT OF VIEW

Model support and/or develop by LETI and available in all major SPICE tool.
For $V_{bs}=-3\text{V}$, the electric field makes the inversion charge build up at the front interface $\rightarrow$ we end-up with a front channel only.
For $V_{bs}=0\text{V}$, the carriers are first spread within the thin body at the onset of inversion (volume inversion).

→ Then the charge builds up at the front interface

Animations come from Poisson-Schrödinger simulations are used to illustrate the apparition of the inversion layer in the thin body when the front gate is swept from -0.5V to +1V.

$V_{gs} = +0.05\text{V}$
$V_{bs} = 0\text{V}$
For \( V_{bs} = +3V \), the inversion charge starts to build up at the back interface. When this charge density is large enough, front and back interfaces are electrostatically de-coupled and a second channel is created at the front interface as the gate voltage is further increased.

Animations come from Poisson-Schrödinger simulations are used to illustrate the apparition of the inversion layer in the thin body when the front gate is swept from -0.5V to +1V.
L-UTSOI MODEL: STANDARD MODEL DEDICATED TO FDSOI TECHNOLOGY

- From 2013, the need to consider FDSOI transistor as a true independent double gate transistor, with possible conduction at both thin body interfaces, is fulfilled by Leti-UTSOI 2.x.x versions
- Since 2013, the model has been further improved, based on industrial partner needs
- Since 2020, model is a CMC standard model.

Leti-UTSOI 1.x.x
Back interface assumed depleted/weakly inverted

Leti-UTSOI 2.x.x
No assumption on back interface regime

L-UTSOI
New model name within CMC
OUTLINE

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• Conclusion
In FDSOI transistor, Impact ionization is more significant for thicker oxide transistors, featuring higher supply voltages, and only weak avalanche occurs.

This small impact ionization component increases source/drain current (in opposition to bulk MOSFET where impact ionization results in a bulk/drain current).

Inclusion of this model in term of physics and code implantation is close to that of PSP model [1]. For low-level avalanche multiplication, the avalanche current is [2]:

\[ I_{aval} = I_{DS} \cdot \int_0^L \alpha_n \cdot dx \sim A1.\Delta V_{sat} \cdot I_{DS} \cdot e^{\frac{A2}{\Delta V_{sat}}} \]

\[ \Delta V_{sat} = V_{DS} - A3. V_{DSsat} \]

\[ A_2 = A2. \left( \frac{T_{KC}}{T_{KR}} \right)^{STA2} \]

where \( A1, A2, A3 \) and STA2 are related parameters

IMPACT IONIZATION EVIDENCE AND MODELING: MODEL PARAMETERS VARIATION

Gd vs $V_{DS}$ (A.U.) for diff. value of $V_{GS}$ in log scale:
- A1 variation
- A2 variation
- A3 variation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Comment</th>
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<tbody>
<tr>
<td>SWIMPACT</td>
<td>-</td>
<td>Flag for impact ionization current</td>
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<tr>
<td>A1</td>
<td>-</td>
<td>Impact ionization pre-factor</td>
</tr>
<tr>
<td>A2</td>
<td>-</td>
<td>Impact ionization exponent at TR</td>
</tr>
<tr>
<td>A3</td>
<td>-</td>
<td>Saturation voltage dependence of impact ionization</td>
</tr>
</tbody>
</table>

In accordance with previous theory A1, A2 and A3 modulate $g_d v_d$ curve to include low-level avalanche multiplication
IMPACT IONIZATION EVIDENCE AND MODELING: MODEL VS EXPERIMENT

Long channel

Short channel

Negative $gm$ is the consequence of SHE

$V_{GS} = 0.2, 0.4, 0.6, 0.8, 1.0, 1.2, 1.6, 2.0$ V
Fowler-Nordheim (FN) [1-2]:
- For MOS structures with a relatively thick oxide.
- Barrier is triangular.

Direct Tunneling (DT) [1-2]:
- Oxides have thicknesses in the order of a few nanometers.
- Barrier is not triangular, but approximately trapezoidal.

In view of reduction of oxide thickness and supply voltage Direct tunneling is sufficient to model at first order gate current.
ACCURATE MODEL FOR OVERLAP GATE CURRENTS: PHYSICAL FOUNDATION OF GATE CURRENT MODEL IN L-UTSOI 2/2

Initially this model comes from PSP [1], where the integration over energy is skipped to obtain explicit function by assuming that all electrons have the same kinetic energy.

\[ J_{g(x)} = J_0 \int_{0}^{\infty} D_{(E,x)} \cdot F_{S(E,x)} \cdot dy \sim J_0 \int_{0}^{\infty} D_{(x)} \cdot F_{S(x)} \]

where \( D_{(E,x)} \) is the transmission coefficient calculated in the WKB approximation, \( F_{S(E,x)} \) is the supply function and \( x \) is the position along the channel.

\[ D_{(x)} = e^{-B_0 \cdot f_{(zg)}} \]

where \( zg \) is the voltage drop through the gate oxide normalized to the built-in voltage, \( J_0 \) and \( B_0 \) are constant related to the tunneling current.

\[ f_{(zg)} = \left(1 - \frac{1 - zg}{zg}\right)^{1.5} \sim -3 + \frac{G2}{2} zg + \frac{G3}{3} zg \]

G2 (0.375), G3 (0.063) is taylor expansion parameter.

DT-like formulation

\[ \frac{\phi_{s}^{\frac{1}{2}} - (\phi_s - qV_{ox})^{3/2}}{\phi_{ox}^{\frac{1}{2}} - \phi_s^{3/2}} \]

GC2O in PSP

GC3O in PSP

In current version of L-UTSOI, this model is derived for « inversion » and « overlap » branch.

Discrepancy observed on gate current is evident for $V_{GS} << 0$ and $V_{DS} >> 0$. We observe 2 different behaviors at low and high $V_{GD}$ values.

We propose to add high electric field component close to Fowler-Nordheim (FN) equation:

$$J_g \sim J_0 \cdot F_s(x) \cdot e^{-\frac{B_0}{f(zg)}} + FNOV \cdot e^{-\frac{B_0}{GCOVFN \cdot zg}}$$

We introduce 2 more parameters $FNOV$ and $GCOVFN$.
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• Conclusion
SUBSTRATE DOPING MODEL ENHANCED: LIMITATION

Model vs TCAD

C\textsubscript{GG}

C\textsubscript{GB}

L-UTSOI 102.4.0

Variation <1f and no parasitic capacitance

Long & Wide channel

C\textsubscript{GB} vs C\textsubscript{BG}

C\textsubscript{GS} vs C\textsubscript{SG}

C\textsubscript{GD} vs C\textsubscript{DG}

V\textsubscript{BS} = 5 .. -2 V

Capacitance and reciprocal capacitance is not aligned and sometime go below expected charge (unphysical behavior).

RQ: inclusion of substrate depletion is already a correction of the core model. Here we propose to improve it.
Present UTSOI model uses an approximation to calculate the substrate depletion where its surface potential resolution is similar to PSP: all SOI stack is considered as an unique dielectric.

Core's model calculation

\[
\text{Previous solution} = \text{Core's model calculation} + \text{"Boundary condition correction"}
\]
Present UTSOI model uses an approximation to calculate the substrate depletion where its surface potential resolution is similar to PSP: all SOI stack is consider as an unique dielectric.

Core's model calculation

Previous solution

Proposed solution

Physically, the channel inversion charge screens the gate control to the back plane depletion. We propose to replace gate voltage by an approximated value using similar initial guess as the surface potential calculation.
SUBSTRATE DOPING MODEL ENHANCED: MODEL

Core’s model only (no substrate depletion)
SUBSTRATE DOPING MODEL ENHANCED: MODEL

Core’s model only
(no substrate depletion)

Previous UTSOI model:
All SOI stack is consider as an unique dielectric.

w. substrate depletion
& wo. Inversion in back channel

Threshold voltage
VGB (V)

Potential at 
substrate/BOX interface (V)
SUBSTRATE DOPING MODEL ENHANCED: MODEL

Core’s model only
(no substrate depletion)

Previous UTSOI model:
All SOI stack is consider as an unique dielectric.

By using an approximated back channel surface potential
(similar to initial guess as the surface potential calculation)
Model vs TCAD

Variation <1f and no parasitic capacitance

Long & Wide channel

L-UTSOI 102.4.0

\( C_{GG} \)

\( C_{GB} \)

New model

L-UTSOI 102.5.0

\( V_{BS} = 5 \ldots -2 \text{ V} \)

\( C_{BG} \)

\( C_{GB} \)

\( C_{GG} \)

\( C_{SG} \)

\( C_{GD} \)

\( C_{DG} \)

Capacitance and reciprocal capacitance is improved
Comparison between measurement from 28nm technology (symbol) and model including improvement on substrate depletion (line): For long & wide device.
TCAD ILLUSTRATION: POLY-DEPLETION

TCAD: Potential and $C_{GG}$ vs $V_{GS}$ @ diff. NP TOX=2n, TSI=2n & TBOX=25n

Poly-Silicon Potential from interface to volume ($\Psi_P$)

Surface potential at Si/Ox ($\Psi_S$)

NP=1e22
TCAD ILLUSTRATION: POLY-DEPLETION

The 2 effects of Poly-Silicon gate: charge reduction due to depletion in gate & Vt shift due to flat band shift.
POLY-DEPLETION MODEL: CORRECTIVE SOLUTION

Modification of core model is not possible. Our objective is to find a corrective solution to include the poly-depletion.

Starting from Poisson equation in Polysilicon gate:

\[
\frac{d^2 \Psi}{dy^2} = \frac{q}{\varepsilon_{si}} \left( N_p - N_p \cdot e^{-\frac{\Psi}{ut}} \right)
\]

Using boundary conditions and \( \Psi_p >> 0 \) in polarization range:

\[
\frac{1}{2} \left( \frac{d\Psi_p}{dy} \right)^2 = \frac{q \cdot N_p}{\varepsilon_{si}} \left( \Psi_p + ut \cdot e^{-\frac{\Psi_p}{ut}} - ut \right) \approx \frac{q \cdot N_p}{\varepsilon_{si}} (\Psi_p)
\]

Equating with the charge in silicon film:

\[ C_{ox} \cdot (V_{GS} - \Psi_s - \Psi_p) = kp \cdot C_{ox} \cdot \sqrt{\Psi_p} \]

Thus, \( \Psi_p \) equation is [1]:

\[
\Psi_p (\Psi_s) = \left( \sqrt{V_{GS} - \Psi_s} + kp^2/4 - kp/2 \right)^2 \quad \& \quad kp = \sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_p / C_{ox}}
\]

Note: the implementation in code is more complex due to the charge partitioning (not detailed here).

POLY-DEPLETION MODEL: CORRECTIVE SOLUTION

Modification of core model is not possible. Our objective is to find a corrective solution to include the poly-depletion effect.

- Starting from Poisson equation in Polysilicon gate:

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\psi_p (\psi_s) = \left( \sqrt{V_{GS} - \psi_s} + k_p^2/4 - k_p/2 \right)^2 \quad \& \quad k_p = \sqrt{2 \cdot \varepsilon_{si} \cdot N_p / C_{ox}}
\]

\( q_{g,0} = (V_{GS} - \psi_{s,0}) \) & \( \psi_{s,0} \) is charge surface potential without included Poly-Depletion effect:

\[
\text{Ratio} = \frac{q_{g,PD}}{q_{g,0}} = \frac{V_{GS} - \psi_s - \psi_p (\psi_s)}{V_{GS} - \psi_{s,0}} \approx \frac{V_{GS} - \psi_{s,0} - \psi_p (\psi_{s,0})}{V_{GS} - \psi_{s,0}}
\]

\[
\Delta V_{FB, PolyDep} = ut \cdot \ln \left( \frac{N_p}{n_i} \right)
\]

Advantage: This solution seems to be the most simple.

Limitation: Global accuracy for huge the poly-depletion.

2 flat-band model mode:
- When Poly-Depletion model is de-activated : metal gate is considered.
- When Poly-Depletion model is activated: Poly-Si gate is considered. But in 2 cases user can manage further flat-band through well known VFBO.

Comparison between measurement from Qualcomm (symbol) and model including Poly-Depletion (line) for PMOS device: For long & wide device.
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NQS SOLUTION IN SPICE

The state-of-the-art design of RF and mixed-signal CMOS circuits can require inclusion of the non-quasi-static (NQS) effects, such as the finite channel transit time.

Segmented model

Use several model instance

Several instance of SPICE model is used to emulate continuity equation. Unfortunately, complex parameter management strategy is necessary.

RTA model

This is sort of charge filtering by using RC as a filter of charge. This is first order effect of NQS only.

Spline-collocation-method

“Integrated” version of the segmented model. There are no specific parameter management compare. But model itself is limited (complexity, convergence ...)

\[
\frac{\partial q_i}{\partial t} + f(q_i, y) = 0
\]

\[
i_s = -i_S(dC) + X_S \frac{Q_{def}}{\tau}
\]

\[
i_D = I_D(dC) + X_D \frac{Q_{def}}{\tau}
\]
RTA-NQS MODEL IN L-UTSOI

\[
\begin{align*}
\frac{dQ_x}{dt} &= -\frac{Q_x - Q_x^{QS}}{\tau} \\
\frac{1}{\tau} &= \frac{\mu_{\text{eff}}}{L} \left( K_{\text{DRIFT}} \frac{Q_i}{C_{\text{ox}}} + K_{\text{DIFF}} u_t \right) \\
I_{\text{DS}} &\propto -\frac{1}{\tau} \cdot V(D_{\text{nsq}}) \\
I_{\text{GS}} &\propto -\frac{1}{\tau} \left( V(G_{\text{nsq}}) + \frac{V(G_{\text{nsq2}})}{K_\alpha} \right)
\end{align*}
\]

KDRIFT and KDIFF are extracted parameters

• RTA equations (1) is solved for \(Q_i\) and \(Q_D\) by the circuit simulator thanks to the use of internal nodes.
• The relaxation time is given by similar equation from\(^*\).
• An empirical pole is added to improve a little bit the accuracy through the partition parameter \(\alpha \in [0,1]\) with an associated relaxation time \(K_\alpha\).

Comparison between TCAD, segmented and NQS-RTA (no quantum, constant mobility, TOX=2n, TSI=10n, TBOX=25n and L=10u)

The good accuracy of NQS-RTA model up to twice the transition frequency.
We show the capability of the NQS-RTA model to reproduce 28nm FDSOI technology. Note that QS extraction (low frequency) is not illustrated here, but follows the usual extraction flow, only KDRIFT and KDIFF are extracted.
Simulation of “killer” NOR gate circuit which is a good benchmark of NQS interest*. The large peak, observed in QS condition due to a non physical current from the top transistor, is strongly reduced when we use the NQS model. As expected, this peak modulation is directly dependent on the model’s parameters setting.

*H. Wang et al, TED, vol 53, no. 9, September 2006
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Our team is a developer of the CMC (Compact Model Coalition) for 2 SPICE models: standardization process, implementation in commercial IC simulators, strong interaction with users.

- L-UTSOI compact model is dedicated to FDSOI technologies: [https://www.cea.fr/cea-tech/leti/l-utsoisupport](https://www.cea.fr/cea-tech/leti/l-utsoisupport)

<table>
<thead>
<tr>
<th>Date</th>
<th>Release</th>
<th>Major improvements/features</th>
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<tbody>
<tr>
<td>2020, January</td>
<td>L-UTSOI102.4</td>
<td>• Introduction of impact ionization model.</td>
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<tr>
<td></td>
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<td>• Introduction of extra gate to overlap current.</td>
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<td>2021, January</td>
<td>L-UTSOI102.5</td>
<td>• Introduction of Gate Poly-Depletion model</td>
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<tr>
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<td>• Enhancement of substrate depletion.</td>
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<td>2022, Mars</td>
<td>L-UTSOI102.6</td>
<td>• Introduction of RTA NQS model.</td>
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<tr>
<td><strong>Planned</strong></td>
<td>L-UTSOI102.7</td>
<td>• Introduction of cryogenic model.</td>
</tr>
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- PSP is a surface potential based model for deep-submicron bulk MOSFET: [https://www.cea.fr/cea-tech/leti/pspsupport](https://www.cea.fr/cea-tech/leti/pspsupport)

- Our website contains: Release information, Model documentation for PSP and L-UTSOI and Downloadable Verilog-A codes.

Thank you for your attention