Design Technology Co-Optimization Method for RF EDA

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II. QPZD nonlinear model

III. Statistical model and yield optimization

IV. MMIC IP model

V. Conclusion
Content

I. Introduction

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IV. MMIC IP model

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I. Introduction

Semiconductor Technology Landscape:

- Design technology co-optimization (DTCO)
- System Technology Co-optimization (STCO)

Beyond 1nm?

Can we close the gap?

1.5 & 1nm?

2nm?

4-3nm Nanosheet

7-5nm EUV MOL Co

16-14nm FinFET introduction

28nm

20nm

14nm

10nm

7nm

5nm

3nm

2nm

1nm

- New memory (STT, ...)
- New computing arch. (ML, ...)
- New cooling solution
- Advanced packaging (3DSIC, interposers)

- New materials (Cu, Ru, Ge)
- New interconnects (BPR, Airgap)
- New devices (CFET, Nanosheet)
- Track height scaling (9T, 6T, 4T ...)
I. Introduction

Design Technology Co-Optimization

- Another option beyond technology scaling
- Early feedback in process development

Multi-physics coupling

[Lu, IEDM 2018 Tutorial]
I. Introduction

DTCO for RF circuits require Cross-layer Physical Models (CPM)

- Connection the device parameters to electrical parameters
- Conduct the device parameters design for higher electrical performance
I. Introduction

DTCO for RF circuits: From material to system

- Circuit IP model
- Transistor Model
- Statistical Model

Cross-layer Physical Models
- Transistor Model
- Statistical Model
- Circuit IP model
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I. Introduction

II. QPZD transistor model

III. Statistical model and yield optimization

IV. Circuit IP model

V. Conclusion
II. QPZD transistor model

History of compact models

Advanced/4th: ACM, EKV (EPFL), BSIM5/6, MOS11, PSP (NXP), HiSIM (Hiroshima)
II. QPZD transistor model

Curtice (1980)  
Root (1991)  
L. Eastman (IEEE Fellow, Cornell Univ.)  
Nonlinear model without self-heating

Angelov (1992)  
TOM (1990)  
R. Trew (NCSU)  
Zone Division (ZD) based on analytical model

EEHMT 1993  
Black-box (1997)  
U. Radhakrishna (MIT)  
MVSG based on charge-based model

Black-box (time-domain) 1997

W. Curtice/M. Khan/J. Hwang (IEEE Fellows)  
Including Ambient temperature

• K. Webb (IEEE Fellow, Purdue Univ.)  
• Curtice cubic model with self-heating

Y. S. Chauhan (UNIK/UCB/IIT)  
ASM-HEMT based on surface potential model

G. Branner (IEEE Life Member, UC Davis)  
Including trapping and self heating

Y. Xu (UESTC)  
QPZD model based on analytical model

GaN device  
Empirical model

GaN device  
Physical model
II. QPZD transistor model

Concept of compact models

- Ideal device model
- Real device model

Intrinsic Models

- Trapping effect
- Self-heating effect
- Field-plate capacitance
- Velocity saturation
- Mobility degradation
- Device Noise

Parasitic Parameter
II. QPZD transistor model

Motivation of Quasi-Physical Zone Division model

- Many fitting parameters for real devices
- Convergency

GaN ASM-HEMT Model

GaN MVSG Model

GaN QPZD Model

<table>
<thead>
<tr>
<th>Models</th>
<th>Approx. Number of Parameters</th>
<th>Self-Heating Effects</th>
<th>Trapping Effects</th>
<th>Ambient Temperature Effects</th>
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<td>Angelov GaN [8]</td>
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<tr>
<td>Modified Angelov [30]</td>
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<td>✓</td>
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</tbody>
</table>

- Simplify functions
- Reserve physical parameters
II. QPZD transistor model

Core IV Model

Zone division theory

Parameter extraction flowchart

Electron sheet density model

\[ n_s = A_n \cdot \tanh(a_n \cdot (V_{gs} - V_{off}) + b_n) + B_n \]

Critical electric field model

\[ E_c = (a_0 + a_1 V_{gs})(b_0 + b_1 T_{ch} + b_2 T_{ch}^2) \]

Threshold voltage model

\[ V_{off}(T) = \phi_B(T) - \Delta E_c(T) - \frac{qN_d d_d^2}{2\varepsilon_{AlGaN}} - \frac{q\sigma(d_d + d_i)}{\varepsilon_{AlGaN}} \]
II. QPZD transistor model

Parasitic EM model

Parameter extraction flowchart

Device Structure

\[ Y_{11} = j\omega \left( C_{gsx} + C_{gdx} \right) \]
\[ Y_{22} = j\omega \left( C_{dsx} + C_{gdx} \right) \]
\[ Y_{12} = Y_{21} = j\omega C_{gdx} \]
II. QPZD transistor model

Thermal model

Self-heating Effects

\[ T_{ch} = T_0 + P_{\text{diss}} R_{th} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L_g)</td>
<td>Gate length</td>
</tr>
<tr>
<td>(t_{\text{sub}})</td>
<td>Substrate thickness</td>
</tr>
<tr>
<td>(t_{\text{GaN}})</td>
<td>Buffer thickness</td>
</tr>
<tr>
<td>(W_g)</td>
<td>Gate width</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

Buffer:

\[ \Delta T_{\text{GaN}} = \frac{P_{\text{diss}}}{\pi NW_g K_{\text{GaN}}} \ln \left( \frac{4t_{\text{GaN}}}{\pi L_g} \right) \]

Substrate:

\[ \Delta T_{\text{Sub}_{\text{up}}} = \frac{P_{\text{diss}}}{\pi NW_g K_{\text{Sub}}} \ln \left( \frac{\eta s^2}{t_{\text{GaN}} W_g} \right) \]

Die attach:

\[ \Delta T_{\text{Die}_{\text{attach}}} = \frac{P_{\text{diss}} t_{\text{Die}_{\text{attach}}}}{K_{\text{Die}_{\text{attach}}} A_{\text{Die}_{\text{attach}}}} \]
II. QPZD transistor model

Trapping model

SRH model for trapping

1. Electron capture
2. Electron emission
3. Hole capture
4. Hole emission

Emission: \[ i_E = \omega_C C_T (V_0 - v_T) \]

Capture: \[ i_C = \omega_C C_T v_T \exp \left( \frac{v_I}{kT/q} \right) \]

Equivalent circuit model

\[ \frac{dp_D}{dt} = c_n N_C \left[ (N_D - p_D) e^{\frac{E_D - E_C}{kT/q}} - p_D e^{\frac{E_F - E_C}{kT/q}} \right] \]
II. QPZD transistor model

Field-plate model

Device structure

Equivalent circuit model

\[ Q_{g,k} = \frac{2 \cdot w \cdot C_{g,k} \cdot L_k}{3} \cdot \left( \frac{V_{gd,k} - V_{off,k}}{V_{gs,k} + V_{gd,k} - 2 \cdot V_{off,k}} \right)^2 + \frac{(V_{gd,k} - V_{off,k})(V_{gs,k} - V_{off,k}) + (V_{gs,k} - V_{off,k})^2}{V_{gs,k} + V_{gd,k} - 2 \cdot V_{off,k}} \]

\[ C_{gs,k} = -\frac{\partial Q_{g,k}}{\partial V_{s,k}} = -\frac{\partial Q_{g,k}}{\partial V_{gs,k}} \cdot \frac{\partial V_{gs,k}}{\partial V_{s,k}} = -\frac{\partial Q_{g,k}}{\partial V_{s,k}} \cdot \frac{\partial (V_{g,k} - V_{s,k})}{\partial V_{s,k}} = \frac{\partial Q_{g,k}}{\partial V_{gs,k}}; \]

\[ C_{gd,k} = -\frac{\partial Q_{g,k}}{\partial V_{d,k}} = -\frac{\partial Q_{g,k}}{\partial V_{gd,k}} \cdot \frac{\partial V_{gd,k}}{\partial V_{d,k}} = -\frac{\partial Q_{g,k}}{\partial V_{d,k}} \cdot \frac{\partial (V_{g,k} - V_{d,k})}{\partial V_{d,k}} = \frac{\partial Q_{g,k}}{\partial V_{gd,k}}; \]
II. QPZD transistor model

Noise Model

Equivalent circuit model

Channel thermal noise

\[ S_{Lg} = 4kT_{ch} \omega^2 W r^2 C_g^2 \left( \frac{W^4 \mu^4 C_g^4 A_g^2}{I_d^5 L^2} A_{id} - \frac{2W^3 \mu^3 C_g^3 A_g}{I_d^4 L} B_{lg} + \ldots \right) \]

Gate-induced noise

\[ S_{Lg} = \frac{4kT_{ch} W^2 C_g^2 \mu_{eff}^2}{I_d^2} \left[ (V_L - V_{si})^2 V_{go}^2 - (V_L^2 - V_{si}^2) V_{go} + \frac{1}{3} (V_L^3 - V_{si}^3) \right] \]

Noise correlation

\[
C = \frac{S_{g1g}}{\sqrt{S_{Lg} S_{Ld}}} = -j \left( \frac{A_{lg} A_{id} - I_d L}{W \mu C_g} B_{lg} \right) \sqrt{A_{id} \left( A_{lg}^2 A_{id} - \frac{2I_d L}{C_g \mu W} A_{lg} B_{lg} + \frac{I_d^2 L^2}{C_g^2 \mu^2 W^2} C_{lg} \right)}
\]

<table>
<thead>
<tr>
<th>Model</th>
<th>Fitting Parameter Number</th>
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<tr>
<td>Pucel</td>
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<tr>
<td>Pospieszalski</td>
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<tr>
<td>ASM-HEMT</td>
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</tr>
<tr>
<td>MVSG</td>
<td>3</td>
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<tr>
<td>This model</td>
<td>0</td>
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</table>
II. QPZD transistor model

Model Validation

- **Pulse-IV**
  - Simulated and Measured curves for $I_d$ vs. $V_{ds}$

- **Noise**
  - Simulated and Measured $N_{Fmin}$ vs. Frequency at 25°C

- **S parameter**
  - S21, S12, S11, S22 plots

- **Fundamental RF performance**
  - Gain and $P_{out}$ vs. $P_{in}$

- **Harmonic RF performance**
  - Harmonic $P_{out}$ vs. $P_{in}$

- **Linearity performance**
  - $P_{out}$ vs. $P_{in}$ at 10 MHz
II. QPZD transistor model

Device Co-optimization

Technical Parameter Analysis

- Barrier thickness
  - $P_{in} = P_{3dB}$

- Al mole fraction
  - $P_{in} = P_{3dB}$

Thermal Management

- MSL structure
- ISV structure
- Channel temperature
  - Ambient temperature: 25°C
  - Modeled (MSL):
    - By Ansys (MSL)
    - Modeled (MSL)
II. QPZD transistor model

Device Co-optimization for MMIC

In house parameters extraction

PDK for EDA tools

GaN MMIC optimization
I. Introduction

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V. Conclusion
III. Statistical model and yield optimization

**Statistical model**

- **Process fluctuation**
- **Output variation**
- **Low yield circuit design in some cases**

### Golden Die
- Data-based
- Poor extrapolation

For circuit evaluation

### TCAD Model
- Fully physical
- Time expensive

For device optimization

### Physical-based Model
- Physically interpretable
- Fast simulation

Co-optimization
III. Statistical model and yield optimization

QPZD Statistical Model

\[ \tilde{X} = \mu_X + \sigma_X \left( \sum_{i=1}^{3} L_i F_i + \varepsilon_X \right) \quad (X = d, v_{\text{max}}, \mu_{\text{sat}}, n_s) \]

Physical parameters variation modeling

\[ I_{ds} = I_{max} V_{ds} \left( 1 + \lambda V_{ds} \right) \frac{1}{\sqrt{E_{\text{eff}}}} \left[ \beta \left( l_s + l_d + E_{\text{eff}} l_g + V_{ds} \right) \right]^\beta \]

QPZD nonlinear model

Parameter extraction flowchart

Characterization of the fluctuation
III. Statistical model and yield optimization

GaN MMIC Yield Optimization

Traditional Method

New Method

A load-pull method considering both output and yield using statistical model

Circuit tuning

Yield evaluation

Circuit yield optimization by iterative design in DOE

Pout contours in Smith chart

Yield contours in Smith chart

Mean of Pout

Zcircuit=15.6+j40.2

32 GHz

Zmaxyield=11.1+j40.1

Zcircuit=15.6+j40.2

32 GHz
III. Statistical model and yield optimization

GaN MMIC Yield Optimization

Yield load-pull flowchart

Boundary setting
Optimum impedance considering yield and output performance

 specifications check

Yes

Obtain optimum $Z_L$

Select $Z_L$ accounting for satisfying output and yield

Calculate yield, $\tilde{P}_{out}$ and $\tilde{\eta}_{PAE}$ at selected $Z_L$

Draw constant $\tilde{P}_{out}$ and $\tilde{\eta}_{PAE}$ contours in the Smith chart

Draw constant yield contours in the Smith chart

Calculate $\tilde{P}_{out}$ and $\tilde{\eta}_{PAE}$ at each $Z_L$

Calculate yield at each $Z_L$

Determine boundary parameters in yield criteria

Set up $Z_L$ sweep range in the Smith chart

Probability

Probability

Probability

21.85
20.45
19.05
18.35

29.5
29.7
29.9
30.1
30.3
30.5

Pout (dBm)

$P_{out_{min}}$
$\eta_{PAE_{min}}$

Pass

Fail

Pass

Fail

$P_{out_{max}}$
$\eta_{PAE_{max}}$

Case 1

Min

Max

0
20
40
60
80
100 %

Min

Max

0
10
20
30
40
50

dBm

%
III. Statistical model and yield optimization

GaN MMIC Yield Optimization

32~38GHz 15W GaN PA

<table>
<thead>
<tr>
<th>Boundary</th>
<th>Values</th>
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<tbody>
<tr>
<td>Poutmin</td>
<td>43dBm</td>
</tr>
<tr>
<td>Gainmin</td>
<td>16dB</td>
</tr>
<tr>
<td>Gainmax</td>
<td>18dB</td>
</tr>
<tr>
<td>PAEmin</td>
<td>31%</td>
</tr>
<tr>
<td>Yield</td>
<td>81.3%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Values</th>
<th></th>
<th></th>
</tr>
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<tbody>
<tr>
<td>42dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18dB</td>
<td>30%</td>
<td>98.2%</td>
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</table>

13% improvement comparing with conventional method

300 samples
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GaN MMIC IP model

MMIC IP model for EDA tools

Junction temperatures Vs. Pin & RF frequency

Performance
IV. Circuit IP model

Electro-thermal Analysis of GaN MMIC

Thermal analysis of PA with package
IV. Circuit IP model

Electro-thermal(Eth) Analysis of GaN MMIC

2~6 GHz 10W GaN PA

Thermal distribution (Mo-Cu heat sink)

Thermal distribution (QFN package)

Pout Vs. ambient temperatures

Pout Vs. packages

2 GHz

0°C

75°C

6 GHz

Ideal

Mo-Cu

QFN
IV. Circuit IP model

Electro-thermal Analysis of GaN MMIC

2~6 GHz GaN LNA

Thermal distribution (Mo-Cu heat sink)

Thermal distribution (QFN package)

NF Vs. temperatures

NF Vs. packages
IV. Circuit IP model

Electro-thermal Analysis of GaN T/R MMIC

![Power Amplifier](image1)

![Low-noise Amplifier](image2)

![Switch](image3)

T - transmitter

R - Receiver

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Graph 1</th>
<th>Graph 2</th>
<th>Graph 3</th>
<th>Graph 4</th>
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<tr>
<td>Gain (dB)</td>
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<td>P1dB (dBm)</td>
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<td>P1E (%)</td>
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<td>S11 (dB)</td>
<td><img src="image16" alt="Graph" /></td>
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<td>S21 (dB)</td>
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<td><img src="image21" alt="Graph" /></td>
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<td>NF (dB)</td>
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<td><img src="image25" alt="Graph" /></td>
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<td>S21 (dB)</td>
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<td><img src="image34" alt="Graph" /></td>
<td><img src="image35" alt="Graph" /></td>
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V. Conclusion
V. Conclusion

- The design technology co-optimization (DTCO) for RF EDA is introduced taking GaN MMIC for example.
- The physics-based nonlinear transistor model can realize a good mapping between physical parameters and circuit electrical performance.
- The statistical model can realize a good mapping between process variation and circuit yield.
- The DTCO and STCO will be useful for next generation of RF design.
References

Thank you for your attention!