Compact Modeling for Transistors Accommodating Inner Thermal Feedback Behavior

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Context

- Background
  - Theory and Derivation
  - Model Development
    - FinFET Device Modeling
  - Extended Application
- Summary
Self-heating Effect in Transistors

- **DC Behaviors:** device temperature rise, reduction in on-current.....
- **Frequency Behaviors:** long signal delays, oscillation, inductive in-/output-impedance.....

Freq: 100KHz to 3.1GHz

Commonly Used Thermal Sub-circuit
Commonly Used Small-signal Model for Transistors

- Model normally extracted at hi-frequency, e.g. No thermal effect considered;
- For FinFETs application, the frequency range of thermal effect can high to ~1GHz, strong thermal effect can not be omitted in device modeling.

Small-signal model for Si-FET devices.

Fig. 1 Comparison of the model simulated (solid lines) and measured (symbols) $Y$-parameters ($Y_{21}$) of a FinFET device at $I_{be} = 2 \times 10^{-4}A$, $V_{ce} = 1.2$ V.
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Derivation of the Network Parameters with Thermal Effect

\[ P_{\text{diss}} = I_1 V_1 + I_2 V_2 \]

\[ T = f(t) \]

**Fig. 2** Voltages and currents in a two-port network.

**P1:** Thermal Isolated Part, \( T = T_{\text{nom}} \)

**P2:** Instance Temperature Dependent Part, \( T = T_{\text{nom}} + T_{\text{rise}} \)

**P3:** Self-heating Dependent Part, \( T = T_{\text{nom}} + Z_{\text{th}} P_{\text{diss}} \)

\[ I_1 = f_1(V_1, V_2, T) \]

\[ I_2 = f_2(V_1, V_2, T) \]

\[ V_t = Z_{\text{th}} P_{\text{diss}} \]
Y-parameters Accommodating Self-heating Behavior

\[ y_{mn} = \frac{dI_m}{dV_n} = \frac{\partial f_m}{\partial V_n} + \frac{\partial f_m}{\partial T} \frac{dT}{dV_n} \]

For P3:

\[ dT = Z_{th} dP_{diss} \]

\[ P_{diss} = I_1 V_1 + I_2 V_2 \]

\[ \frac{dP_{diss}}{dV_n} = Z_{th} \frac{dP_{diss}}{dV_n} \]

\[ dP_{diss} = I_1 dV_1 + V_1 dI_1 + I_2 dV_2 + V_2 dI_2 \]

For \( y_{m1} \), \( dV_2 = 0 \); for \( y_{m2} \), \( dV_1 = 0 \)

\[ y_{mn} = \frac{y_{mn}^* + M_m Z_{th} I_m I_n}{1 - M_m Z_{th} P_{diss}} \]

(Ref. O. Mueller, 1964)

Fig. 3 General thermal equivalent circuit

\[ Z_{th} = \sum_{k=1}^{p} Z_{thk} = \sum_{k=1}^{p} R_{thk} / (1 + j \omega R_{thk} C_{thk}) \]
Compact Model Development

\[ y_{mn} = \frac{y_{mn}^* + M_m Z_{th} I_m I_n}{1 - M_m Z_{th} P_{diss}} \]

**Only DC consideration:**

\[ D_{ij} = -M_i (P_{diss} I_i / V_i + I_i I_j) \]

\[ y_{mn}^* = y_{mn} - Z_{th} M_m \left( y_{mn} P_{diss} + I_m I_n \right) = y_{mn} + Z_{th} D_{mn} \]

\[ Z_{th} = \sum_{k=1}^{p} Z_{thk} = \sum_{k=1}^{p} \left( R_{thk}^{-1} + j \omega R_{thk} C_{thk} \right)^{-1} \]

\[ Z_{th} D_{mn} = D_{mn} \sum_{k=1}^{p} Z_{thk} = \sum_{k=1}^{p} \left( D_{mn} R_{thk} \right)^{-1} + j \omega C_{thk} D_{mn}^{-1} \]

\[ y_{mn}^* = y_{mn} + \sum_{k=1}^{p} \left( R_{mnk}^* + j \omega L_{mnk}^* \right)^{-1} \]

Enables complete small-signal model for transistors.
Small-signal Model Topology Development

Fig. 4 Complete small-signal model for transistors with thermal feedback caused by self-heating effect.

\[
y_{t, mn} = \sum_{k=1}^{p} \left( R_{mnk}^* + j\omega L_{mnk}^* \right)^{-1}
\]

\[
y_2^* = y_2 + \sum_{k=1}^{p} \left( R_{21k}^* + j\omega L_{21k}^* \right)^{-1}
\]

\[
g_m^* = g_m + \sum_{k=1}^{p} \left( R_{21k}^* + j\omega L_{21k}^* \right)^{-1}
\]
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FinFET Devices Modeling

- For FinFET devices, \( I_1 = I_{\text{gate}} < 1.0 \times 10^{-9} \text{ A} \), self-heating is mainly caused by \( I_2 = I_{ds} \)

\[
\frac{dP_{\text{diss}}}{dt} \text{ can be simplified to } \frac{dP_{\text{diss}}}{dt} = I_2 dV_2 + V_2 dI_2
\]

\( y_{t\_11} \) and \( y_{t\_12} \) are then can be omitted.

\[
g_m = g_m^* \left[ 1 + \sum_{i=1}^{n} k_{s\_hi} / (1 + j \omega \tau_{s\_hi}) \right]
\]

\( k_{s\_hi} = -M_2 P_{\text{diss}} R_{\text{hi}}, \ \tau_{s\_hi} = R_{\text{hi}} C_{\text{hi}}, \)

Figure 5. Proposed small-signal model for FinFETs
Self-heating effect is a low frequency behavior, HF elements can be extracted from \( Y_{|HF} \) at first, the thermal feedback elements are then can be extracted from low frequency \( Y \)-parameters, \( Y_{|LF} \), analytically.

- \( R_s, R_s \) and \( R_g \) are extracted by using the methods proposed in [10]. Bias condition \( V_{ds} = 0 \) V and \( V_{gs} = 0.9 \) V is used.
- Once the terminal elements are extracted, the inner \( y \)-parameters are used to extract inner elements.
Thermal Feedback Elements Extraction

\[ dY = Y_{HF}(2, 2) - Y_{LF}(2, 2) = \sum_{k=1}^{p} (R_{22k}^* + j\omega L_{22k}^*)^{-1} \]

\[ dY = Y_{HF}(2, 1) - Y_{LF}(2, 1) = \sum_{k=1}^{p} (R_{21k}^* + j\omega L_{21k}^*)^{-1} \]

**TABLE I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Extracted Value</th>
<th>Optimized Value</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{g/d/s} ) (Ω)</td>
<td>91.6, 37, 24.5</td>
<td>94.9, 39.8, 21.4</td>
<td>3.6, 7.5, 12.6</td>
</tr>
<tr>
<td>( R_{sub} ) (kΩ), ( \tau ) (pS)</td>
<td>2.295, 1.06</td>
<td>2.21, 0.92</td>
<td>4.1, 13.2</td>
</tr>
<tr>
<td>( C_{gs/d} ) (fF)</td>
<td>11.45, 5.5911.46, 5.390.8, 3.5</td>
<td>11.46, 5.39</td>
<td>0.8, 3.5</td>
</tr>
<tr>
<td>( C_{ds}, C_{sub} ) (fF)</td>
<td>1.02, 1.23</td>
<td>0.91, 1.34</td>
<td>10.7, 8.9</td>
</tr>
<tr>
<td>( *R_{t1/2/3} ) (kΩ)</td>
<td>204, 7.5, 8.4</td>
<td>198, 7.4, 8.6</td>
<td>2.9, 1.3, 2.3</td>
</tr>
<tr>
<td>( *L_{t1/2/3} ) (uH)</td>
<td>59k, 90, 24.6</td>
<td>57k, 87.6, 23.2</td>
<td>3.4, 2.7, 5.7</td>
</tr>
<tr>
<td>( g_{ds}, g_{m} ) (mS)</td>
<td>0.72, 28.1</td>
<td>0.71, 25.82</td>
<td>1.3, 8.1</td>
</tr>
<tr>
<td>( *\tau_{sh1/2/3} ) (nS)</td>
<td>290, 12.1, 2.9</td>
<td>266, 12.9, 2.7</td>
<td>8.2, 6.6, 6.9</td>
</tr>
<tr>
<td>( *k_{sh1/2/3} ) (× 10^{-3})</td>
<td>-13, 28.3, 21.6</td>
<td>-14.2, 26.5, 22.1</td>
<td>9.2, 6.3, 2.3</td>
</tr>
</tbody>
</table>

Initially Extracted and Optimized Values of the Model Parameters at Bias 1: Vgs =0.6 V, Vds =0.9 V. RMS Error = |Extracted Value – Optimized Value| / Extracted Value ×100%.

Model Parameters for SHE Characterization Only are Marked with Symbol *.
Model Verification

- Bulk FinFET, 4-Fin N-MOSFET with a total number of fingers $N_f = 32$ and gate length $L = 16 \text{ nm}$, is fabricated using SMICs 14 nm bulk standard technology.

- A roughly frequency, $f_{sh} = 0.75 \text{ GHz}$ can be observed in the image parts of $Y_{21}$ and $Y_{22}$ where self-heating effect is negligible when $\text{freq} > f_{sh}$.

Fig. 6. Comparison of the model simulated with (solid lines) / without (dashed lines) SHE and measured (symbols) $Y$-parameters at $V_{gs} = 0.6 \text{ V}$, $V_{ds} = 0.9 \text{ V}$. 
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Summary and Discussion

- A novel small-signal model for transistors accommodating self-heating behavior is presented.
- Based on the model theory, a method to accurately extract the thermal model of transistors is proposed.
- Discussion: Is the thermal model can be extracted from Pulse IV?
  - Thermal isolated testing: the time width of the pulse must less than $1/(2\pi f_{sh})$;
  - $R_{thi}$ and $C_{thi}$ can not be extracted from Pulse IV.

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<td>Extracted FinFET thermal Model Parameters at Bias: $V_{gs} = 0.6$ V, $V_{ds} = 0.9$ V.</td>
</tr>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>-----------</td>
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<td>$\tau_{sh1/2/3}$ (nS)</td>
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Thanks!