ASCENT

European Nanoelectronics Infrastructure Access

Nicolás Cordero
The Challenge

- Cost/performance returns by scaling are diminishing
- Cost to achieve tape out on new nodes is increasing

**Stuttering**
- Transistors per chip, '000
- Clock speed (max), MHz
- Thermal design power*, W

**This can’t go on**
Design cost by chip component size in nm, $m

Sources: Intel; press reports; Bob Colwell; Linley Group; IB Consulting; The Economist

*Maximum safe power consumption
A truly unique opportunity:

ASCENT combines Tyndall, imec and CEA-Leti’s nanofabrication & electrical characterisation capabilities into a single research infrastructure and makes it accessible to all
Objectives

ASCENT will:

- Leverage Europe’s Unique advantage in nanofabrication to strengthen modeling and characterisation research community
- Accelerate development of advanced models at scales of 14nm and below
- Provide characterisation community with access to advanced test chips, flexible fabrication and advanced test and characterisation equipment
- Make project outputs available and easily accessible to nanoelectronics research community

ASCENT offers simplified access to advanced technology and research infrastructure
>220 members of ASCENT Network
Committee Membership

Industry Innovation Committee

- Bernie Capraro
  - Intel
- Patrick Drennan
  - Qualcomm
- Ronald Gull
  - Synopsys
- Dominique Thomas
  - ST Microelectronics

Users Committee

- George Angelov
  - TU Sofia
- Asen Asenov
  - Uni Glasgow
- Francisco Gamiz
  - Uni Granada
- Benjamin Iñiguez
  - Uni Rovira i Virgili
- Andreas Schenk
  - ETH
State-of-the-art 14 nm bulk FDSOI CMOS
Advanced transistor and interconnect test structures
Electrical & nano-characterization platforms

Fabrication facilities for nanowires & 2D materials
Advanced nanowire and nano-electrode test structures
Electrical & nano-characterization platforms

State-of-the-art 14 nm FinFET CMOS
Advanced transistor and interconnect test structures
Electrical & nano-characterisation platforms

www.ascent.network
• Test wafer/chips
• Electrical Characterisation
• Physical Characterisation
• Nanoscale non-standard fabrication
• 14nm technology data (Virtual Access)

www.ascent.network
FinFET 14/28nm Material for Device Analysis

• Test chips/wafers
  - 300mm wafers with Bulk FinFET devices (14nm)
  - 300mm wafers with Planar Metal Gate devices (28nm)
• Digital and Analog/RF existing test chips
• Complete suite of test structures for Reliability/ESD/Matching/Local Layout effects/…
• Standard devices up to circuit level [Ring-Oscillators, …]
• State-of-the-art bulk FinFET device baseline
• 300mm wafers with planar FDSOI and Nanowire devices
• SPICE models and model cards for digital: target and preliminary
  - 14nm FDSOI
  - 10nm FDSOI
  - 10nm FFSOI
• TCAD decks
  - FDSOI MOSFET
  - Trigate SOI Nanowire
  - GAA Nanowire MOSFET (mainly electrostatics)
• To come in the near future:
  - Spice model for Stacked NWs (7nm tech. node)
• >500 m² of test labs, ~ 25 semiauto/manual 300mm probers
• Statistical data treatment in JMP
• Fully and Semi-automatic 300mm parametric testers
• Temperature range for test on wafers 77/10K ➔ high T
• Fast Pulse testing, Self-Heating characterization
• HF tests up to 50 GHz
• Noise measurements
• Reliability tests: hot carriers, TDDB, charge pumping, ...
• High power tests (10kV, > 100A) on 300mm prober
• Electrostatic discharge LAB
- Parametric testers with 300mm full auto probers
- Probe cards and new membrane cards
- Statistical data treatment
- Functional tests
- General purpose I(V)-C(V) 200/300mm testers
- Temperature range for test on wafers: 2K ⇒ 600°C
- Test systems for memories
- HF tests up to 40 MHz
- Noise measurements
- Reliability tests: hot carriers, TDDB, charge pumping, ...
- Internal Photo Emission
- Emission microscopy (visible & infrared)
- Electrical test under calibrated strain
- High power tests (10kV, > 100A) on 300mm prober
- Deep Level Transient Spectroscopy
- Electrostatic discharges
- Electromigration
- Oven and climatic environments
### Electrical Characterisation Labs

<table>
<thead>
<tr>
<th>Lab Type</th>
<th>Description</th>
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<tbody>
<tr>
<td>Open Access Test Lab</td>
<td>Wide range of test equipment for device and wafer testing</td>
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<tr>
<td></td>
<td>e.g.: impedance, capacitance, voltage, current, spectrum analysers, ...</td>
</tr>
<tr>
<td>Nanoscale Test Lab</td>
<td>Variable Temperature, Micromanipulator Probe Stations</td>
</tr>
<tr>
<td>Reliability Test Lab</td>
<td>Wide range of test equipment for packaged devices</td>
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</tbody>
</table>
Physical Characterisation

- Atomic Force Microscopy
  - *Dimension AFM Icon/Fast Scan Bruker* working under glovebox (O2, H2O < 1 ppm)
- High Resolution Transmission Electron Microscopy
  - *FEI TECNAI G2 F 20*
  - *FEI TITAN THEMIS 80-200 kV*
- ToF-SIMS
  - *ION TOF ToF SIMS 5*
- Atom Probe Tomography
  - *CAMECA FlexTAP Atom probe*
- XRD (X-ray Diffraction)
  - *Diffractxometer - Smartlab RIGAKU - 5 circles*
- XPS (X-ray Photoelectron Spectroscopy)
  - *Spectrometer/microscope - PHI VERSA PROBE II*
- Ellipsometer
  - *Ultraviolet-visible ellipsometer - HORIBA JOBIN YVON UVISEL*
<table>
<thead>
<tr>
<th>Physical Characterisation Labs</th>
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<tr>
<td><strong>Electron Microscopy Facility</strong></td>
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<tr>
<td><strong>Nanoscale Characterisation</strong></td>
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<tr>
<td><strong>Optical Spectroscopy Labs</strong></td>
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<tr>
<td><strong>Magnetic Characterisation</strong></td>
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<tr>
<td><strong>Package Characterisation</strong></td>
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</table>
Nanoscale fabrication

Range of cleanrooms designed for flexible process & product development

- Silicon MOS Fabrication
- MEMS Fabrication
- Compound Semiconductor Fabrication
- Photonics Fab Training Facility
- e-beam Lithography
- Non-standard nano-processing
Complete nanotechnology lab in one tool

- High resolution pole piece - point-to-point resolution of 0.21 nm
- EDS, Oxford instruments, INCA 250, site-lock drift correction system for high resolution elemental mapping
- In-situ STM-TEM holders, high temperature TEM holders
- STEM mode with BF and HAADF detectors (0.8 nm resolution)
- Oxford Instruments X-MAX 80 for high productivity EDS analysis
- Cryo preparation for liquid and gel-like materials

JEOL 2100 HR-(S)TEM / FEI Helios NanoLab DB-FIB
Nanoscale Technology Data (Virtual Access)

- **FinFET and GAA test chip documentation and DATA (14nm)**
  - Documentation of process assumptions for the test chips
  - Inventory of test structure types available on the test chips
  - Access to test structures data

- **III/V InGaAs GAA test chip documentation and DATA**
  - Documentation of process assumptions for the test chips
  - Inventory of test structure types available on the test chips
  - Access to test structures data

- **PLANAR test chip documentation and DATA (28nm)**
  - Documentation of process assumptions for the test chips
  - Inventory of test structure types available on the test chips
  - Access to test structures data

- **FDSOI: PDK for Full custom IC design**
  - 14nm planar FDSOI technology
  - 10nm planar FDSOI technology (preliminary)
<table>
<thead>
<tr>
<th>Category</th>
<th>Description</th>
<th>Files</th>
</tr>
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<tbody>
<tr>
<td><strong>finFET imec</strong></td>
<td>Data for imec's finFET technology</td>
<td>- Bulk finFET DESCRIPTION&lt;br&gt;- Bulk finFET DATA&lt;br&gt;- Datatiles - Full Curves: IDVG/IDVD on NFIN/PFIN&lt;br&gt;- Bulk finFET Matching DATA&lt;br&gt;- Matching Data - Full curves and VT</td>
</tr>
<tr>
<td><strong>FDSOI Leti</strong></td>
<td>Data for Leti's FDSOI</td>
<td>- PDK LETI FDSOI 14nm&lt;br&gt;- Design Kit and Documentation</td>
</tr>
</tbody>
</table>
• Access to bulk finFET and GAA_SiNW data
  - Integrated dual WFM CMOS
  - LG range 24nm → 90nm within pitch and long channel devices
  - nFIN from 2 to 22

• Room T available
  - 50°C or higher T next
  - Low T can be considered

• DOE for contact, layout effects,…
• Access to raw data and extracted FoM’s
  - Threshold Voltage, Mismatch
  - DC metrics and ID-VD, ID-VG characteristics
  - FEOL/BEOL R/C and Ring-Oscillator circuits

• Full sweep data in VA
  - Covers range of VG/VD and LG/nFin

• Analog FoM, Reliability testing, ESD,…
• Available for subsequent model validation
PLANAR 14NM FDSOI TECHNOLOGY FOR BENCHMARKING

- CPP = 90nm
- Nominal supply voltage Vdd=1V

- **BEOL:**
  - Metal levels: Metal 1 to Metal 5,
  - Pitch = 64nm (similar to 20nm bulk)

- **MEOL:**
  - Trench contact
  - Metal0

- **FEOL:**
  - FDSOI transistor with Lmin = 20nm
  - Standard Well definition (similar to bulk) with possible back-biasing up to Vdd

- **DRM:**
  - simplified design rules
FULL CUSTOM DESIGN FLOW

- Parasitic extraction (PEX)
- RC Simulation
- Technology
- Design Library Simulation
  - Devices Library:
    - N/P FET (multi-VT)
    - Spice Modeling
  - DRM, Reference manuals
- Verification (DRC/LVS)
  - Design Rules Checking
  - Extraction Devices
- Layout
  - Parameterized cells
    (MOS Pcells)
- Electrical simulation for design performance (Schematic → Netlist)
- SPICE Model: library of MOSFET devices (UTSOI2) integrated
- Layout: physical implementation of all technological layers (Techfile)
- Pcell: library of parameterized MOSFET for layout automation
- Design Rules Check (DRC): deck file describing all design rules (DRM)
- Layout Versus Schematic (LVS): comparison layout vs simulation
- Parasitic EXtraction (PEX): extraction of parasitic elements (RC)
- Post-Layout Simulation (PLS): netlist simulation with RC elements
- Digital Library: preliminary basic logic cells for Power Performance Area (PPA) analysis, architecture definition (template)
LIBRARY NAME: DK_FDSOI14LIB

Library
- Technological file include technology, layer information, display and layer map files,
- Based on the OpenAccess Database

Symbol
- Symbol library contains 8 variants of device symbols for MOS => 8 n/p fet (SVT1/SVT2/LVT/HVT),
- Associated SPICE models for simulation

Pcell
- MOS parameterized cells available to reduce layout time and design rule mistakes,
- Pcells manage all kinds of MOS devices and all VT options

LVTFET
Parameters:
- l : 20nm
- w : 46nm
- nf : 1
- m : 1
SPICE MODEL FOR FDSOI: UTSOI2

- The UTSOI2 compact model was developed to describe the electrical behavior of FDSOI transistor: especially back biasing effect
- Several versions are available in major IC simulators (Eldo, Spectre, Hspice, ADS,...)
- The FDSOI MOSFET is a 4 pins device as bulk

Included in device library:
- Parasitic effects: Area SD region (AS-AD)
- Stressor effects: Continuous RX, Isolated MOS
- Pre-layout effects: R, C, R+C
MULTI-VT DESCRIPTION FOR BENCHMARKING

VT definition in PDK: several gate workfunctions

<table>
<thead>
<tr>
<th>VT</th>
<th>Description</th>
<th>Well for nFet</th>
<th>Well for pFet</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVT</td>
<td>Low-VT</td>
<td>N</td>
<td>P</td>
</tr>
<tr>
<td>SVT1</td>
<td>Standard-VT1</td>
<td>N</td>
<td>P</td>
</tr>
<tr>
<td>SVT2</td>
<td>Standard-VT2</td>
<td>P</td>
<td>N</td>
</tr>
<tr>
<td>HVT</td>
<td>High-VT</td>
<td>P</td>
<td>N</td>
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Multi-VT platform can be managed using several solutions:
- Poly-biasing: Lnom + x nm
- Back-biasing: for example +Vdd under nFet
- Gate workfunctions

Multi-VT strategy is foundry-dependent
Continuous RX: used for increasing devices performance

Poly pitch: value is 90nm

Special Construct: used for MEOL layers in dedicated areas. To highlight special construct, used the associated marker (MKR_SpeConst). This allows to waive a set of default rules and check some other specific design rules (see DRM for more details)

MKR_GateTie: this marker must be placed on poly regions. These gates are formed each time we want to abut 2 devices which don’t share the same active regions. The device we are getting is a transistor in OFF state called gate tie. With this marker, the LVS will be able to extract this device
Design Rules Checking (DRC)

- DRC deck file manage:
  - One-Dimensional check,
  - Multi-Dimensional check,
  - Interdependent Multi-Layer check

Layout Versus Schematic (LVS)

- MOS devices extraction:
  - VT option & Gate Tie device
  - Well-tie for Back-gate control
- MOS parameters extraction:
  - Geometry: l/w/nf/m
  - Area: as/ad/ps/pd
  - Stressor effects: sa/sb/sd
- Connectivity declaration

\[(x/X)^2 + (y/Y)^2 = 1\]
PARASITIC EXTRACTION FLOW (PEX)

POST-LAYOUT SIMULATION:

- Parasitic extraction files:
  - Technological and mapping files,
  - Nominal (corners not available)
- 2 descriptions: StarRC / xCalibrate,
- Ignore FEOL capacitances (SPICE)
- Metal resistance included

Description of the FDSOI cross-section:
- DIELECTRIC / CONDUCTOR / VIA

Technological information:
- THICKNESS / PERMITTIVITY / RESISTIVITY

Output: netlist including RC parasitic elements for PLS

Design Kit FDSOI 14nm | CIBRARIO Gérald | 2015 | 10
<table>
<thead>
<tr>
<th>Flow</th>
<th>CAD tools &amp; releases</th>
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<tbody>
<tr>
<td>Framework</td>
<td>Virtuoso (Cadence) release IC6.1.5.500.9</td>
</tr>
<tr>
<td>Simulator</td>
<td>Eldo (Mentor) release 13_2c</td>
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<td></td>
<td>HSPICE (Synopsys) release 2013.03-SP2</td>
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<tr>
<td>DRC/LVS</td>
<td>Calibre (Mentor) release 2015.1_14.11</td>
</tr>
<tr>
<td>PEX</td>
<td>Star-RC (Synopsys) release 2012.12-SP2</td>
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<td>Calibre (Mentor) release 2015.2.19.13</td>
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## Virtual Access Users

<table>
<thead>
<tr>
<th>Ref</th>
<th>User</th>
<th>Institute</th>
<th>Country</th>
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<tbody>
<tr>
<td>002</td>
<td>G. Angelov</td>
<td>T.U. Sofia</td>
<td>Bulgaria</td>
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<tr>
<td>006</td>
<td>G. Fatin</td>
<td>Univ. Maynooth</td>
<td>Ireland</td>
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<td>008</td>
<td>A. Durgaryan</td>
<td>Synopsys</td>
<td>Armenia</td>
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<td>022</td>
<td>A. Nejadmalayeri</td>
<td>Phoelex Ltd (SME)</td>
<td>UK</td>
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<td>X. Wang</td>
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<td>GlobalTCAD Solutions GmbH</td>
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<td>Ireland</td>
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<td>A. Pezzotta</td>
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<td>Switzerland</td>
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<td>062</td>
<td>L. Dobrescu</td>
<td>T.U. Bucharest</td>
<td>Romania</td>
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</tbody>
</table>
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Sign up:
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e-mail: paul.roseingrave@tyndall.ie
Phone: +353-21-2346268

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