Semiconductor Device Compact Modelling with Ageing Effects

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Motivation

- Transistors getting smaller
  - again
Motivation

- Transistors getting smaller
- Ageing effects
  - permanent (HCl)
  - temporary (BTI)
Motivation

- Transistors getting smaller
- Ageing effects
- Analogue case hardly covered
  - Digital case well understood
  - How does that help?
Motivation

- Transistors getting smaller
- Ageing effects
- Analogue case hardly covered
- Ageing simulation questionable
  - Vendor specific, blackbox based
  - Limited flexibility
Motivation

- Transistors getting smaller
- Ageing effects
- Analogue case hardly covered
- Ageing simulation questionable
- No compact modelling standard
  - Hard to create models
  - On any hierarchy level
Motivation

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- Ageing simulation questionable
- No compact modelling standard
A Transistor

\[ V_{\text{out}} \]

\[ \text{Zeit} [\mu s] \]

output [V]

sine

out
A Transistor

Ageing
A Transistor

Ageing
A Transistor

Ageing
Ingredients

- Material Constitution Model
  - Stress levels
  - Ageing processes
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- **Material Constitution Model**
  - Stress levels
  - Ageing processes
- **Component behavioural model**
  - Operating point dependency
  - Material dependency
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- **Compact modelling**
  - Language limitations
  - … and workaround
Ingredients

- **Material Constitution Model**
  - Stress levels
  - Ageing processes

- **Component behavioural model**
  - Operating point dependency
  - Material dependency

- **Compact modelling**
  - Language limitations
  - ... and workaround

- **Simulation**
  - Different time scales
  - Efficient model evaluation
Ingredients

- Material Constitution Model
  - Stress levels
  - Ageing processes
- Component behavioural model
  - Operating point dependency
  - Material dependency
- Compact modelling
  - Language limitations
  - ... and workaround
- Simulation
  - Different time scales
  - Efficient model evaluation
- Implementation
  - gnucap-uf (ageing simulation)
  - gnucap-adms (model compiler)
BTI Measurements

- Stress phase

\[ V_{\text{stress}} \]
BTI Measurements

- Stress phase
  \[ V_{\text{stress}} \]

- Measure phase
  \[ V_{\text{sweep}} \rightarrow 0.05 \text{ V} \]
BTI Measurements

- **Stress phase**

  \[ V_{\text{stress}} \]

- **Measure phase**

  \[ V_{\text{sweep}} \rightarrow 0.05 \text{ V} \]

- \[ \Delta V_{\text{th}} \sim \text{trap density} \]
BTI Measurements

- **Stress phase**
  \[ V_{\text{stress}} \]

- **Measure phase**
  \[ V_{\text{sweep}} \]
  \[ 0.05 \text{ V} \]

- \( \Delta V_{\text{th}} \sim \text{trap density} \)

- Not as meaningful in analogue circuits.
Dissecting a Transistor Model

- $|I_{ds}| = K \cdot |V_{gs} - V_{th}|^2$

- $I_{ds} \sim g \cdot V_{ds}$
Threshold voltage change, conventional model

\[ |I_{ds}| = K \cdot |V_{gs} - V_{th} - \Delta V_{th}|^2 \]

\[ I_{ds} \sim g_{\text{remain}} \cdot V_{ds} \]
Threshold voltage, the analogue case

\[ |V_{gd}| \]  
\[ |V_{th}| \]  
\[ |V_{gs}| \]  
\[ \Delta V_{th} \]  

\[ |I_{ds}| \sim g_{\text{remain}} \cdot |V_{ds}| \]
Threshold voltage, the analogue case

\[ |V_{gd}| \quad |V_{gs}| \]
\[ |V_{th}| \quad \Delta V_{th} \]

\[ \Rightarrow |I_{ds}| \sim g_{\text{remain}} \cdot |V_{ds}| \]
\[ \ldots \neq K \cdot |V_{gs} - V_{th} - \Delta V_{th}|^2 \]
Conventional Block Based Model

```
.model pfet_aged [...] vt=vt0+dvth
```

\[ \Delta V_{th} \]
Conventional Block Based Model

.model pfet_aged [..] vt=vt0+dvth

\[ \Delta V_{\text{th}} \]
Ageing Processes

- Map stress wave $L: [0, t] \rightarrow \mathbb{R}$ to ageing state.
- arithmetically simple (ideally).
Ageing Processes

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- Integrator

$$L \mapsto \int L \, dt$$
Ageing Processes

- Map stress wave $L: [0, t] \rightarrow \mathbb{R}$ to ageing state.
- Arithmetically simple (ideally).
- Integrator
- Controlled decay process

$$L \mapsto \exp \left( - \int \frac{1}{\tau(L(t))} dt \right)$$
Ageing Processes

- Map stress wave $L: [0, t] \to \mathbb{R}$ to ageing state.
- Arithmetically simple (ideally).
- Integrator
- Controlled decay process
- Reversely Coupled Decay (RCD) process

\[
\tau_c(L) = \exp(k_c - m_c L)
\]

\[
\tau_e(L) = \exp(k_e + m_e L)
\]
Process Based Ageing Effect Model

- In Verilog-A
  - additional discipline
  - no language extension required
  - but extra semantics
  - transport stress and ageing states
Process Based Ageing Effect Model

- In Verilog-A
  - additional discipline
  - no language extension required
  - .. but extra semantics
  - transport stress and ageing states

- Declaration
  ```verilog-a
  discipline degradational
    potential Damage;
    flow Stress;
  enddiscipline
  nature Damage
    units = "1";
    access = State;
  endnature
  nature Stress
    units = "1";
    access = Level;
  endnature
  ```
Process Based Ageing Effect Model

- In Verilog-A

- Declaration
  discipline degradational [..]

- BTI Subdevice
  module bti_traps(p, n, d);
    electrical p, n; // electrical field
    degradational d; // defect density
    degradational n1, n1;
    rcd_exp #([..]) rcd1 (p, n, n1);
    rcd_exp #([..]) rcd2 (p, n, n2);
    analog begin
      @ ( initial_step ) begin
        State(d) <+ 0; // fresh.
      end
      State(d) <+ w1*State(n1) + w2*State(n2);
    end
  endmodule
Process Based Ageing Effect Model

- In Verilog-A

- Declaration

  discipline degradational [..]

- BTI Subdevice

  module bti_traps(p, n, d);

  [..]

  rcd_exp #([parameters ..]) rcd1 (p, n, n1);
  rcd_exp #([parameters ..]) rcd2 (p, n, n2);
  [..]

  endmodule

- Parameters: machine learning.
Process Based Ageing Effect Model

- In Verilog-A
- Declaration
  discipline degradational [..]
- BTI Subdevice
  module bti_traps(p, n, d);
    [..]
    rcd_exp #([parameters ..]) rcd1 (p, n, n1);
    rcd_exp #([parameters ..]) rcd2 (p, n, n2);
    [..]
  endmodule
- Parameters: machine learning.
- Processes: implemented in/for gnucap-uf
module ageing_mosfet(d, g, s, b);
    electrical d, g, s, b;
electrical ch; // channel mid
degradational a1, a2, a3; // 3 ageing nodes
bti_traps bti0(s, g, a1);
bti_traps bti1(ch,g, a2);
bti_traps bti2(d, g, a3);
[..]
analog begin
    analog begin
        Level(a1) <+ V(g,s);
        Level(a2) <+ V(g,ch);
        Level(a3) <+ V(g,d);

        // channel segmentation
        green = f(V(d), V(g), V(s), V(b)
                   State(a1), State(a2), State(a3));

        I(d,s) += green * V(d,s);
    end
endmodule
```verilog
module ageing_mosfet(d, g, s, b);
    electrical d, g, s, b;
    electrical ch; // channel mid
    degradational a1, a2, a3; // 3 ageing nodes
    bti_traps bti0(s, g, a1);
    bti_traps bti1(ch, g, a2);
    bti_traps bti2(d, g, a3);
    [...] // analog begin
    analog begin
        Level(a1) <+ V(g, s);
        Level(a2) <+ V(g, ch);
        Level(a3) <+ V(g, d);

        // channel segmentation
        green = f(V(d), V(g), V(s), V(b)
                  State(a1), State(a2), State(a3));

        I(d,s) += green * V(d, s);
    end
endmodule
```
Run inverter circuit on sine wave
- Compute $I_{ds}/V_{gs}$ dc-characteristic

Same $\Delta V_{th}$, still different
Thank You.