Infrastructure underpinning advanced nanoelectronics design

ESSDERC ESSCIRC
Leuven, Belgium 2017

Jim Greer and Julie Donnelly
Paul Roseingrave, Nicolas Cordero, Brendan Sheenan, Graeme Maxwell
The Challenge

Cost/performance returns by scaling diminishing
Cost to achieve tape out on new nodes increasing
The Challenge

Nanowire Transistors,
Colinge & Greer,
Cambridge University Press 2016
A part of the solution ...

... an infrastructure for the **global** nanoelectronics modeling, characterization, and design communities
The Access Providers

State-of-the-art 14 nm bulk FDSOI CMOS
Advanced transistor and interconnect test structures
Electrical & nano-characterization platforms

Fabrication facilities for nanowires & 2D materials
Advanced nanowire and nano-electrode test structures
Electrical & nano-characterization platforms

State-of-the-art 14 nm FinFET CMOS
Advanced transistor and interconnect test structures
Electrical & nano-characterisation platforms

www.ascent.network
Material for Device Analysis

300mm wafers with planar FDSOI and Nanowire devices

SPICE models and model cards for digital: target and preliminary
- 14nm FDSOI
- 10nm FDSOI
- 10nm FFSOI

TCAD decks
- FDSOI MOSFET
- Trigate SOI Nanowire
- GAA Nanowire MOSFET (mainly electrostatics)

To come in the near future:
- Spice model for Stacked NWs (7nm tech. node)
Access to LETI 300mm wafers with Nanowire devices for characterization and study of advanced nanodevices in the characterization facilities of the Nanoelectronics Lab of UGR.
Tyndall FlexiFab

Range of cleanrooms designed for flexible process & product development

- Silicon MOS Fabrication
- MEMS Fabrication
- Compound Semiconductor Fabrication
- Photonics Fab Training Facility
- e-Beam Lithography
- Non-standard nano-processing

Tyndall

Silicon MOS, MEMS, Compound Semiconductor, Photonics, e-Beam, Non-standard nano-processing
Fab Access
Access to Tyndall FlexiFab for non-standard processing

Test Chips
Si nano-wire test chips with range of devices

Electrical Characterisation Access
Access to Tyndall electrical test labs

Physical Characterisation Access
Access to Tyndall device characterisation facilities
Imec’s offer

Access to state of the art process technology

- Fin & STI module
- NFET wells I/I
- PFET wells I/I
- Well RTA
- Dummy gate
- NFET extension I/I
- PFET extension I/I
- Extension RTA
- NFET SiN dep & etch
- NFET recess
- NFET epi
- PFET SiN dep & etch
- PFET recess
- PFET epi
- Laser anneal
- ILD0
- RMG
- LI and BEOL
- 8..10 nm finCD
- 45nm Fin Pitch

State-of-the-art devices with dedicated experiments ready on 300mm Silicon wafers.

Main features: Bulk finFET, Replacement Metal Gate, S/D epi with Local Interconnect and silicide-last integration using single metal BEOL
Imec’s offer

Material for Device Analysis

- 300mm wafers with Bulk FinFET devices
- Silicon EPI nFET/pFET CMOS fully integrated vehicle
- Embedded Si:P / SiGe S/D CMOS fully integrated vehicle
- Replacement Metal Gate [RMG] with Local Interconnect
- Single level BEOL metal
- Digital and Analog/RF existing test chips
- Complete suite of test structures for Reliability/ESD/Matching/Local Layout effects/…
- Standard devices up to circuit level [Ring-Oscillators, …]
- State-of-the-art bulk FinFET device baseline

iFET test chip documentation

- Documentation of process assumptions for the test chips
- Inventory of test structure types available on the test chips
- Access to test structures data

Electrical Characterization Capabilities

- >500 m² of test labs, ~25 semi-auto/manual 300mm probers
- Statistical data treatment in JMP
- Fully automatic 300mm parametric testers
- Semi-automatic 300mm parametric testers
- Temperature range for test on wafers 77/10K → high T
- Fast Pulse testing, Self-Heating characterization
- HF tests up to 90 GHz
- Noise measurements
- Reliability tests: hot carriers, TID/D, charge pumping, …
- High power tests (10kV, >100A) on 300mm prober
- Electrostatic discharge LAB

STD Test-chip Content

- Testchip Documentation and Simulation
- State-of-the-Art Device

- SPICE models and model cards for digital
- SPICE models for Layout effect

Scientific & technical support

- Whenever necessary and upon request of the User, Imec can offer scientific support for in-depth data interpretation.
Developing new offering for the community

Development of Device Forensic Techniques & Contaminant Assessment for <14nm CMOS devices

- Investigate *new device forensic techniques* for sub-14nm devices using partners exemplar devices structures.
- Investigate *contamination effects* on shrinking gate dimensions and the impact of new geometries on contaminant tolerance.
- Perform a *baseline assessment of contaminants*: investigate levels at which the contaminants destroy chips and current contaminant control techniques.

Goals
- improve understanding of advanced device characterisation techniques by assessing new processes and tooling
- undertake trials using test vehicles at these new dimensions
- make the *results* and *test vehicles* available to the wider nanoelectronics community
Data on InGaAs / Al₂O₃ samples provided to the partners on V.A.
Example of electrical characterisation data

CV-GV measurements provided to the partners on V.A. for parameter extraction

- **9_150nm_Al87**
  - $C$ [F/m²]
  - $V_g$ [V]
  - 1kHz
  - 1MHz

- **9_150nm_Al87**
  - $G$ [S/m²]
  - $V_g$ [V]
  - 1kHz
  - 1MHz

- **C @ V_g=2.0V [F/m²]**
  - $t_{ox}=4.0nm$
  - $t_{ox}=5.7nm$
  - $t_{ox}=8.2nm$
  - $t_{ox}=9.3nm$
  - $\omega$ [rad/s]

- **T**
  - 4.2K, 10K, 30K, 50K, 75K, 100K, 125K, 150K, 175K, 200K, 250K, 300K

**cryogenic prober**
How to Access

Step 1: Sign Up
Step 2: Enquire
Step 3: Apply
Step 4: Selection
Step 5: Access
Step 6: Report
Step 1- Sign-Up

Sign-up Form

Please fill your details below. By signing up, you become a member of the ASCENT network. Members will receive specific information by e-mail on ASCENT technologies, details about upcoming events and news.

For a more detailed technical enquiry regarding access, please fill the ASCENT Enquiry form.

Your name *
Your e-mail address *
Comments
How did you hear about ASCENT?

Sign Up
252 members of ASCENT Network
Step 2 - Enquire

For a detailed technical enquiry regarding access, please fill your details below. To become a member of the ASCENT network, please fill the ASCENT Sign-up form instead.

ASCENT Enquiry Form

- Name
- Position
- e-mail
- Phone no
- Organisation
- Website
- Organisation type
- Sector / Activity
- Address 1
- Address 2
- City
- Postcode
- Country

1 minute ASCENT overview

Tweets by ASCENTeu

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Step 3 - Apply

ASCENT
Access Application Form

Requested Access
Summary / Abstract (incl. relevance to State of the Art)*

Current Research
Research Area*
Research background
(State of the Art)

Current project (if any)
Current project funding
Public (EU, National, ...), Industry

Research team
Describe your research team and team research record
<table>
<thead>
<tr>
<th>Ref No</th>
<th>Name</th>
<th>Affiliation</th>
<th>Country</th>
<th>Access To</th>
<th>Title/Objectives</th>
<th>Effort (p.d.)</th>
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<tbody>
<tr>
<td>010</td>
<td>Carlos Márquez</td>
<td>Univ Granada</td>
<td>Spain</td>
<td>Tyndall</td>
<td>Electrical characterisation of rGO</td>
<td>9</td>
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<tr>
<td>011</td>
<td>Gerard Ghibaudo</td>
<td>Minatec INPG</td>
<td>France</td>
<td>imec</td>
<td>14nm bulk FinFET test wafers for transport parameter and statistical LFN studies</td>
<td>8</td>
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<tr>
<td>023</td>
<td>Mircea Dragoman</td>
<td>IMT Bucharest</td>
<td>Romania</td>
<td>Tyndall</td>
<td>Deposition of low roughness metal for MIM application</td>
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<tr>
<td>029</td>
<td>Liang Ye</td>
<td>Univ Twente</td>
<td>Netherlands</td>
<td>Tyndall</td>
<td>Si nanowires for Monolayer Doping (MLD) Experiment</td>
<td>7.5</td>
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<tr>
<td>030</td>
<td>Enrique Miranda</td>
<td>U.A. Barcelona</td>
<td>Spain</td>
<td>Tyndall</td>
<td>Characterisation of electrically stressed high-k dielectrics for 2D III-V MOSFETs</td>
<td>13</td>
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<td>034</td>
<td>Rotislav Rusev</td>
<td>TU Sofia</td>
<td>Bulgaria</td>
<td>Tyndall</td>
<td>Fabrication of nanoscale fingers for SAW tweezers</td>
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<td>042</td>
<td>Francisco Gámiz</td>
<td>Univ Granada</td>
<td>Spain</td>
<td>Leti</td>
<td>Simulation &amp; characterization of SOI devices</td>
<td>15</td>
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<td>044</td>
<td>Rosaria Puglisi</td>
<td>CNR-IMM</td>
<td>Italy</td>
<td>Tyndall</td>
<td>Molecular Doping of Si Nanowires</td>
<td>9</td>
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<td>048</td>
<td>Drago Strle</td>
<td>Univ Ljubljana</td>
<td>Slovenia</td>
<td>Tyndall</td>
<td>Comb capacitor with nanoscale finger width/spacing</td>
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<tr>
<td>050</td>
<td>Peter Schuffelgen</td>
<td>FZ Julich</td>
<td>Germany</td>
<td>Tyndall</td>
<td>TEM investigation of topological insulators</td>
<td>10</td>
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<tr>
<td>Ref No</td>
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<td>054</td>
<td>Artola Laurent</td>
<td>ONERA</td>
<td>France</td>
<td>imec</td>
<td>Characterization of radiation effects in 14nm FinFET Technology</td>
<td>40</td>
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<td>055</td>
<td>Nobuyuki Takeyasu</td>
<td>Okayama University</td>
<td>Japan</td>
<td>Tyndall</td>
<td>Characterisation of 2D metal nanoparticle array</td>
<td>12</td>
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<tr>
<td>059</td>
<td>Alexei Nazarov</td>
<td>Lashkaryov Institute of Semiconductor Physics</td>
<td>Ukraine</td>
<td>Tyndall</td>
<td>Low-T hydrogen plasma treatment of III-V MISFETs</td>
<td>10</td>
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<tr>
<td>064</td>
<td>Takashi Teranishi</td>
<td>Okayama University</td>
<td>Japan</td>
<td>Tyndall</td>
<td>Nanoscale TLs for ferroelectric characterisation</td>
<td>12</td>
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<td>069</td>
<td>Gioele Mirabelli</td>
<td>Tyndall National Institute</td>
<td>Ireland</td>
<td>Leti</td>
<td>Atom Probe Tomography of 2D protrusions</td>
<td>5</td>
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<tr>
<td>070</td>
<td>Maart van Druenen</td>
<td>University College Cork</td>
<td>Ireland</td>
<td>Leti</td>
<td>SIMS Analysis of Molecular Doped Samples</td>
<td>2</td>
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<td>073</td>
<td>Ray Duffy</td>
<td>Tyndall National Institute</td>
<td>Ireland</td>
<td>Leti</td>
<td>Atom Probe Tomography of Dense Pitch Si Nanowires</td>
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<td>074</td>
<td>Panagiotis Dimitrakis</td>
<td>Institute of Nanoscience and Nanotechnology</td>
<td>Greece</td>
<td>Leti</td>
<td>Carrier Mobility-Noise measurements on SOI-FinFETs</td>
<td>7</td>
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<tr>
<td>075</td>
<td>Prof. Jaume Segura</td>
<td>Universitat Illes Balears</td>
<td>Spain</td>
<td>imec</td>
<td>Radiation induced transients on 14nm FinFETs</td>
<td>40</td>
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<tr>
<td>077</td>
<td>Assistant Prof. Grande Marco</td>
<td>Politecnico di Bari</td>
<td>Italy</td>
<td>Tyndall</td>
<td>Fabrication of High Q-factor Asymmetric Nanobeams</td>
<td>41</td>
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<tr>
<td>087</td>
<td>Assistant Prof. Jae Woo, LEE</td>
<td>Korea University</td>
<td>South Korea</td>
<td>Leti</td>
<td>Low Frequency Noise study on PMOS SiGe Omega FET</td>
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</tbody>
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### Sample TA User Profiles

<table>
<thead>
<tr>
<th>Researcher</th>
<th>Institute</th>
<th>Researchers topics/interests</th>
<th>Facilities Accessed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. Alexei Nazarov</td>
<td>Lashkaryov Institute of Semiconductor Physics NASU, Ukraine. (ASCENT ref: 059)</td>
<td>This project will apply low-temperature plasma annealing (not more 250°C) to new types of semiconductor MOS devices such as junctionless III-V MISFET which are very sensitive to high-temperature processing. Testing of interface and border traps in the interface Al2O3/InGaAs, channel electron mobility, source-drain contact resistance and channel resistivity and leakage current through InGaAs/InP heterojunction will be performed before and after low-temperature plasma annealing to extract an optimal regime of the annealing and demonstration of possibilities of the technology. The project will allow to develop a new approach to control of main electrical parameters of such nanoscaled devices.</td>
<td>Access provided to fabricated devices and advanced electrical characterization facilities at Tyndall</td>
</tr>
<tr>
<td>Peter Schüffelgen</td>
<td>Forschungszentrum Jülich, Germany (ASCENT ref: 050)</td>
<td>Three-dimensional topological insulators (TIs) possess metallic surface states with a spin-locked momentum. In proximity to an s-wave superconductor, Majorana zero modes (MZMs) are predicted to occur at the surface of TIs. Due to their non-abelian exchange statistics, such MZMs are expected to enable fault-tolerant quantum computation. Within my PhD I am fabricating topological insulator – superconductor hybrid junctions of various geometries. A high quality of the interface between superconductor and topological insulator is crucial. Tyndall’s expertise on Focus Ion Beam and Transmission electron microscopy allowed to actually have a look at such interfaces. In this way I could compare different superconductors and find the best material combination.</td>
<td>Access provided to Focussed Ion Beam and TEM facility at Tyndall.</td>
</tr>
<tr>
<td>Prof. Francisco Gamiz</td>
<td>University of Granada, Spain (ASCENT ref: 042)</td>
<td>The project will develop new characterization and simulation tools required to understand the behaviour of state-of-the-art semiconductor devices. Some effects which were considered so far as second-order effects, are now very important and understanding the behaviour of second order effects will help to boost the performance of the new devices, not only in the More Moore domain, but also in the More than Moore domain.</td>
<td>Access provided to a 300mm CMOS wafer with FDSOI and Si nanowire devices from CEA-Leti.</td>
</tr>
<tr>
<td>Ref</td>
<td>User</td>
<td>Institute</td>
<td>Country</td>
</tr>
<tr>
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<tr>
<td>002</td>
<td>G. Angelov</td>
<td>Technical University of Sofia</td>
<td>Bulgaria</td>
</tr>
<tr>
<td>006</td>
<td>G. Fatin</td>
<td>University of Maynooth</td>
<td>Ireland</td>
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<tr>
<td>008</td>
<td>A. Durgaryan</td>
<td>Synopsys</td>
<td>Armenia</td>
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<tr>
<td>022</td>
<td>A. Nejadmalayeri</td>
<td>Phoelex Ltd (SME)</td>
<td>UK</td>
</tr>
<tr>
<td>031</td>
<td>X. Wang</td>
<td>Univ. Glasgow</td>
<td>UK</td>
</tr>
<tr>
<td>035</td>
<td>K. Miyaguchi</td>
<td>IMEC</td>
<td>Belgium</td>
</tr>
<tr>
<td>036</td>
<td>G. Ghibaudo</td>
<td>IMEP-LAHC/INPG</td>
<td>France</td>
</tr>
<tr>
<td>037</td>
<td>F. Gamiz</td>
<td>University of Granada</td>
<td>Spain</td>
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<tr>
<td>043</td>
<td>M. Karner</td>
<td>GlobalTCAD Solutions GmbH</td>
<td>Austria</td>
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<tr>
<td>045</td>
<td>T. Kelly</td>
<td>EOLAS Designs</td>
<td>Ireland</td>
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<td>047</td>
<td>A. Pezzotta</td>
<td>EPFL ICLAB</td>
<td>Switzerland</td>
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<td>057</td>
<td>C. Couso</td>
<td>Univ. Aut. Barcelona</td>
<td>Spain</td>
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<td>058</td>
<td>M. Bucher</td>
<td>Technical University of Crete</td>
<td>Greece</td>
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<td>062</td>
<td>L. Dobrescu</td>
<td>T.U. Bucharest</td>
<td>Romania</td>
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<td>068</td>
<td>B. Sheehan</td>
<td>Tyndall National Institute</td>
<td>Ireland</td>
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<td>082</td>
<td>P. Dimitrakis</td>
<td>Institute of Nanoscience &amp; Nanotechnology</td>
<td>Greece</td>
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<tr>
<td>085</td>
<td>Y. Chauhan</td>
<td>Indian Institute of Technology, Kanpur</td>
<td>India</td>
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</table>
## Sample VA User Profiles

<table>
<thead>
<tr>
<th>Researcher</th>
<th>Institute</th>
<th>Researchers topics/interests</th>
<th>What will you use the CMOS datasets for?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dr X. Wang</td>
<td>University of Glasgow, UK</td>
<td>I am a Research Associate with Device Modelling Group in the School of Engineering at University of Glasgow. Dr Wang’s current research interest involves nanoscale MOSFET devices, TCAD and atomistic modeling and numerical simulations. He is particularly interested in intrinsic parameter fluctuations due to statistical variability and reliability. (ASCENT ref: 031)</td>
<td>I have been working in advanced MOSFET architecture and compact modelling for many years and I am currently developing novel statistical compact models. I am coordinating the EU H2020-funded REMINDER project on behalf of Prof. Asenov at University of Glasgow and access through ASCENT came just at the right time for me.</td>
</tr>
<tr>
<td>Dr Gholamreza Zare</td>
<td>NUI Maynooth, Ireland</td>
<td>My current research interest includes the design of different RFIC blocks for a transceiver targeting the next generation of the wireless communications systems. I am also interested in design of high speed data converters, millimetre wave integrated circuits and phased array circuits. (ASCENT ref: 006)</td>
<td>I was interested to be able to design with these advanced transistors (FDSOI and FinFET) and investigate their circuit characteristic. I am working on RFIC design and want to know their performance in this design field. This was the main reason to request for access. I am also interested in characterisation of these transistors (chips).</td>
</tr>
<tr>
<td>Dr Gerard Ghibaudo</td>
<td>IMEP-LaHC, Grenoble, France</td>
<td>I am the Director of Research at CNRS and Director of IMEP-LAHC Laboratory located at MINATEC-INPG centre. My main research activities are in the field of electronics transport, oxidation of silicon, MOS device physics, fluctuations and low frequency noise and dielectric reliability. I became Fellow IEEE in 2013. (ASCENT ref: 036)</td>
<td>Internal needs for PhD students and comparison to other technologies (FDSOI).</td>
</tr>
<tr>
<td>Prof. Francisco Gamiz</td>
<td>University of Granada, Spain</td>
<td>My group at the University of Granada develops several research lines. A priority is the development of numerical simulators of advanced semiconductor devices. The combination of both experimental and simulation results is key for the understanding of the physical mechanisms under the operation of these advanced devices, and for the implementation of new transport models, and scattering mechanisms. (ASCENT ref: 037)</td>
<td>Calibration and tuning of semiconductor TCAD and home-made simulators.</td>
</tr>
<tr>
<td>Prof. George Angelov</td>
<td>Technical University of Sofia, Bulgaria.</td>
<td>My research interests are in the fields of device physics; bioelectronics; electrical engineering; multi-physics &amp; control systems; electric vehicles and batteries; renewable energy sources systems and energy efficiency. (ASCENT ref: 002)</td>
<td>Matching simulations based on compact models to experiment data.</td>
</tr>
</tbody>
</table>
Step 6 - User Feedback

Recent on-line survey to all members - 68 replies

85% : Yes, programme is relevant to their research

75% : Have not applied for access yet

44% : plan to apply

88% : Rated application process at highest option

100% : Would recommend this programme to colleagues
Step 6 - User Feedback

- I already recommend my research fellow to Ascent programme, because of world class cutting edge facilities for device fabrication and characterization which is not available in our country.

- Short turnaround time

- ASCENT can provide experimental data, which in our group is quite valuable

- The ASCENT partners are well equipped concerning infrastructure and it seems to be easily accessible.

- Programme provides a good opportunity to exchange ideas with experts in the field

- I was working with THALES for many years before creating TE-OX and this access program could be profitable for making very new specific devices with enhanced performances.

- It is very interesting. You have access to very advanced devices and technology very easily. You only have to write a short proposal, explaining which devices you're interested in, what you're planning to do, and submit it. After a short time, you get the data, the devices, or you visit approved.

- Access to state-of-the-art devices and make good experiments leading to interesting publications and they can communicate with experts and exchange data and ideas

- Access in state of the art devices and perform good experiments leading to high impact publications
Please visit our stand (Paul is here @ ESSDERC) to discuss your requirements

Join our community:
www.ascent.network

email: paul.roseingrave@tyndall.ie
Phone: +353-21-2346268

Please join us in this exciting opportunity for nanoelectronics research