Development of Verilog-A models for silicon photonics devices and implementation in a standard EDA environment

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Summary

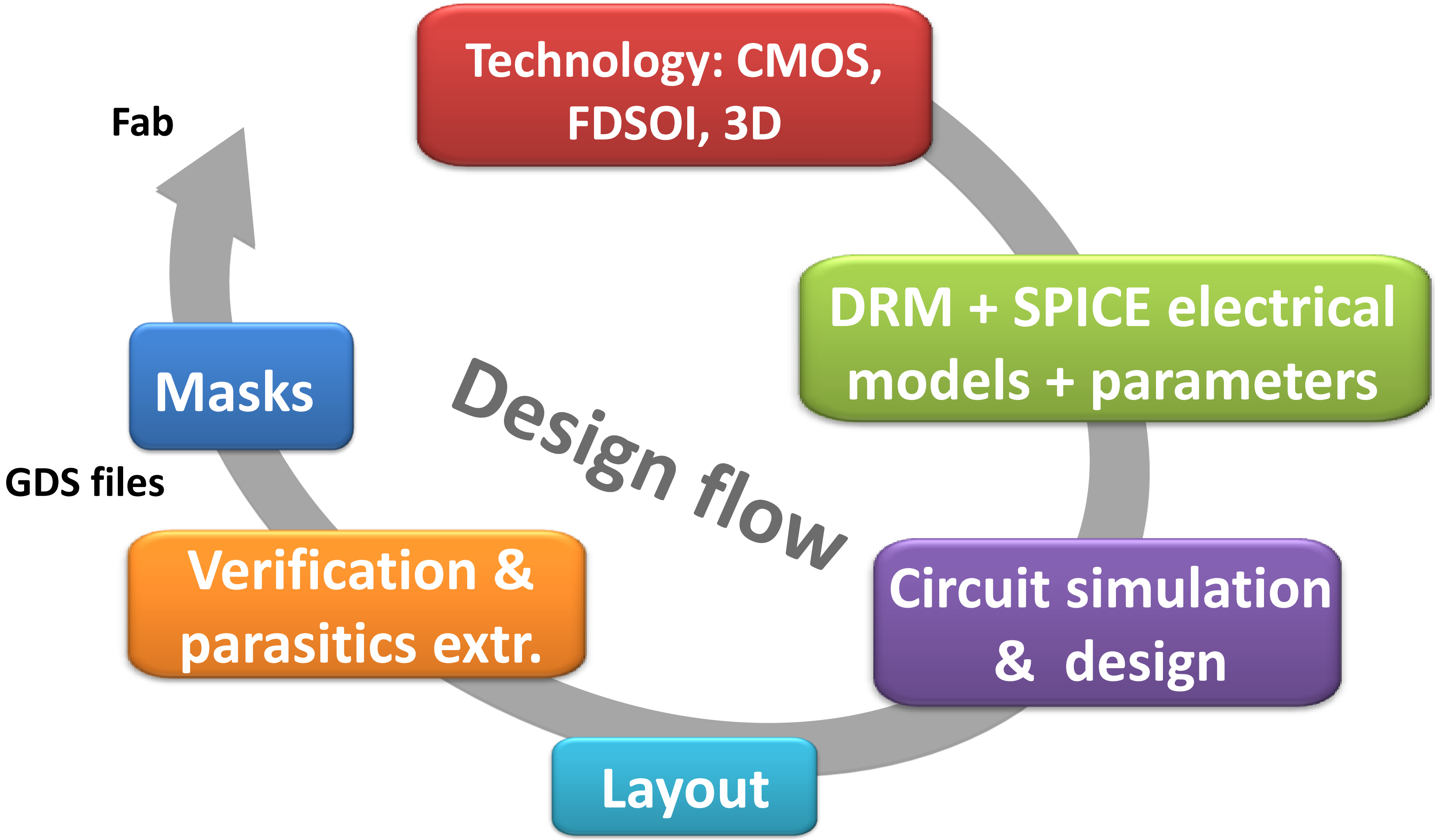
- Why we did this work?
- CMOS PDK and ASICs design flow
- Existing SPICE models for photonics
- Photonics device modeling
- Optical bus
- SPICE toolbox of passive/active silicon photonics devices and symbols
- Photonics PDK and ASPICs design flow
- Arrays in Verilog-A and busses in SPICE netlists
- Conclusion

Why we did this work?

- Growing demand for efficient CAD tools for ASPICs design (Application Specific PhotonICs)
- A wide variety of existing tools for optical design[1]
- A wide variety of existing tools for electrical circuits design (SPICE devices and simulators)[2]
- But few CAD tools for ASPICs design
- One other possibility:
  - Use the Verilog-A language to represent not only active electro-optical devices (e.g. a photodiode), but also purely passive optical devices (e.g. a waveguide)
  - Then integrate these new devices (codes + associated model cards) in a PDK (Process Design Kit) compatible with a standard CMOS CAD environment
  - Design, simulate with SPICE simulators and optimize circuits

[1] Aurrion, Lumerical, Luxtera, Phoenix, UGhent/Imec, etc.
[2] Cadence Design Systems, Mentor Graphics, Synopsys, etc.

CMOS PDK and ASICs design flow



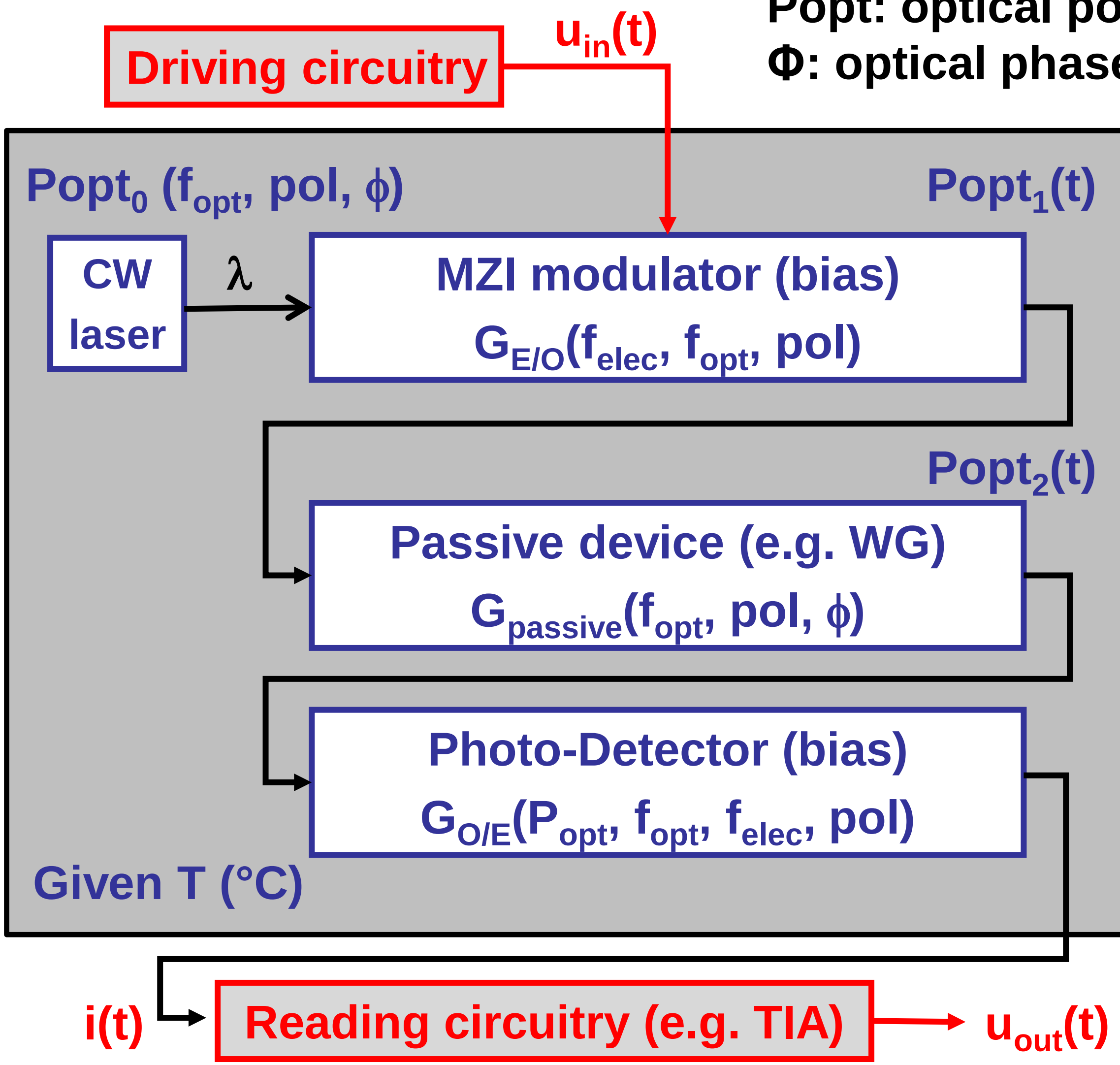
Existing SPICE models for photonics

- Very few models
- Photodiode in Qucs (Quite Universal Circuit Simulator) from Mike Brinson [1]
- Mekis book [2]: Verilog-A models
- Pedagogic publication from the Strasbourg team [3]
- PICMOS EU project, O'Connor et al., 2006 [4]

[1] http://qucs.sourceforge.net/docs/photodiode.pdf
[2] Mekis *et al.*, Computer-Aided Design for CMOS photonics, chap. 12, in "Silicon Photonics for Telecommunications and Biomedicine", CRC Press
[3] F. Pêcheux *et al.*, VHDL-AMS and Verilog-AMS as Alternative Hardware Description Languages for Efficient Modeling of Multidiscipline Systems, IEEE Trans. on Computer-Aided Design, 24, 2, 204-225 (2005)
[4] http://picmos.intec.ugent.be/fileadmin/projectdata/deliverables/D12_draft.pdf

Photonics device modeling

Popt: optical power, pol: light polarization,
Φ: optical phase



$Popt_1 =$
$G_{E/O}(f_{elec}, f_{opt}, pol)$
$\times\, u_{in}(t) \times Popt_0\, (f_{opt}, pol, \phi)$

$Popt_2 =$
$G_{passive}(f_{opt}, pol, \phi)$
$\times\, G_{E/O}(f_{elec}, f_{opt}, pol)$
$\times\, u_{in}(t) \times Popt_0\, (f_{opt}, pol, \phi)$

$i(t) =$
$G_{O/E}(Popt, f_{opt}, f_{elec}, pol)$
$\times\, G_{passive}(f_{opt}, pol, \phi)$
$\times\, G_{E/O}(f_{elec}, f_{opt}, pol)$
$\times\, u_{in}(t) \times Popt_0\, (f_{opt}, pol, \phi)$

$u_{out}(t) = Z \times i(t)$

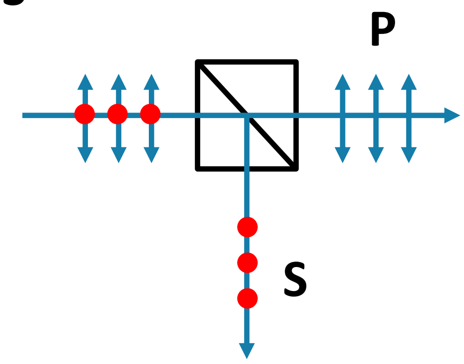
Photonics device modeling (cont'd)

To simulate a device we need:

- The optical/electro-optical model (optical losses, phase shift, electro-optical effect): coded in Verilog-A
- The electrical model (R-L-C-G from electrical contacts, extrinsic elements due to BOX and HR substrate in the Leti SOI photonics process, etc.): described by a macro-circuit inside a SPICE netlist
- The optical and electrical I/O: optical I/O are described by an optical bus of 9 lines

Optical bus

- Up to now, only optical power (in W) and phase (in rad) were considered
- However in some optical devices, light is polarized
- Optical phase is always in the interval [- π, + π]
- Passive optical devices are bidirectional (light from left to right or from right to left)
- We introduce a new concept: an optical signal composed of different lines which are grouped in a optical bus by analogy with an electrical bus such as the IEEE-488 bus
- This bus is composed of 9 lines



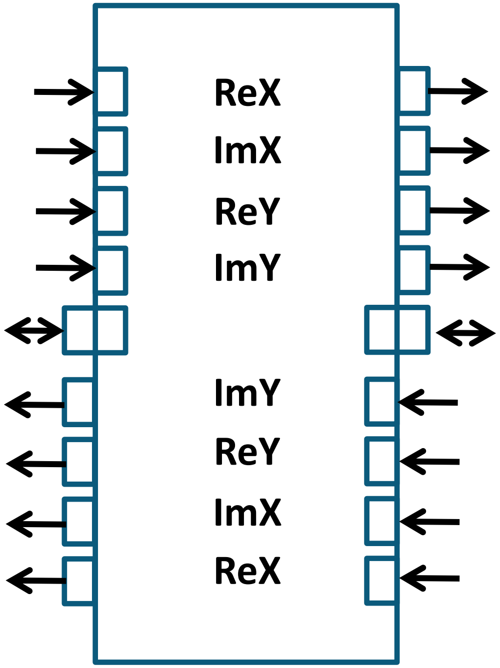
Polarization splitter

Optical bus (cont'd)

The optical signal is represented by 9 variables:
1 variable is the wavelength λ
2 x 2 x 2 = 8 other variables to describe the optical field

2 possible directions | **2 possible polarizations** | **Real part and imaginary part (in $W^{1/2}$)**

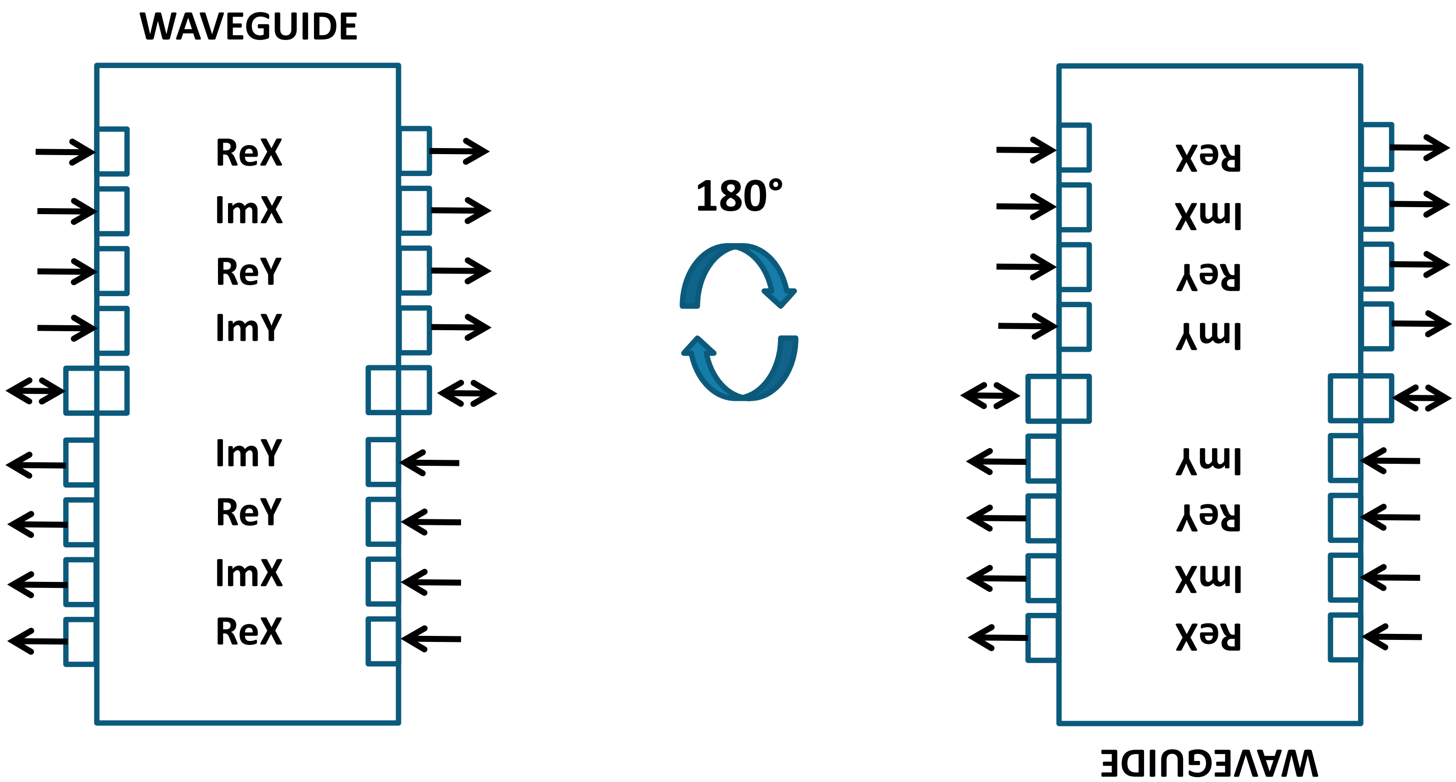
Waveguide (WG)



- $Re(A_x(t))$
- $Im(A_x(t))$
- $Re(A_y(t))$
- $Im(A_y(t))$
- λ
- $Im(A_y(t))$
- $Re(A_y(t))$
- $Im(A_x(t))$
- $Re(A_x(t))$

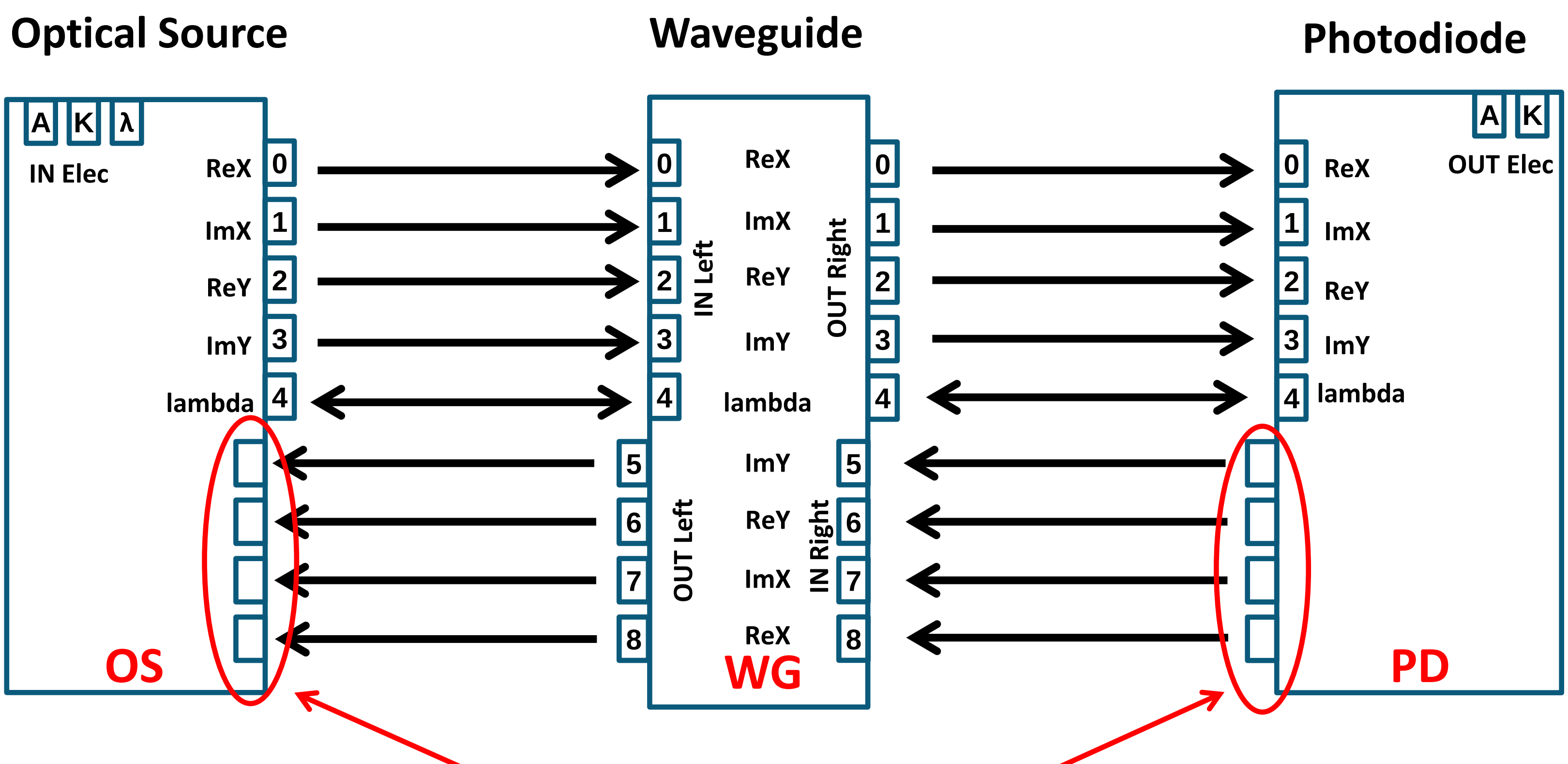
- A_x and A_y are the complex amplitude of the two polarization modes
- Complex amplitude more practical than power & phase (linear equations, no discontinuity, less equations)
- The wavelength is the same for every devices connected together. It's the central wavelength of the simulation, usually chosen as the laser wavelength

WG after 180° rotation



The optical bus is the same everywhere. After 180° rotation of a waveguide, an identical waveguide is obtained

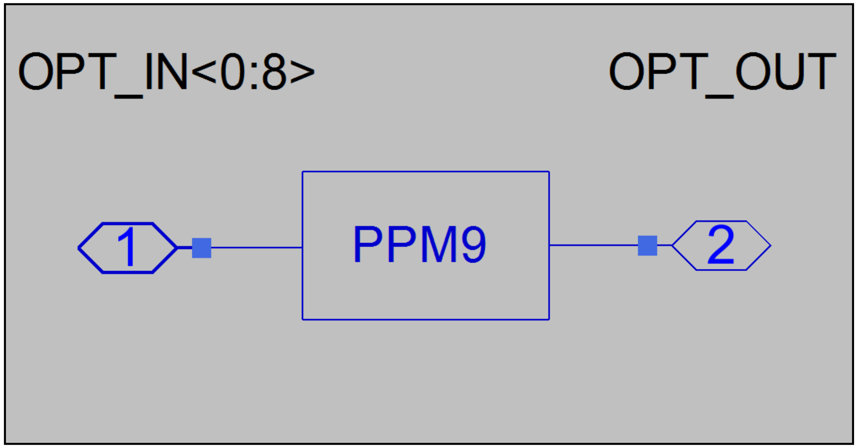
Building an optical link like a Lego® game



Pins existing in the schematic but not used in the component model (to avoid warnings)

Virtual instrument: Power and Phase Meter (PPM)

Symbol with optical bus

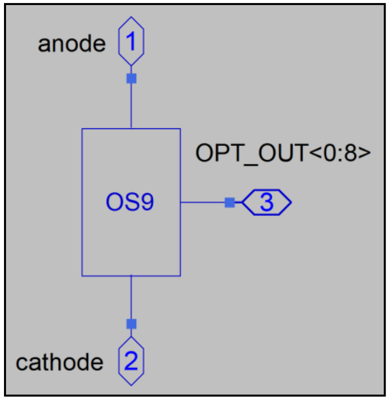


Using complex notation:

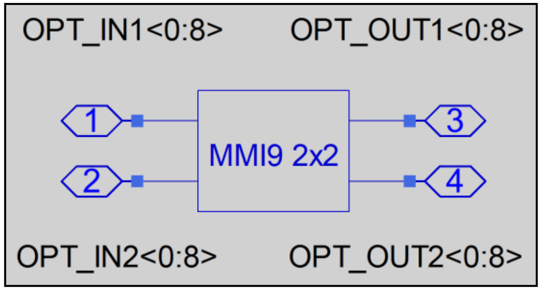
- $A_i = P_i^{0.5} \exp(j\ \varphi_i)$ **with i = X or Y**
- $Power_i = (Re\_A_i)^2 + (Im\_A_i)^2$ **(Watt)**
- $Power = \Sigma_i P_i$
- $Phase_i = arctg\ (Im\_A_i / Re\_A_i)$ **(rad)**

SPICE toolbox of passive/active silicon photonics devices and symbols

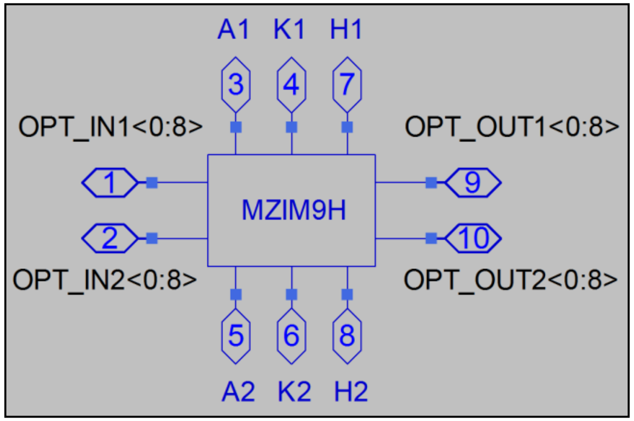
Laser (optical source)



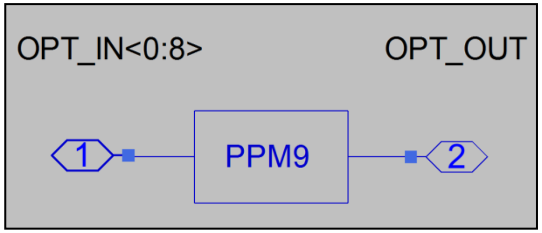
MMI 2x2 coupler



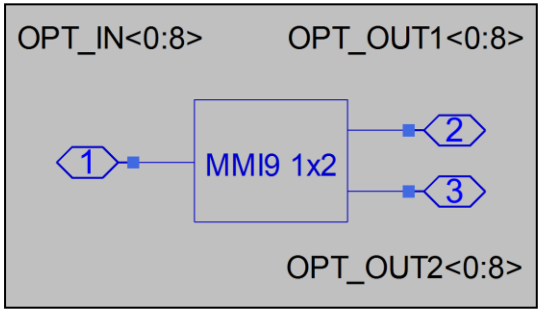
Mach-Zehnder modulator + diode + heater



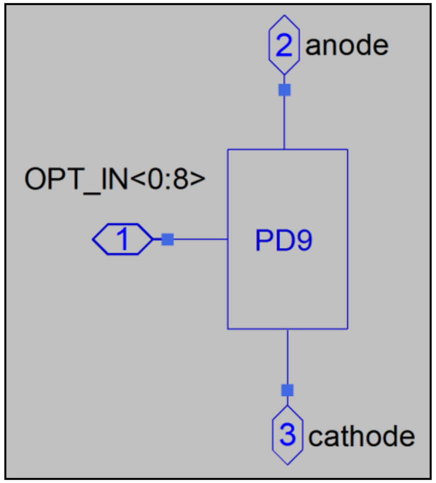
Power & Phase Meter



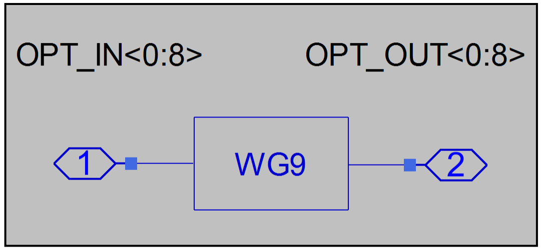
MMI 1x2 & 2x1 couplers



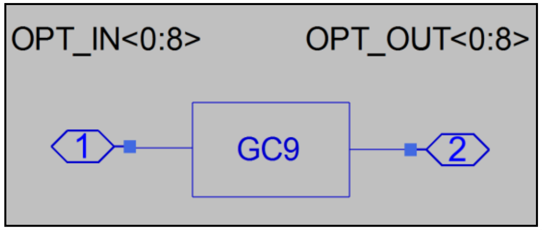
Ge PIN photodiode



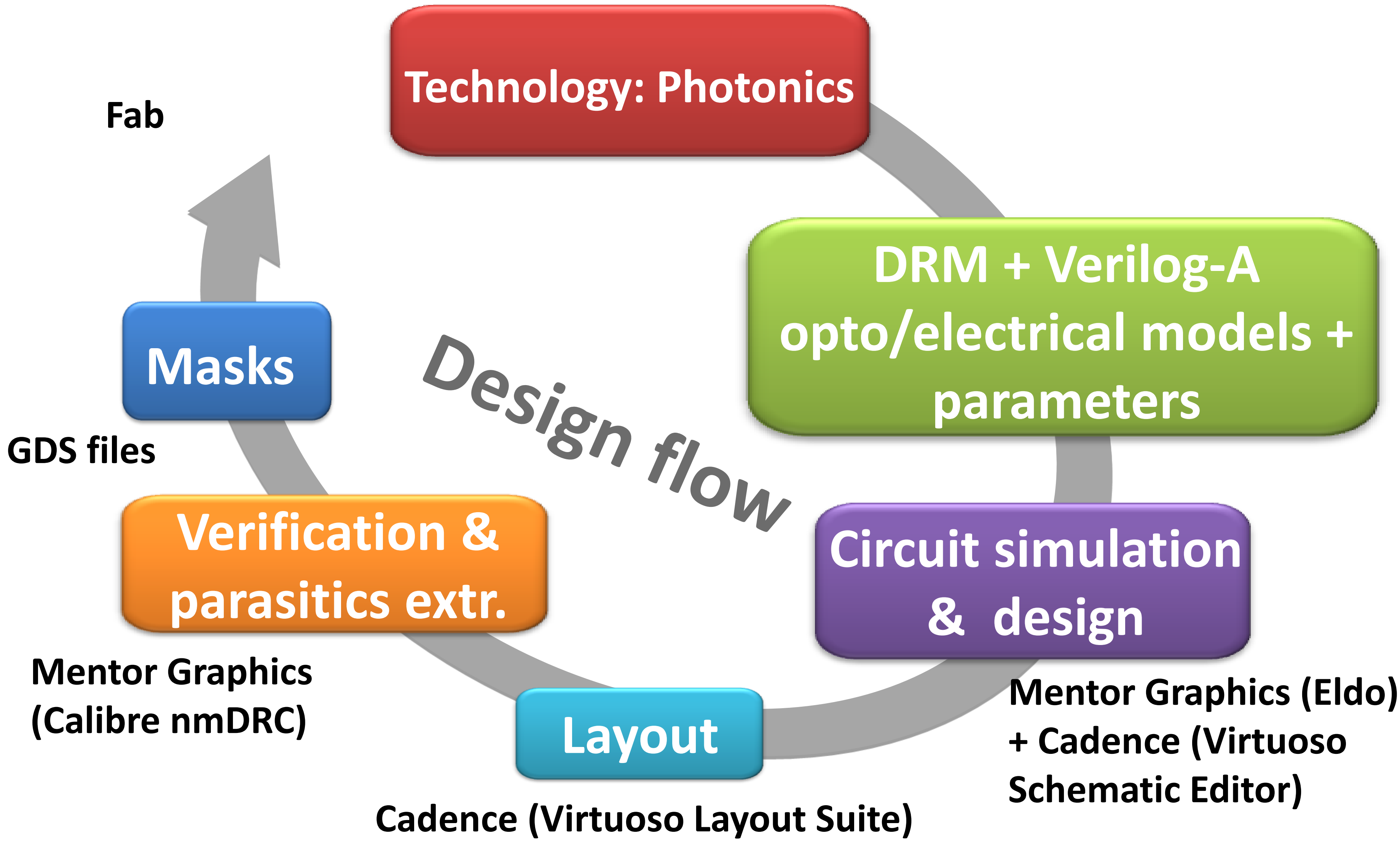
Si waveguide



Grating coupler

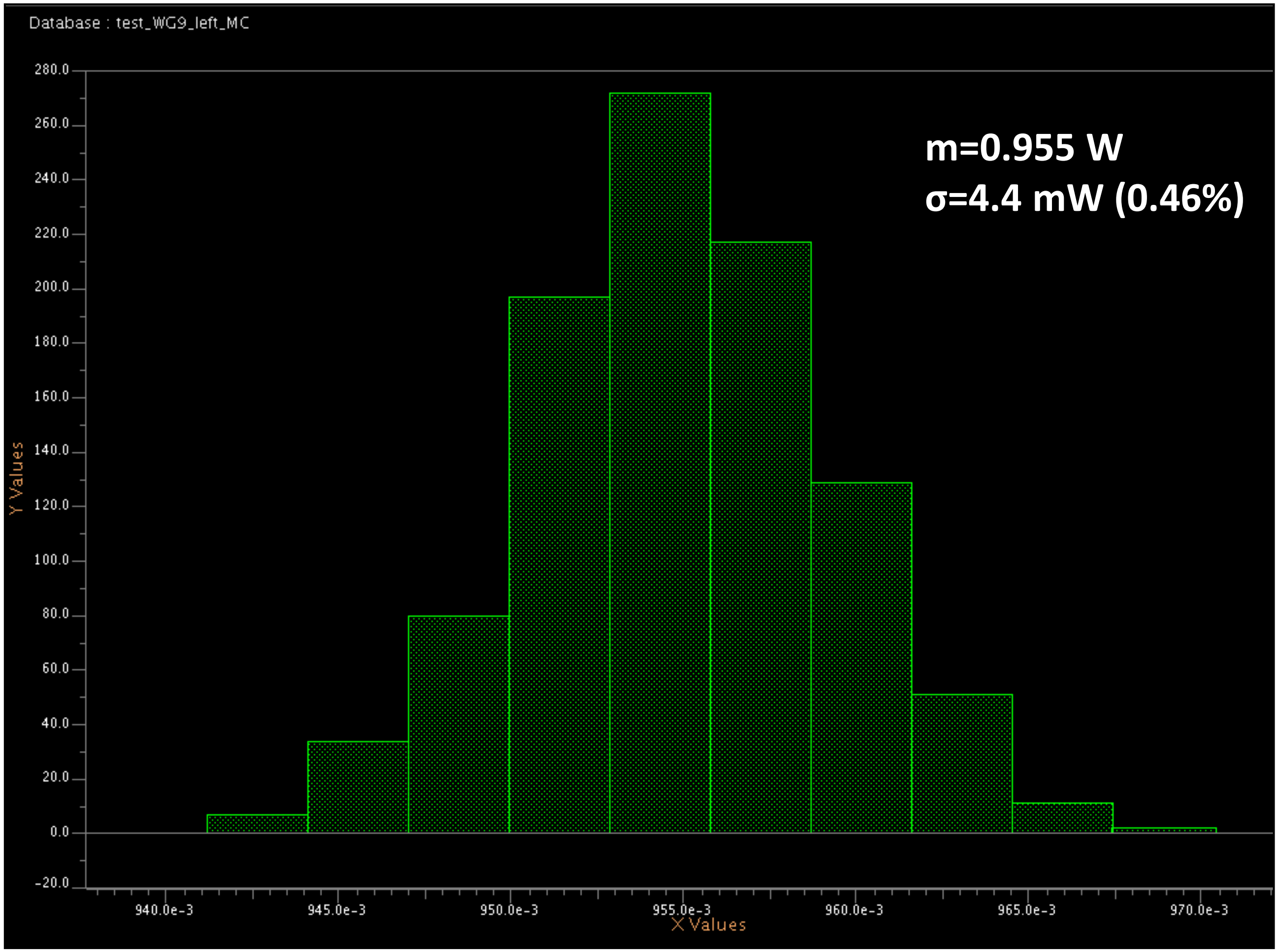


Photonics PDK and ASPICs design flow



Variability study in a purely passive optical device, such as a waveguide, with an electrical simulator

Eldo simulator - Monte Carlo analysis / Number of runs=1000
Optical input power=1.000 W / λ=1.55 µm / T=25 °C / WG_LENGTH=1m DEV/GAUSS=10 %



Frequency

Optical output power (W)

SOI WG, propagation loss: 2 dB/cm

Arrays in Verilog-A

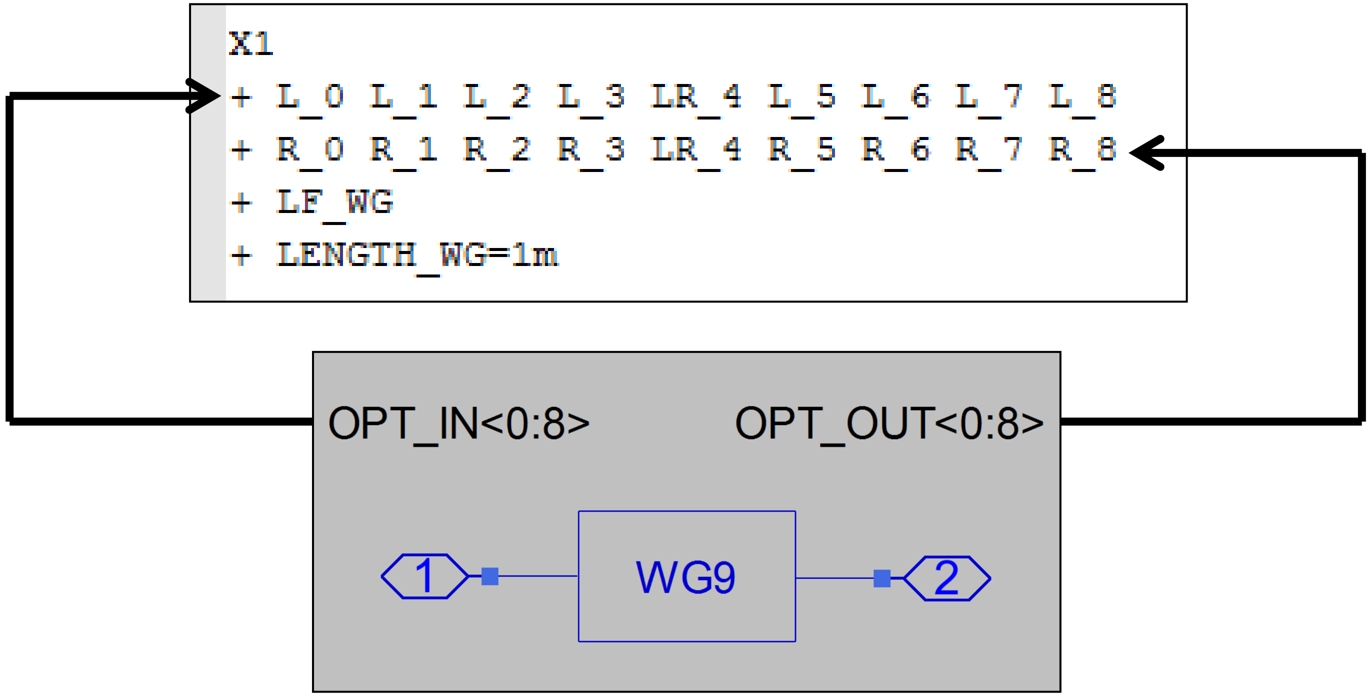
- Are not part of the Accellera Verilog-AMS Language Reference Manual (LRM)
- ADS from Agilent: OK
- Eldo from Mentor Graphics: Not allowed
- Would facilitate writing of Verilog-A modules of photonics devices

```
// Test of two-dimensional array

module T2D (in, out);
    inout in, out;
    electrical in, out;
    real matrix[1:`ROWSIZE][1:`COLSIZE]; // `define ROWSIZE 100, `define COLSIZE 4
    genvar i,j;
    real tmp;
analog begin
    for (i = 1 ; i <= `ROWSIZE ; i = i + 1) begin
        for (j = 1 ; j <= `COLSIZE ; j = j + 1) begin
            matrix[i][j] = i * j;
        end
    end
    tmp = matrix[100][4];
    $strobe("The value of tmp is %e", tmp, " -");
    V(out) <+ tmp * V(in);
end // analog
endmodule // T2D
```

Busses in SPICE netlists

- Not allowed in SPICE netlists
- Must be expanded (spread)
- Bus notation B<i:j> as in symbols would facilitate building/reading of netlists for photonIC's circuits



Conclusion

- **A new approach for photonics devices modeling**
- **New optical bus with 9 lines: light is polarized, phase is well calculated [-π, +π], optical devices are bidirectional**
- **Verilog-A models developed for silicon WG, grating coupler, MMI 2x2 coupler, splitter, combiner, PD (model derived from JUNCAP diode), MZIM, optical terminaison, etc…**
- **A toolbox for Silicon on Insulator (SOI) photonics**
- **Need for components standardization**
- **Forthcoming publication at MIEL 2014, Belgrade (Serbia)**

Acknowledgment

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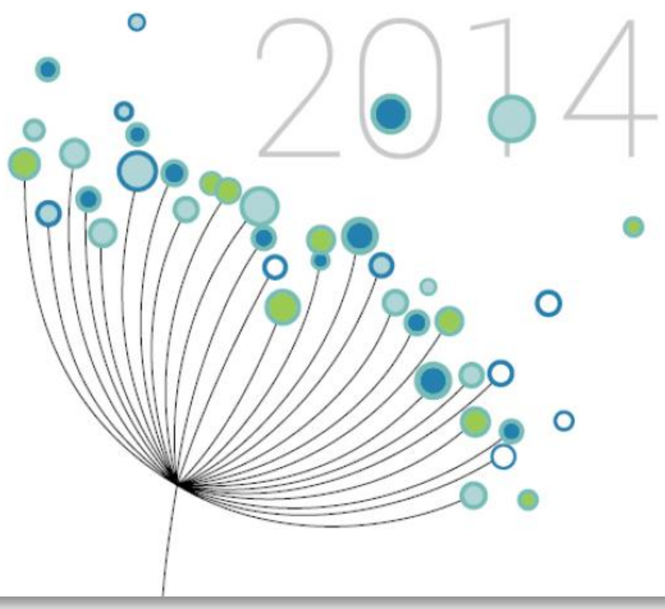

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