EPFL-JL 1.0
Model

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Outline

- Junctionless FETs
- The EPFL-JL model
- Implementation of the model
Let’s follow the Moore’s Law

- Uniformly doped.
- The fabrication process: easier and cheaper.
- fully compatible with CMOS technology and there is not a big barrier.

Schematic view of the n-type junctionless DGMOSFET.
The EPFL-JL model

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Charge-based modeling

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“Ultrashort channel” (<10nm)
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Explicit drain current

Design space

Trans-capacitance modeling

Link to nanowire

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- Charge-based modeling
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- Trans-capacitance modeling
- Link to nanowire
- SCE modeling

MOSAK Workshop, March 27, 2014
The EPFL-JL model

Schematic view of the n-type junctionless DGMOSFET.
Charge based relationships

Depletion

\[ V_G - V_{ch} - \Delta \varphi - U_T \ln \left( \frac{N_D}{n_i} \right)^{dep} \approx - \frac{Q_{sc}^2}{8 q N_D \varepsilon_{si}} - \frac{Q_{sc}}{2 C_{OX}} + U_T \ln \left[ 1 - \left( \frac{Q_{sc}}{q N_D T_{sc}} \right)^2 \right] \]

Accumulation

\[ V_G - V_{ch} - \Delta \varphi - U_T \ln \left( \frac{N_D}{n_i} \right)^{acc} \approx - \frac{Q_{sc}}{2 C_{OX}} + U_T \ln \left[ 1 + \frac{Q_{sc}^2}{8 q N_D \varepsilon_{si} U_T} \right] \]

TED Vol. 58 p. 8, 2011
Explicit drain current

Recently, an approximate and explicit solution has been proposed which bridges the gap between model and implementation.

Design space and off-current

Simulations\(^1\) and experimental results\(^2\) support that below some value of VG (if n type channel), an inversion hole layer starts to build up at the Si/SiO\(_2\) interfaces: The center of the channel becomes electrically ‘isolated’.

\(w/L = 1, \mu = 1417 \text{cm}^2/\text{Vs} \)

1) TED Vol. 60 Issue. 7 p. 2120, 2013
2) TED Vol. 60 Issue. 6 p. 2080, 2013
Trans-capacitance modeling

An analytical and explicit solution has been developed to model the trans-capacitance matrix.

\[ C_{GG} = C_{DG} = C_{SG} \]

\[ N_D = 1 \times 10^{19} \text{cm}^{-3} \]
\[ V_{DS} = 0 \text{V} \]
\[ t_{si} = 20 \text{nm} \]
\[ t_{ox} = 1.5 \text{nm} \]
\[ W = 1 \mu \text{m} \]
\[ L_G = 1 \mu \text{m} \]

\[ 1 \times 10^{-14} \]
\[ 2 \times 10^{-14} \]
\[ 3 \times 10^{-14} \]
\[ 4 \times 10^{-14} \]
\[ 5 \times 10^{-14} \]

\[ 1 \]
\[ 2 \]
\[ 3 \]
\[ 4 \]
\[ 5 \]

TED Vol. 60 Issue. 12 p. 4034, 2013

MOSAK Workshop, March 27, 2014
SCE modeling

An analytical and explicit solution has been developed to model the capacitance matrix.

SSE Vol. 82, p. 103 (2013)
Nanowire modeling

Defining equivalent parameters, it is possible to simulate charges and current in JL nanowire using the relationships developed for the DG counterpart.

<table>
<thead>
<tr>
<th>Physical parameters</th>
<th>Nanowire</th>
<th>Equivalent DG FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radius and thickness</td>
<td>R (radius)</td>
<td>$T_{sc} = 2\times R$</td>
</tr>
<tr>
<td>Oxide thickness</td>
<td>$t_{ox}$</td>
<td>$T_{sc}/2 \times \ln(1 + 2t_{ox}/ T_{sc})$</td>
</tr>
<tr>
<td>Width</td>
<td>--</td>
<td>$W = \pi \times R$</td>
</tr>
<tr>
<td>Doping concentration</td>
<td>$N_D$</td>
<td>$N_D/2$</td>
</tr>
<tr>
<td>Intrinsics carrier concentration</td>
<td>$n_i$</td>
<td>$n_i/2$</td>
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</tbody>
</table>

TED Vol. 60 Issue. 12 p. 4277, 2013
Nanowire modeling

Defining equivalent parameters, it is possible to simulate charges and current in JL nanowire using the relationships developed for the DG counterpart.

TED Vol. 60 Issue. 12 p. 4277, 2013
The EPFL-JL 1.0 has been implemented as sub-circuits compatible for Hspice simulations.

The proposed model can be imported as a library to Cadence virtuoso or Advanced Design System (ADS).
DC implementation

Flat band conditions at source and drain obtained by:

\[ V_{GFBD} = V_{GFBS} + V_{DS} = \Delta \varphi + U_T \ln \left( \frac{N_D}{n_i} \right) \]

The model structure described above is schematically depicted in Fig.

The model structure described above is schematically depicted in Fig.

\[ N_D = 10^{19} \text{cm}^{-3}, \quad T_{sc} = 10 \text{nm}, \quad L_G = 100 \text{nm}, \quad W = 1 \mu m, \quad t_{ox} = 1.5 \text{nm}, \quad V_{DS} = 1 \text{V} \]

<table>
<thead>
<tr>
<th></th>
<th>( V_G &lt; V_{GFBS} ) (Depletion)</th>
<th>( V_{GFBS} &lt; V_G &lt; V_{GFBD} ) (Hybrid)</th>
<th>( V_G &gt; V_{GFBD} ) (Accumulation)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW_1</td>
<td>Close</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>SW_2</td>
<td>Open</td>
<td>Close</td>
<td>close</td>
</tr>
<tr>
<td>SW_3</td>
<td>Open</td>
<td>Open</td>
<td>Close</td>
</tr>
<tr>
<td>SW_4</td>
<td>Close</td>
<td>Close</td>
<td>Open</td>
</tr>
<tr>
<td>SW_5</td>
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<td>Close</td>
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<tr>
<td>SW_6</td>
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</tr>
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<td>SW_7</td>
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</tr>
<tr>
<td>SW_8</td>
<td>Open</td>
<td>Open</td>
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</tr>
</tbody>
</table>
Trans-capacitance matrix

JLDGFET
- $N_D = 10^{19} \text{ cm}^{-3}$
- $T_{sc} = 10 \text{ nm}$
- $L_g = 100 \text{ nm}$
- $t_{ox} = 1.5 \text{ nm}$
- $W = 15.7 \text{ nm}$

NW FET
- $N_D = 2 \times 10^{19} \text{ cm}^{-3}$
- $R = 5 \text{ nm}$
- $L_g = 100 \text{ nm}$
- $t_{ox} = 1.75 \text{ nm}$

**Depletion**
- $V_i = 0 \text{ V} < V_{FBS}$

**Hybrid**
- $V_{FBS} < V_i < 1 \text{ V} < V_{FBD}$

**$V_{FBS}$ = 0.54 V and $V_{FBD}$ = 1.54 V**

**$V_{DS}$ = 1 V**
Trans-capacitance matrix

\[ V_{ds} = 0.7\, \text{V} \]

**JLDGFET**
- \( N_D = 10^{19} \, \text{cm}^{-3} \)
- \( T_{sc} = 10\, \text{nm} \)
- \( L_g = 100\, \text{nm} \)
- \( t_{ox} = 1.5\, \text{nm} \)
- \( W = 15.7\, \text{nm} \)

**NW FET**
- \( N_D = 2 \times 10^{19} \, \text{cm}^{-3} \)
- \( R = 5\, \text{nm} \)
- \( L_g = 100\, \text{nm} \)
- \( t_{ox} = 1.75\, \text{nm} \)

Depletion
- \( V_i = 0\, \text{V} < V_{FBS} \)
- \( V_{FBS} = 0.54\, \text{V} \) and \( V_{FBD} = 1.24\, \text{V} \)
- \( V_{DS} = 0.7\, \text{V} \)

Accumulation
- \( V_i = 1.3\, \text{V} > V_{FBD} \)
Small Signal

\[ C_{ij} = \frac{\partial Q_i}{\partial V_j} \]

\[
\begin{pmatrix}
i_g \\
i_d
\end{pmatrix} = \begin{pmatrix} C_{GG} & C_{DG} \\ C_{GD} & C_{DD} \end{pmatrix} \times \begin{pmatrix} v_{gs} \\ v_{ds} \end{pmatrix}
\]
Small Signal

\[
\begin{aligned}
C_{ij} &= \frac{\partial Q_i}{\partial V_j} \\
\begin{pmatrix}
  i_g \\
  i_d
\end{pmatrix} &=
\begin{pmatrix}
  C_{GG} & C_{DG} \\
  C_{GD} & C_{DD}
\end{pmatrix}
\times
\begin{pmatrix}
  v_{gs} \\
  v_{ds}
\end{pmatrix}
\end{aligned}
\]
JLDG & Nanowire FET amplifier

**JLDGFET**
- \( N_D = 10^{19} \text{cm}^{-3} \)
- \( T_{sc} = 10 \text{nm} \)
- \( L_g = 100 \text{nm} \)
- \( t_{ox} = 1.5 \text{nm} \)
- \( W = 15.7 \text{ nm} \)

**NW FET**
- \( N_D = 2 \times 10^{19} \text{cm}^{-3} \)
- \( R = 5 \text{nm} \)
- \( L_g = 100 \text{nm} \)
- \( t_{ox} = 1.75 \text{nm} \)

Common source amplifier based on n-JLFET

**Frequency = 3MHz, \( R_L = 40k \mid r_o \right \), \( V_{ds} = 1V, \)
- \( I_{bias} = 360 \mu A, \) \( V_{Gbias} = 0.1V, \) \( A_V = -180 \text{ V/V} \)**

**Frequency = 500MHZ, \( R_L = 50k \mid V_{ds} = 10mv, \)
- \( V_{Gbias} = 1.5V, \) \( \text{Phase difference is} \ 90^\circ \)**

**Frequency = 500MHZ, \( R_L = 10k \mid V_{ds} = 1V, \)
- \( V_{Gbias} = 1.5V, \) \( \text{Phase difference is} \ 180^\circ \)**
JL DG FET Inverter

**JLDGFET**
- $N_D = 10^{19} \text{cm}^{-3}$
- $T_{sc} = 10 \text{nm}$
- $L_g = 100 \text{nm}$
- $t_{ox} = 1.5 \text{nm}$
- $W = 15.7 \text{nm}$

**NW FET**
- $N_D = 2 \times 10^{19} \text{cm}^{-3}$
- $R = 5 \text{nm}$
- $L_g = 100 \text{nm}$
- $t_{ox} = 1.75 \text{nm}$

$V_{DD} = 0.3 \text{V}$ $V_{SS} = -0.3 \text{V}$
Thank you!
JLDG & Nanowire FET Amplifier

**JLDGFET**
- \( N_D = 10^{19} \text{cm}^{-3} \)
- \( T_{sc} = 10 \text{nm} \)
- \( L_g = 100 \text{nm} \)
- \( t_{ox} = 1.5 \text{nm} \)
- \( W = 15.7 \text{ nm} \)

**NW FET**
- \( N_D = 2 \times 10^{19} \text{cm}^{-3} \)
- \( R = 5 \text{ nm} \)
- \( L_g = 100 \text{nm} \)
- \( t_{ox} = 1.75 \text{ nm} \)

Common source amplifier based on n- JL Double Gate FET

- \( f = 3 \text{MHZ}, R_L = 40k \), \( r_o V_{ds} = 1V, I_{bias} = 360 \text{uA}, V_{Gbias} = 0.1V, A_v = -180 \text{ V/V} \)

Amplifier for low frequency, phase difference is 180. As illustrated on the right side, for high frequency we do not have gain and depends on \( V_{ds} \) we can see the coupling effect. For low \( V_{ds} \) and high frequency, we can see only \( C_{GD} \) and \( C_{DG} \).