Improving Time-Dependent Gate Breakdown of GaN HEMTs with p-type Gate

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Outline

• Introduction to Time-Dependent Gate Breakdown of p-gate GaN HEMTs
• Devices under test and Process gate-stack splits
• Results and Discussion
• Conclusions
Time-Dependent Gate Breakdown (TDGB)

- When a positive bias is applied on the gate, the Schottky diode (D1) is reverse-biased sustaining a high voltage drop, whereas the PiN diode (D2) is slightly forward-biased [1].
- The Schottky junction is not always the cause of the gate failure under forward gate stress;
- Failure’s spot can occur in different regions and caused by different mechanisms depending on the temperature [2], gate-stack configuration, etc.
- **In this work, the cause leading to TDGB at room/low temperatures is investigated.**

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DUTs: Reference vs Gate Metal Retraction (Group 1)

- GaN-based power HEMT with p-type gate, controlled by a Schottky junction, grown on 200mm Si-wafers.
- Symmetric structure for gate reliability investigation
- Gate stack suitable for voltages class from 100 to 650 V ($V_{DS}$)

![Diagram of GaN-based power HEMT with p-type gate, controlled by a Schottky junction, grown on 200mm Si-wafers.](image)
DUTs: GMR with different AlGaN barrier variants (Group 2)

- GaN-based power HEMT with p-type gate, controlled by a Schottky junction, grown on 200mm Si-wafers.
- Symmetric structure for gate reliability investigation
- Gate stack suitable for voltages class from 100 to 650 V
- Gate Metal Retraction

<table>
<thead>
<tr>
<th>Process</th>
<th>Mg (cm(^{-3}))</th>
<th>pGaN (nm)</th>
<th>Al (%)</th>
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<tbody>
<tr>
<td>1A</td>
<td>(2.7 \cdot 10^{19})</td>
<td>80</td>
<td>25</td>
<td>12.5</td>
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<tr>
<td>2A</td>
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<tr>
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- Process 1A (reference)
- From 1 to 3 means thicker AlGaN
- From A to D implies lower Al%.
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• Reference devices show a relatively low maximum gate voltage @ 10 years
• TTF scales only with gate width suggesting time-dependent breakdown along the gate edges (no area dependency)
Gate Time To Failure: Reference device (2)

- Sidewall gate leakage, causing premature gate failure, has been substantiated by TCAD simulation and EBIC measurements [3]

Simulated electron and hole current densities at different forward gate biases of the p-GaN gate

EBIC signal measured at $V_{GS}=2.5$V
Critical regions at the p-GaN sidewalls are marked by arrows

Proposed Solution: Gate Metal Retraction

GMR consists in removing 130nm of TiN metal from gate edge to suppress the sidewall leakage.

- Improved gate lifetime
- TTF shows area dependency (scales with both gate width and length)
Role of the Aluminum content on gate TTF (from A to D)

- The lower Al%, the longer TTF
- The rate of defect creation (structural) in the AlGaN barrier layer decreases when the crystalline lattice of the AlGaN is subjected to weaker mechanical stress, i.e. when lower Al% is adopted

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Role of the AlGaN thickness on TTF (from 1 to 3)

- The thicker AlGaN, the longer TTF (1A and 2A)
- However, a further thickness increase (from 2A/2B to 3C/3D) does not produce a further TTF improvement, despite the lower Al%
Role of the AlGaN thickness on TTF (from 1 to 3)

- The role of AlGaN thickness can be explained by the combination of two mechanisms[4]:
  - a too thin AlGaN requires the creation of only a few defects to form a percolation path (failure), hence a thicker AlGaN improves TTF (1A and 2A);
  - a too thick AlGaN implies a lower $V_{TH}$, which causes a higher gate leakage during the stress due to larger voltage drop on the Schottky junction at given $V_G$.

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• The failure at the gate edges has been suppressed by Gate Metal Retraction, improving gate lifetime;
• The AlGaN barrier has been identified as the layer mainly responsible for TTF at room temperature [4].
• Lower Al% leads to longer TTF because of two benefits:
  o The AlGaN barrier is structurally more robust due to lower mechanical stress;
  o The gate leakage is lower due to higher $V_{TH}$.
• An optimum AlGaN barrier thickness at given Al% exists with respect to TTF:
  o Too thin a layer can speed up the build-up of a percolation path, reducing the TTF;
  o Too thick a barrier increases the gate leakage because of lower $V_{TH}$, reducing TTF

Thanks for your attention