

Parameter extraction strategy for the UCB BSIM4 model

Arbeitskreis MOS Modelle

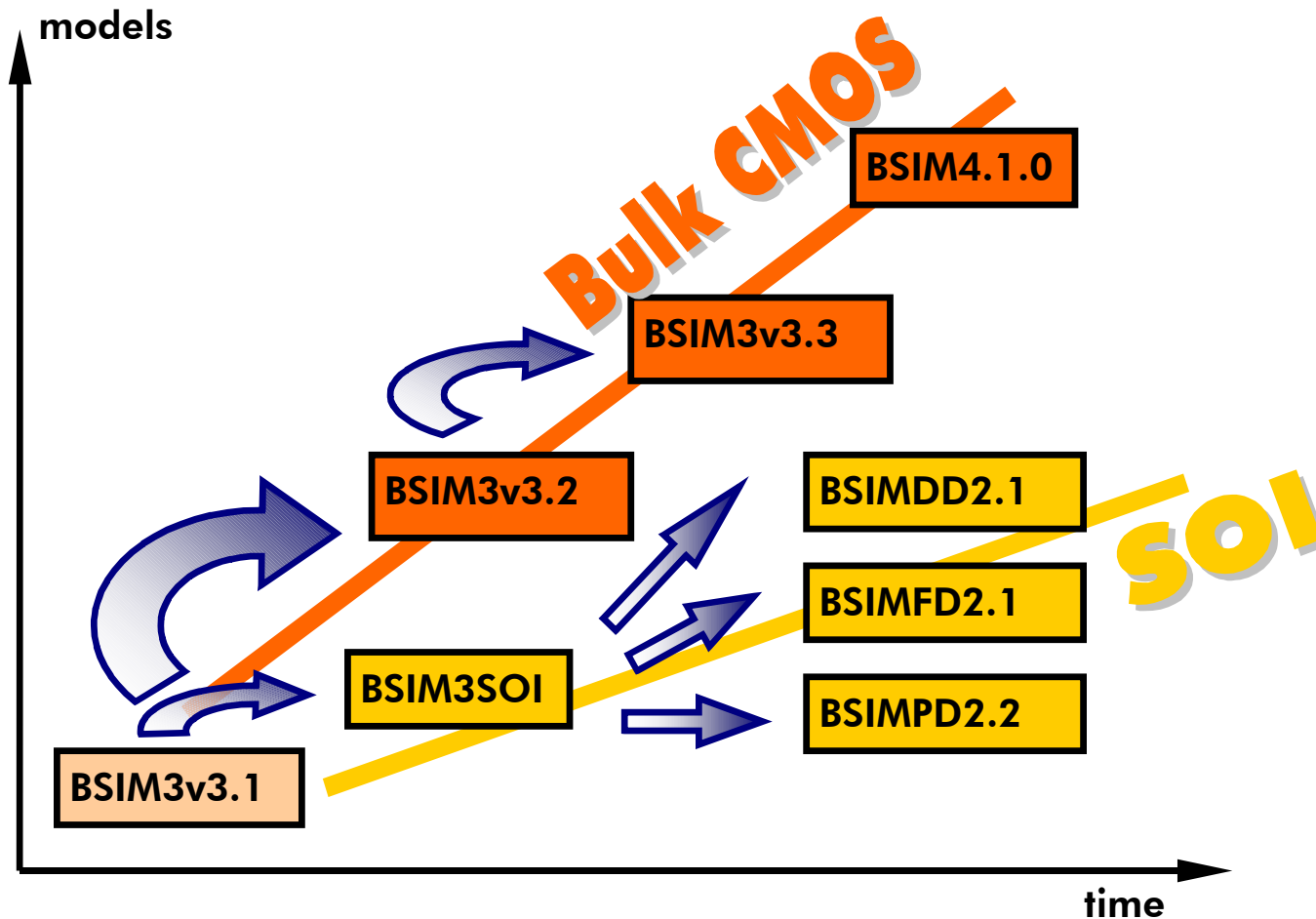
Infineon, München, 5.3.2001

Dr. Thomas Gneiting

Thomas.Gneiting@admos.de

- Introduction
 - Summary of physical effects described in BSIM4
 - Modeling Strategy:
 - ◆ Test devices
 - ◆ Measurements
 - ◆ Condensed data representation concepts
 - ◆ Model configuration guide
 - ◆ Advanced parameter extraction methods
 - Summary and outlook
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Roadmap of BSIM Simulation Models



Physical effects included in BSIM4 (1)

The BSIM4 model covers the following physical effects of deep submicron MOS devices approaching the nanometer region:

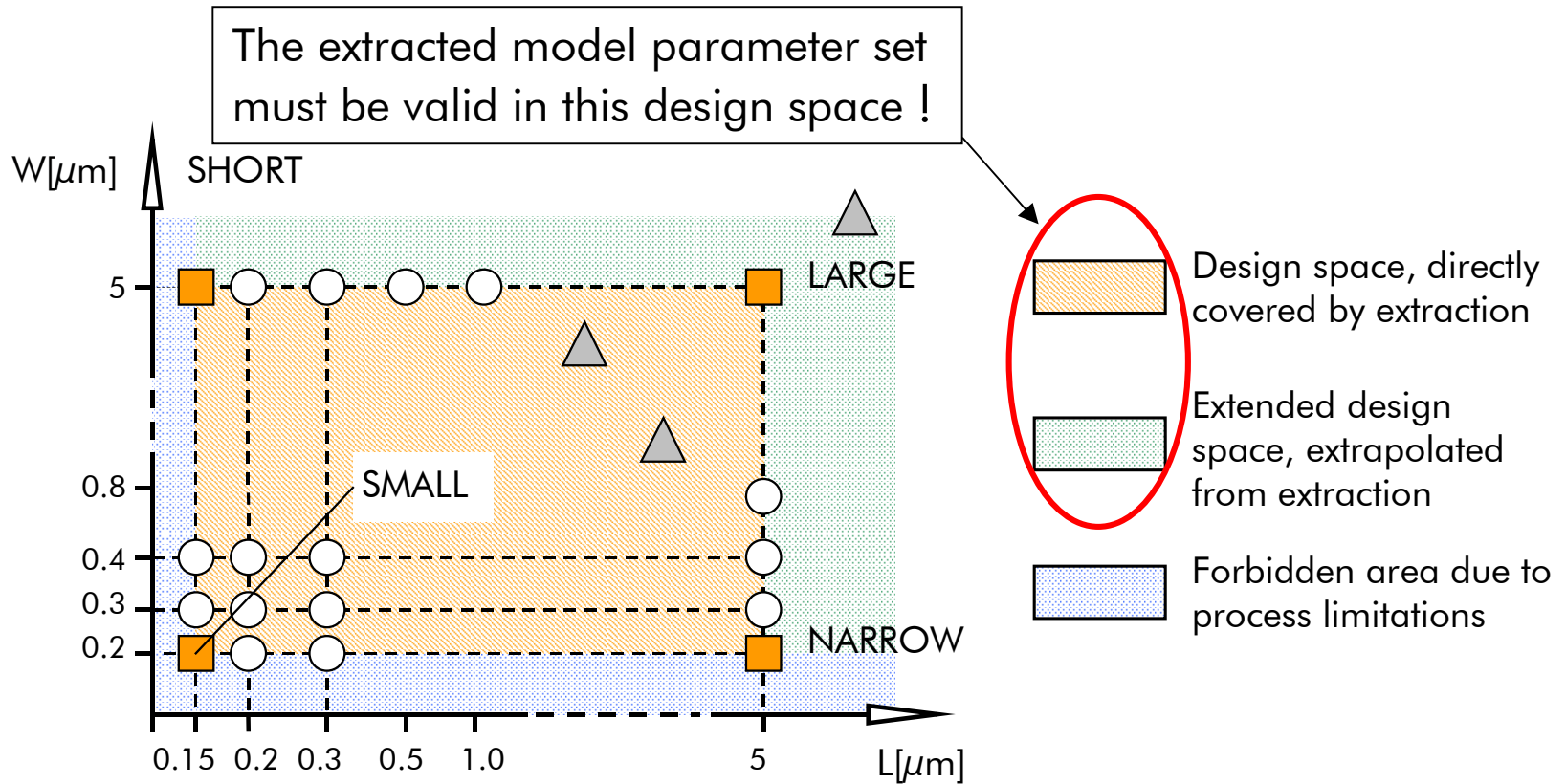
- Basic physical effects:
 - ◆ Short and narrow channel effects on threshold voltage
 - ◆ Non-uniform doping effects
 - ◆ Mobility reduction due to vertical field
 - ◆ Bulk charge effect
 - ◆ Carrier velocity saturation
 - ◆ Drain induced barrier lowering (DIBL)
 - ◆ Channel length modulation (CLM)
 - ◆ Substrate current induced body effect (SCBE)
 - ◆ Parasitic resistance effects
 - ◆ Quantum mechanic charge thickness model

Physical effects included in BSIM4 (2)

- Enhanced drain current model
 - ◆ V_{th} model for pocket/retrograde technologies
 - ◆ New predictive mobility model
 - ◆ Gate induced drain leakage (GIDL)
 - ◆ Internal/external bias-dependent drain source resistance
 - RF and high-speed model
 - ◆ Intrinsic input resistance (R_{gate}) model
 - ◆ Non-Quasi-Static (NQS) model
 - ◆ Holistic and noise-partition thermal noise model
 - ◆ Substrate resistance network
 - ◆ Calculation of layout-dependent parasitic elements
 - Asymmetrical source/drain junction diode model
 - ◆ I-V and breakdown model
 - Gate dielectric tunneling current model
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Test devices (DC)



➔ The proper design of appropriate test structures is the ultimate pre-requisite for accurate model generation !

Measurement effort

Performing the required measurements is an essential part of the modeling flow !!

Include different temperatures

27 C	-20 C	80 C	155 C
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

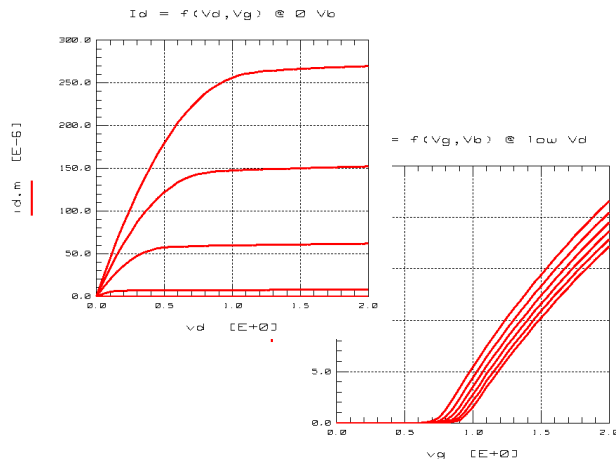
DUT
Large
Narrow
Short
Small
L Scale 1
L Scale 2
L Scale 3
L Scale 4
W Scale 1
W Scale 2
LW Scale 1
LW Scale 2
LW Scale 3
LW Scale 4

DUT	27 C	-20 C	80 C	155 C	L [um]	W [um]	AD [um^2]	AS [um^2]	PD [um]	PS [um]	NF	Comment
Large	0	0	0	0	5	5	2	2	6	6	2	
Narrow	0	0	0	0	5	0.18	0.18	0.18	1.36	1.36	1	
Short	0	0	0	0	0.15	5	5	5	11	11	1	
Small	0	0	0	0	0.15	0.18	0.18	0.18	1.36	1.36	1	
L Scale 1	0	-	-	-	0.18	5	5	5	11	11	1	
L Scale 2	0	-	-	-	0.25	5	5	5	11	11	1	
L Scale 3	0	-	-	-	0.4	5	5	5	11	11	1	
L Scale 4	0	-	-	-	0.8	5	5	5	11	11	1	
W Scale 1	0	-	-	-	5	0.25	0.25	0.25	1.5	1.5	1	
W Scale 2	0	-	-	-	5	0.4	0.4	0.4	1.8	1.8	1	
LW Scale 1	0	-	-	-	0.18	0.25	0.25	0.25	1.5	1.5	1	
LW Scale 2	0	-	-	-	0.18	0.18	0.18	0.18	1.36	1.36	1	
LW Scale 3	0	-	-	-	0.25	0.25	0.25	0.25	1.5	1.5	1	
LW Scale 4	0	-	-	-	0.25	0.18	0.18	0.18	1.36	1.36	1	

Up to 30 test devices for DC and capacitance measurements

Conventional data representation

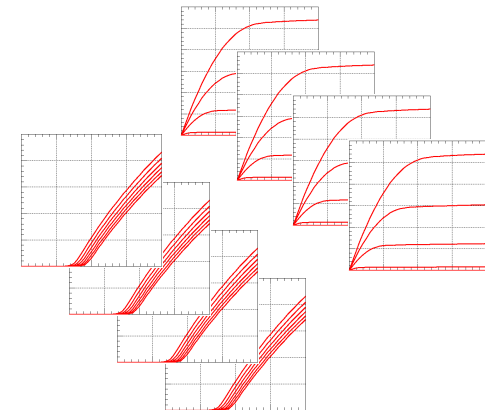
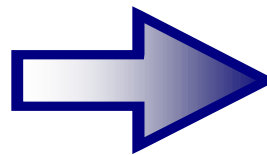
The conventional method is based on **single device** modeling.



I-V-curves are used to:

- extract parameters
- compare measurements versus simulations

This method was mapped to scalable models like BSIM3, MM9 ...

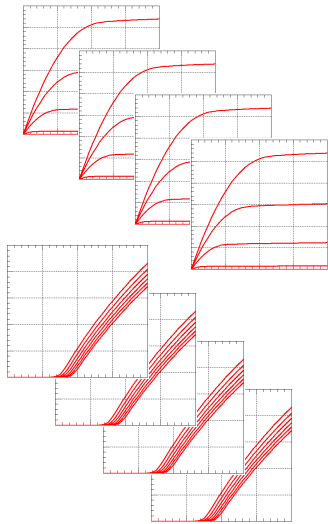


... and resulted in a huge amount of I-V curves to:

- optimize scalable effects on different devices
- verify simulation over devices with different dimensions

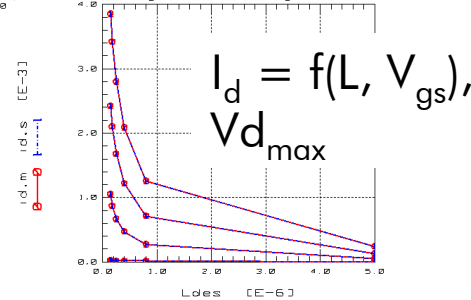
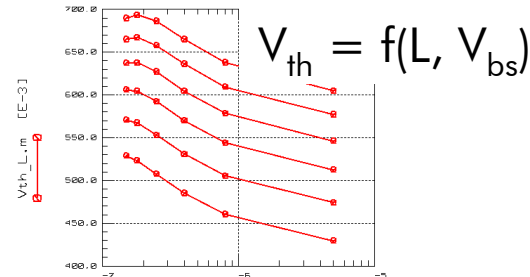
Advanced data representation concept

Collect data of up to 30 test structures during measurement phase of:



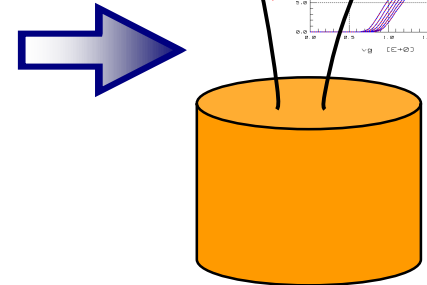
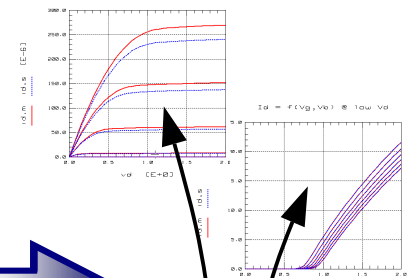
I-V, C-V curves etc.

Generate condensed data arrays for e.g.:



- Extraction of geometry dependant effects and parameters
- meaningful data representation

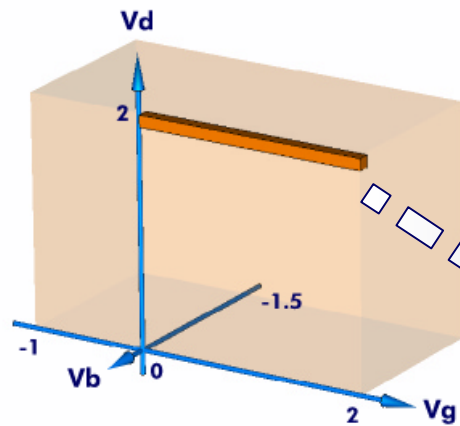
Individual device data display:



Load curves from a database if necessary.

Advanced data representation concept

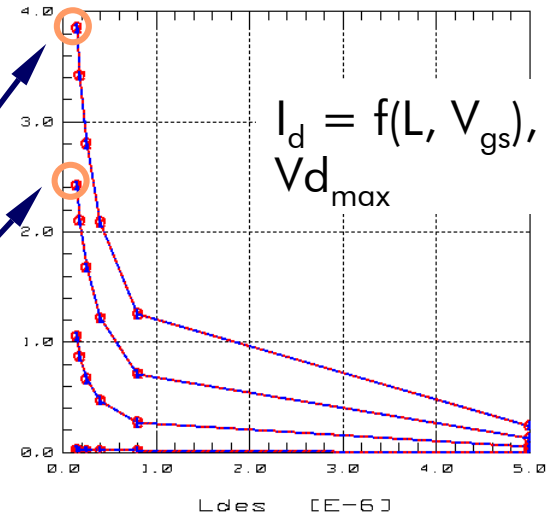
Terminal voltage space for one device:



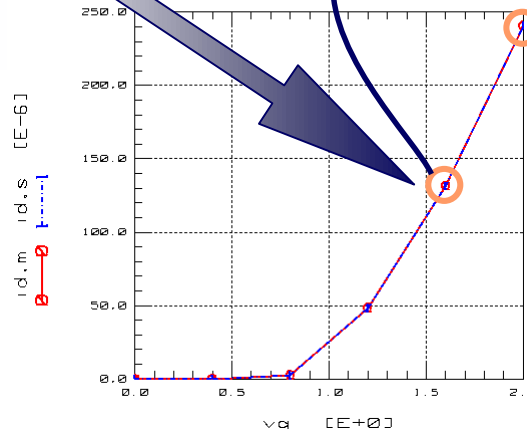
Cut out a representative sub-region for certain effects.

Combine voltage sub-region with length-scaling

$$I_d = f(L_{des}, V_g) @ V_{dmax}, V_b = 0$$



$$I_d = f(V_g) @ \text{high } V_d$$



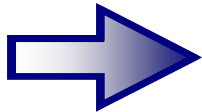
New data array with these properties:

Sweep Order	Variable
1	L_{des}
2	V_g

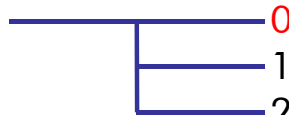




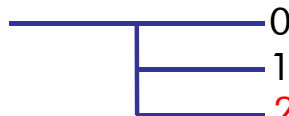

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BSIM4 sub-models

- BSIM4 has roughly 240 model parameters !
- A lot of parameters depend on the selected sub-model !
- In BSIM4, 14 sub-model flags can be set to configure the model behavior.



**Correct selection
is essential for
parameter
extraction !!**

Effect	Sub-model and selection
Mobility	MOBMOD 
Drain/source resistance	RDSMOD 
Gate to channel tunneling current	IGCMOD 
Gate to substrate tunneling current	IGBMOD 
Capacitance	CAPMOD 
Drain/source junction diode	DIOMOD 
Gate edge perimeter	PERMOD 

BSIM4 sub model selection flags for DC / CV

The physical effects, which affects the device behavior of typical CMOS processes below a minimum device dimension of 0.25um are mostly overlaying each other. Therefore, the following general strategy has been found to give best results in the determination of the huge amount of model parameters, describing these effects:

- Identification, whether a certain effect can be observed in the used data set. (CMOS processes of different manufacturers can show very different behavior !!).
- Isolation of a certain physical effect and usage of a meaningful data representation.
- Model parameter extraction using direct extractions, optimizers or tuners on this condensed data representation

This strategy will be demonstrated on the following pages using the threshold voltage $V_{th} = f(L)$ in BSIM4.

Example: BSIM4 threshold voltage

BSIM4 Vth

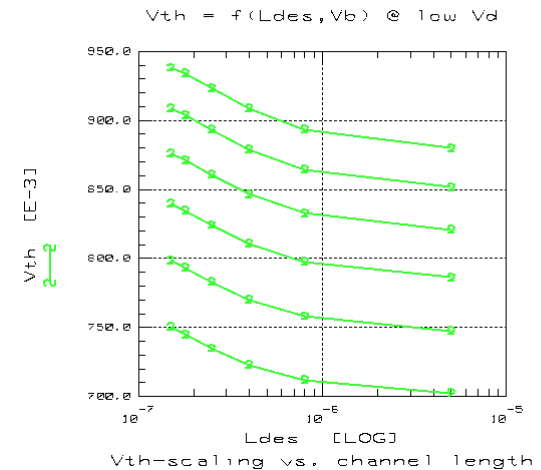
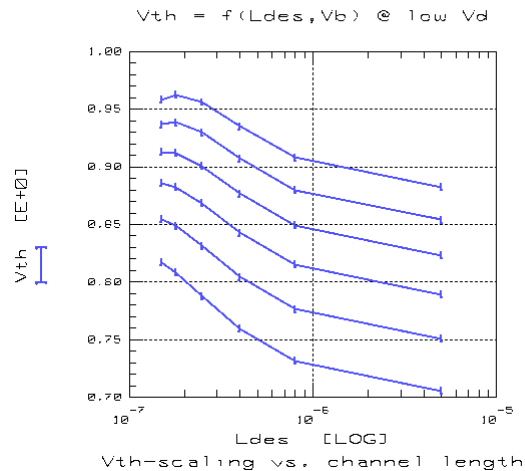
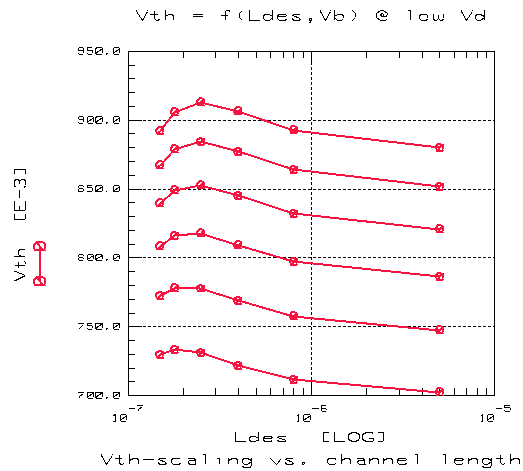
- The threshold voltage in BSIM4 is a complex equation, which is scalable for gate length and width.
- Vth uses 19 model parameters to achieve this scalability!

$$\begin{aligned}
 V_{th} = & VTH0 + \left(K_{1ox} \cdot \sqrt{\Phi_s - V_{bseff}} - K1 \cdot \sqrt{\Phi_s} \right) \sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox} V_{bseff} \\
 & + K_{1ox} \left(\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1 \right) \sqrt{\Phi_s} + \left(K3 + K3B \cdot V_{bseff} \right) \frac{TOXE}{W_{eff}' + W0} \Phi_s \\
 & - 0.5 \cdot \left[\frac{DVT0W}{\cosh\left(DVT1W \frac{L_{eff}W_{eff}'}{l_w}\right) - 1} - \frac{DVT0}{\cosh\left(DVT1 \frac{L_{eff}}{l_t}\right) - 1} \right] (V_{bi} - \Phi_s) \\
 & - \frac{0.5}{\cosh\left(DSUB \frac{L_{eff}}{l_{cs}}\right) - 1} (ETA0 + ETAB \cdot V_{bseff}) \cdot V_{ds} \\
 & - n v_t \cdot \ln \left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot (1 + e^{-DVTP1 \cdot V_{ds}})} \right)
 \end{aligned}$$

The extraction flow for the marked effects (Vth = f(L, Vbs) @ low Vds) will be demonstrated.

Identify technology dependant effects

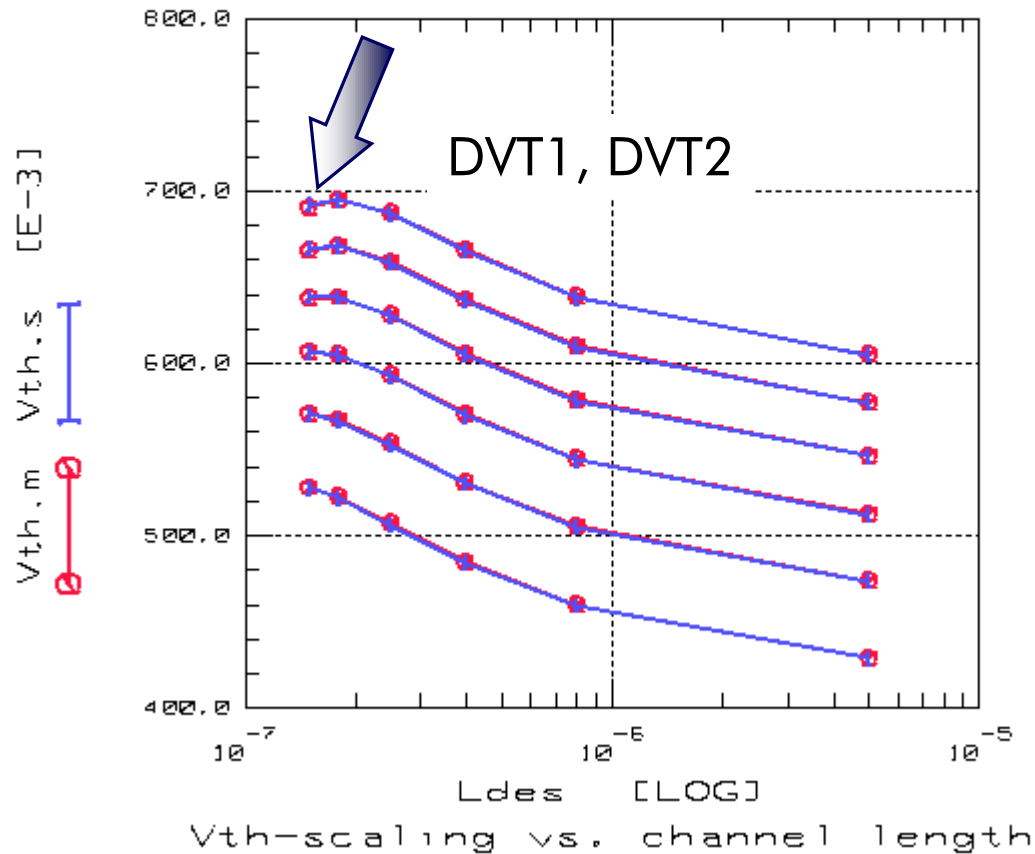
The diagrams show 3 typical patterns for $V_{th} = f(L, V_{bs})$ @ low V_d which can be observed in ultra deep submicron CMOS processes.



Depending on these different patterns, the model extraction flow is configured in a certain way to determine the relevant parameters.

Parameter extraction steps for pattern #2

$$V_{th} = f(L_{des}, V_b) @ \text{low } V_d$$



Summary and outlook

- A complete model parameter extraction strategy for the UCB BSIM4 simulation model could be demonstrated. This strategy includes test pattern design, measurement items, advanced data representation and intelligent parameter determination.
- The special emphasis of this method is, to account for scalable (channel length / width) physical effects with advanced data representation and parameter extraction methods.
- Such a dedicated methodology is necessary to handle the BSIM4 model with its large amount of model parameters and the variety of different configuration possibilities.
- We are currently on the way to verify these BSIM4 methods with 0.18um CMOS data and will continue to work on 0.15um processes and below.