Digital MOS Scaling Challenges--

Impact on Circuit Performance and Reliability

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- Introduction
- TCAD-based Modeling:
  - Analog and Digital Challenges
- Summary

Introduction

- Technology scaling dominantly about digital drive current and parasitic effects (leakage, capacitance, resistance)
- Power limits and the “end of voltage scaling” for silicon is now motivating consideration of alternative materials
- Band-structure engineering is becoming essential; implications for device modeling are many
- TCAD-based modeling supports both device design and development of compact circuit models

Technology-Dependent Circuit Design Issues

•Design requires good models…needed to predict scaling trends and "sweet spots" (shifts with each technology node, especially for analog)

•Variability impacts everything--digital and analog (choices for digital drive-current can adversely impact non-minimum channel length devices*, a major issue for analog).

•The technology inflections (strain, high-k gates etc.) are having major impact on modeling for both digital and analog (and parameterization for design)

***fundamental question**--will channel-length scaling survive for performance-oriented digital??

Performance Issues--Analog Perspective

Different “flavors” of Transistors can help (**if** they are available)…

I_{ds}

CMOS core

??

I/O for HV interface

DE* core for current sources

Drain-
Extended

STI

1.8V 3.3V

*TI, VLSI Technology 2003

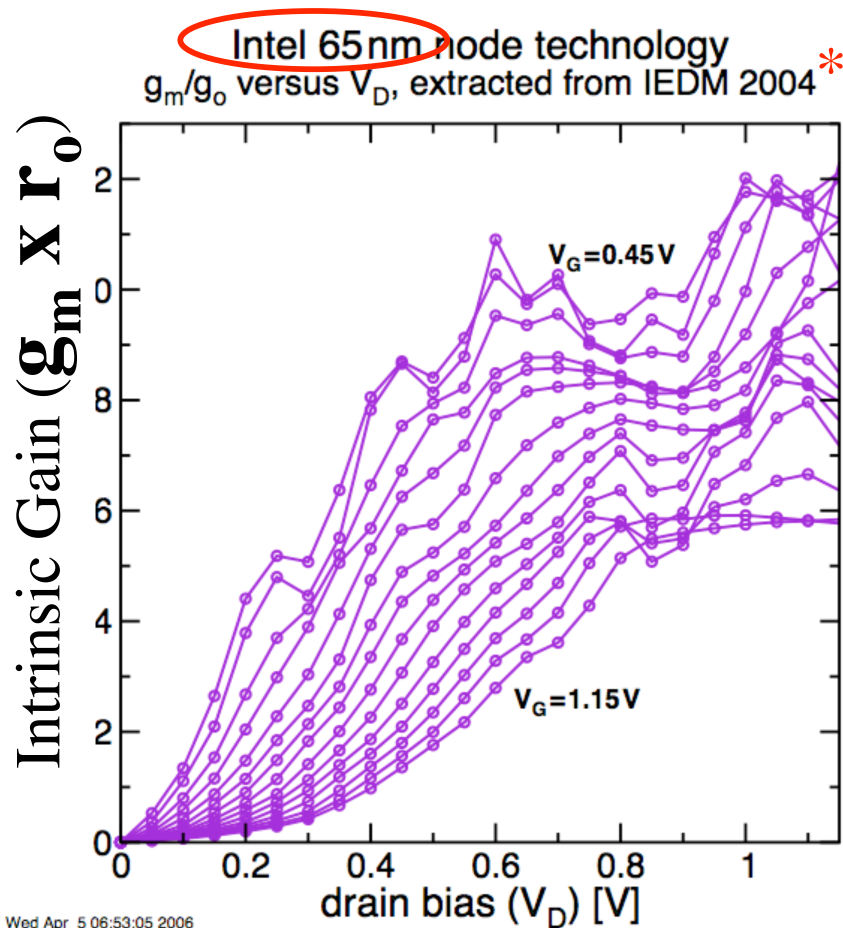
Digital drive current (+)
Intrinsic Gain (--) $= g_m r_o$

Speed (+/-)
Intrinsic Gain (+)
Process Integration (+)

Domain with most flexibility

Speed (-)
Intrinsic Gain (++),
Voltage (+)
Process Integration (?/-)

Modeling Challenges--Data vs. TCAD



- **Data** is <u>not sufficiently smooth</u> that one can use it for analog performance metrics

- <u>Calibrated</u> TCAD opens the door for **computational experiments**, but trends in scaling make this much more difficult (I.e. new materials** and related physics)

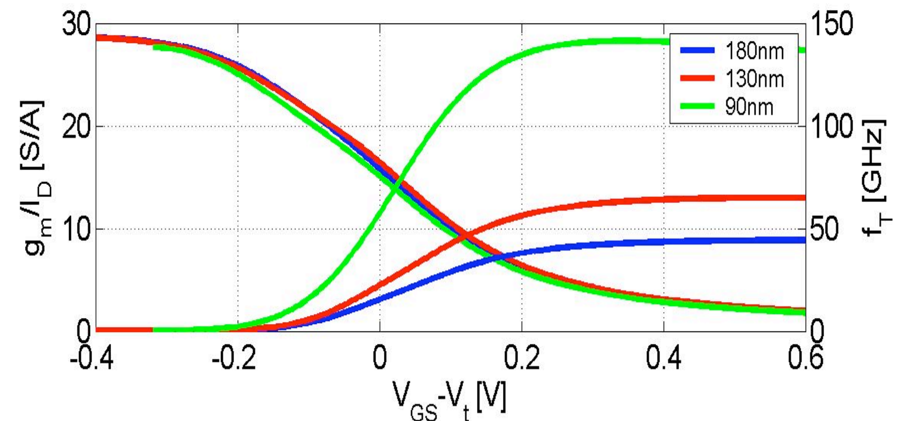
*"noise" in data a result of both "scanning" + large ΔVs

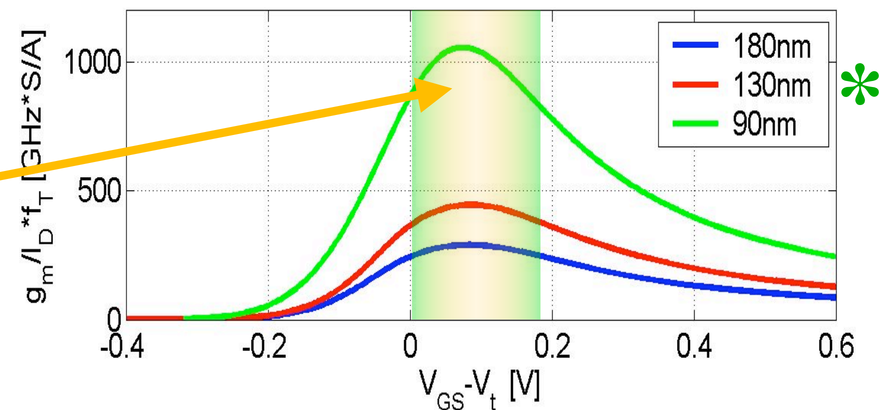
** a focus of Stanford TCAD Group efforts

Metrics for Analog Performance*

Analog metrics:

- $g_m * r_o$: Intrinsic gain
- g_m/I_d : metric for power efficiency
- $\omega_t = g_m/C_{gg}$: metric for self-loaded bandwidth
- $g_m/I_d * f_t$: tradeoff (finding the "sweet spot")



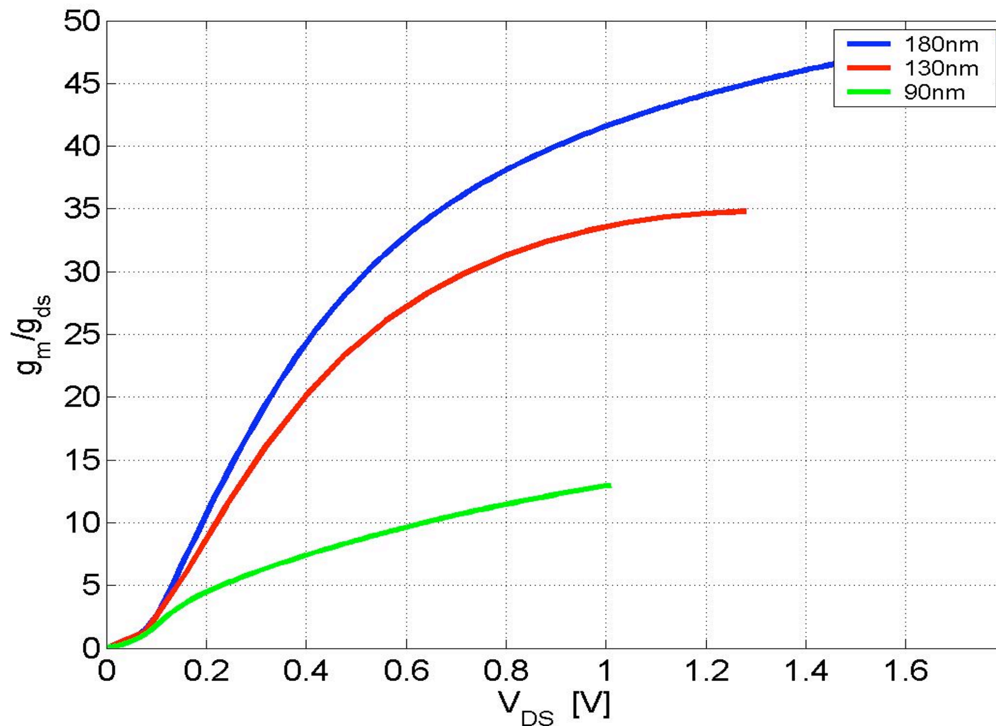


*B. Murmann, R. Dutton et al, IEEE TED, Sept. 2006

*These data are base on BSIM Foundry Model Parameters

Intrinsic Gain--A Challenge…

(even for older technology nodes)

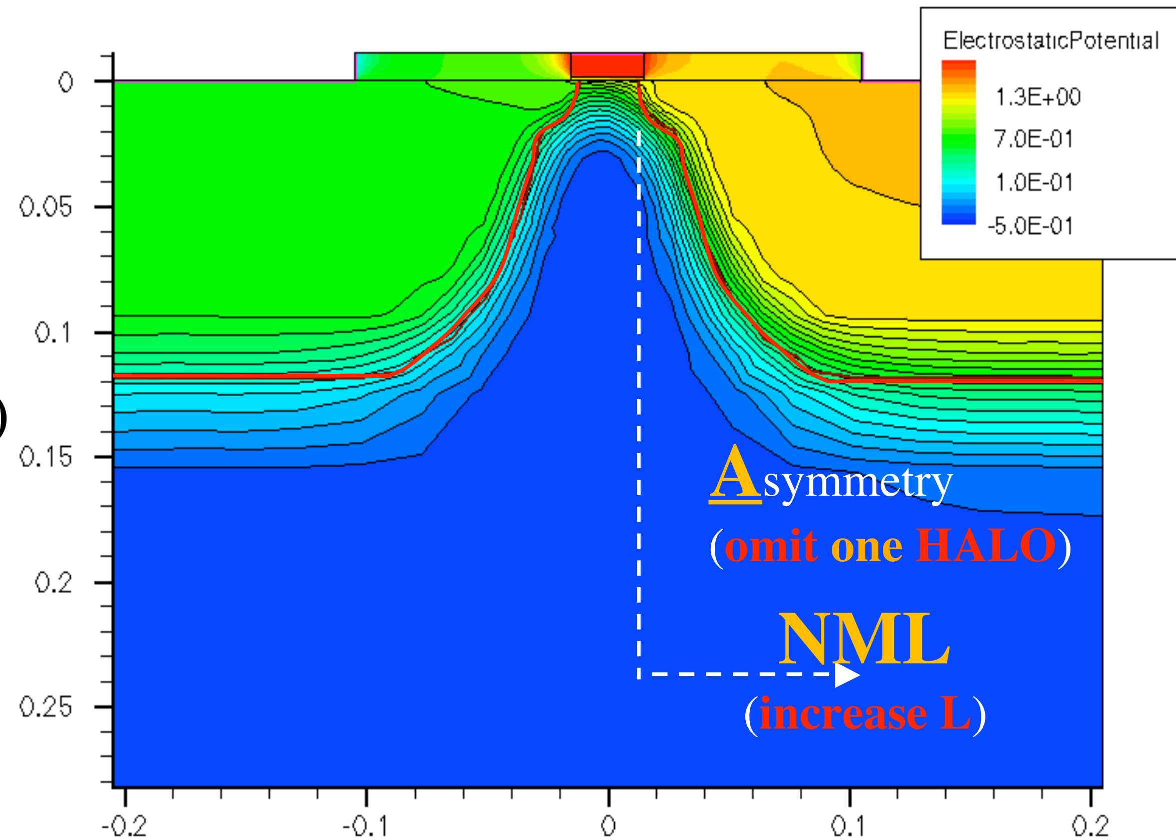


- BSIM parameters for <u>typical foundry processes</u>
- Even 90nm devices have challenges, <u>future generations get worse</u> based on TCAD modeling
- Minimum Length (ML) devices are bad for gain…but what happens for Non-ML devices??

Murmann et al

"What if" changes with Electro-statically "Well-Tempered" MOS (sub-45nm)

- Source/Drain doping levels and junction depths, based on ITRS projections
- HALO doping (and L) profiles adjusted to achieve the necessary <u>sub-threshold slope</u>

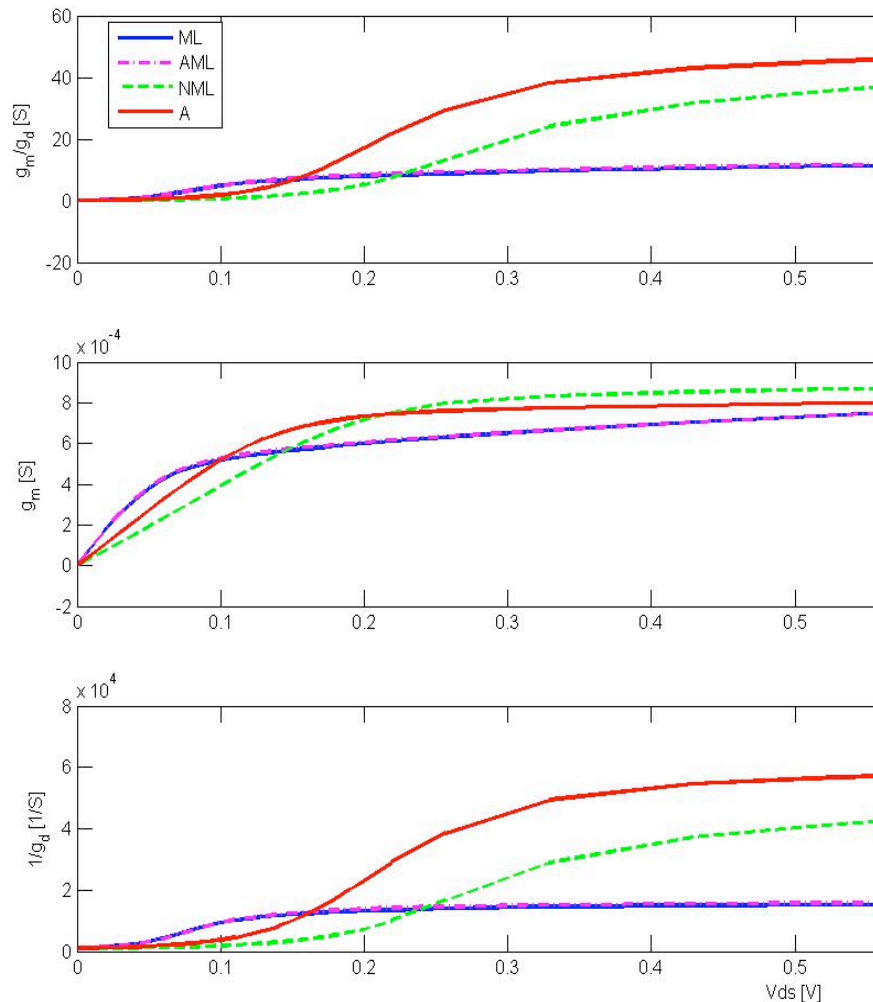


TCAD Experiments with HALO and L

Min. L (ML)
(nominal dev.)

Non-ML A-dev.
(double HALO) (Single HALO)

Intrinsic Gain Trade-Offs



Interesting trends:

- Asymmetric (A) device has highest gain and transconductance
- Non-minimum length (NML) device is very sensitive to bias conditions
- Drain voltage (V_{ds}) "head room" needs to be considered

Other A-Device Modeling Issues

- LDMOS is an essential RF component; many challenges in terms compact modeling
  - Capacitance effects (Philips papers + CMC)
  - Distortion (Infineon, MTT 2006 & 2007)
- Drain-Extended (DE) devices useful for higher voltage I/O; trade-offs from ESD perspective (TI)
- Digital trade-offs as well; high doping not good for mobility (AMD)

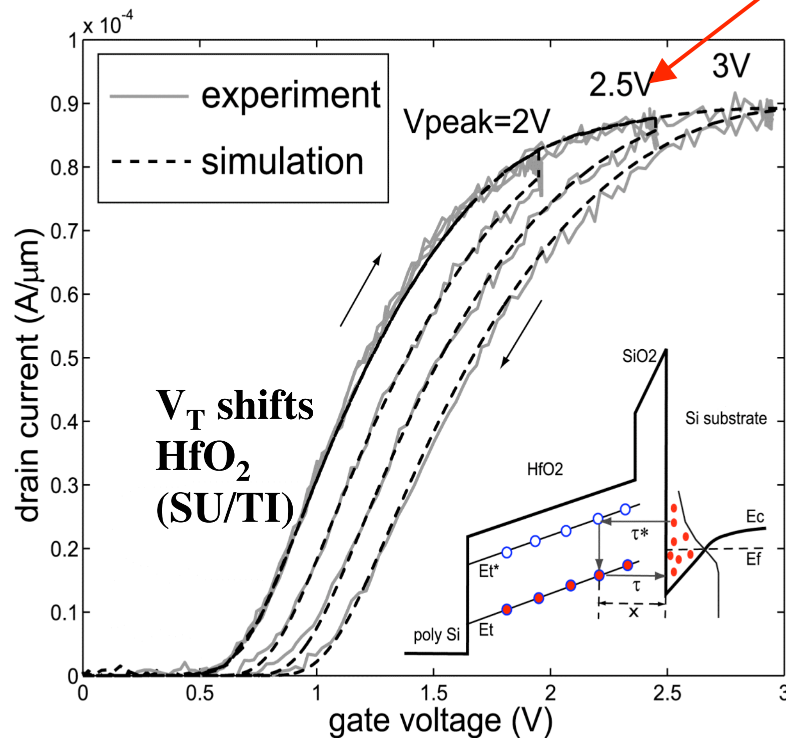
Other Scaling Trends

(and modeling implications)

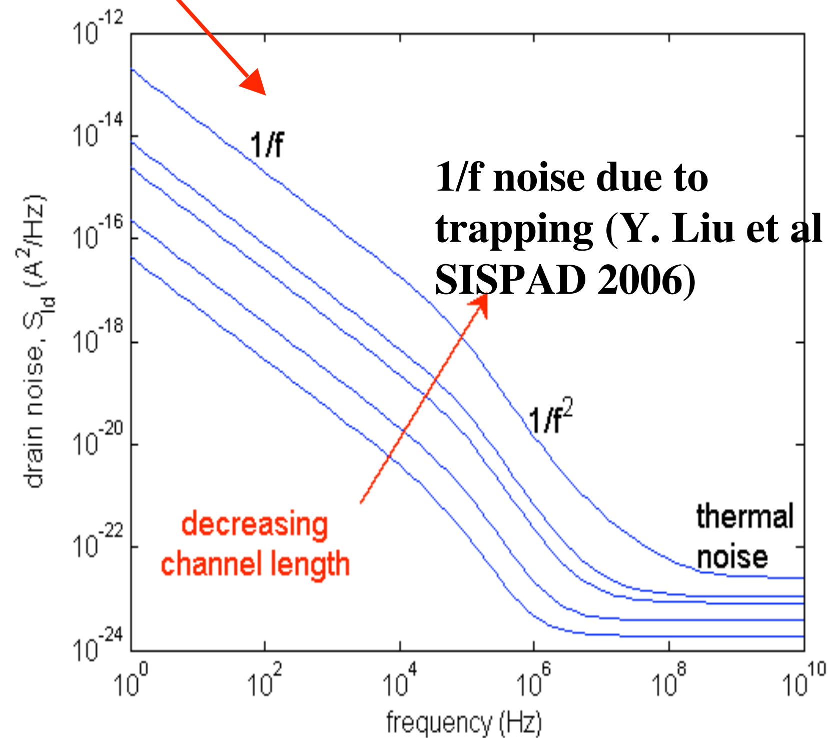
- High-K gate stack, needed for electrostatics and power
  - *Interface and trapping issues need to be modeled*
- High mobility and hetero-junction devices for drive current
  - *SiGe (short term); III-V (longer term)*
  - *Major emphasis on band structure engineering*

Effects on High-K Gate Dielectrics

Gate stack has many issues, both material/processing and electrical…trapping (DC and AC)



V_T shifts HfO_2 (SU/TI)



1/f noise due to trapping (Y. Liu et al SISPAD 2006)

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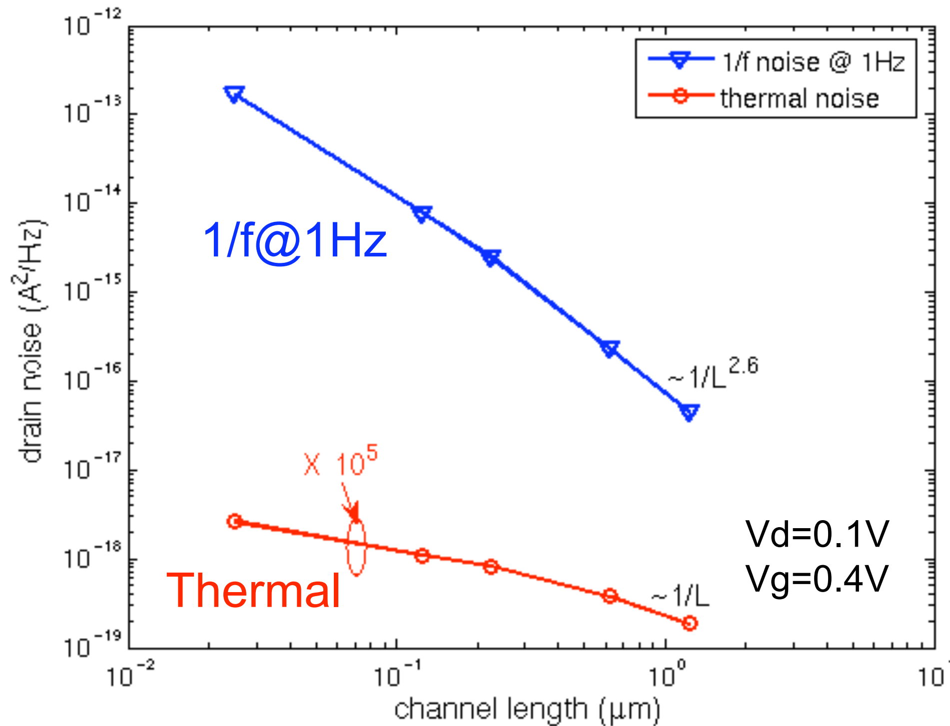
Scaling of Low Frequency Noise

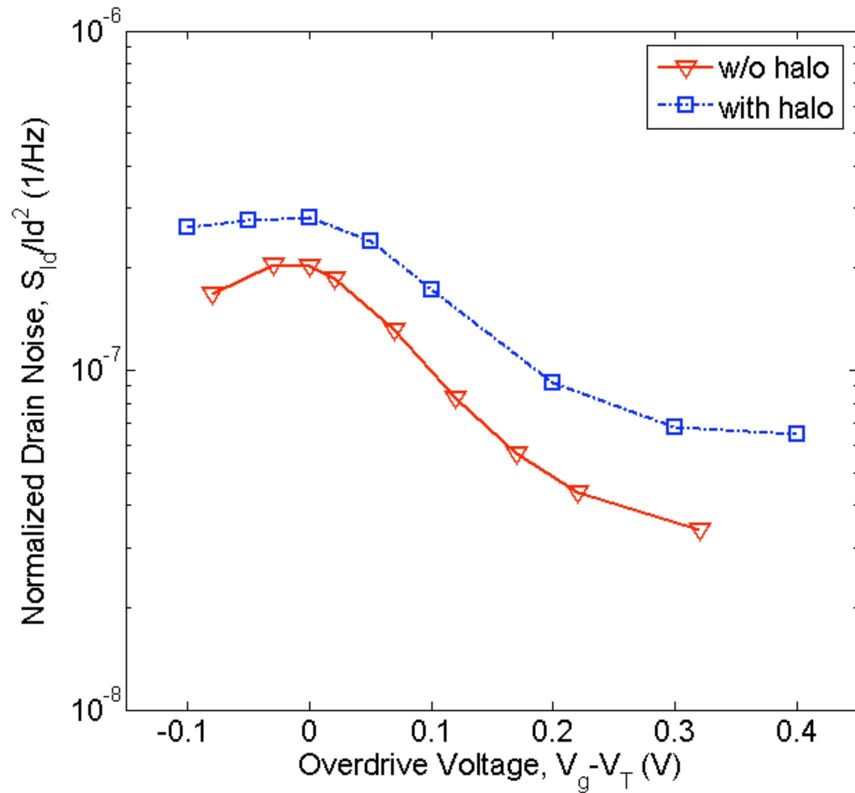


Observations:

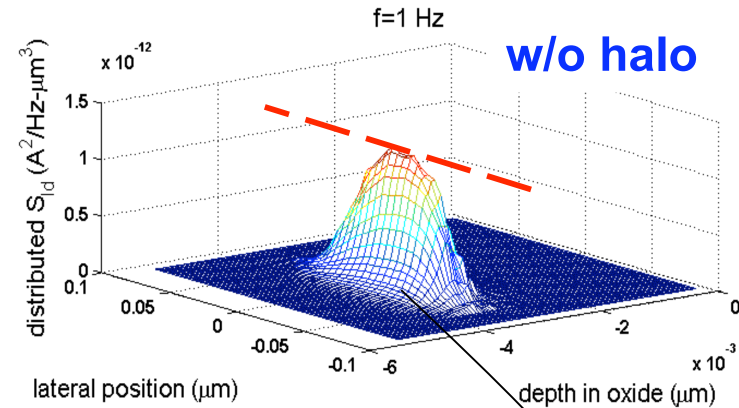
- Significant 1/f noise in high-k devices
- Transition from 1/f to $1/f^2$ due to reduced trap density in interfacial layer
- Channel length scaling: 1/f increases faster than thermal noise

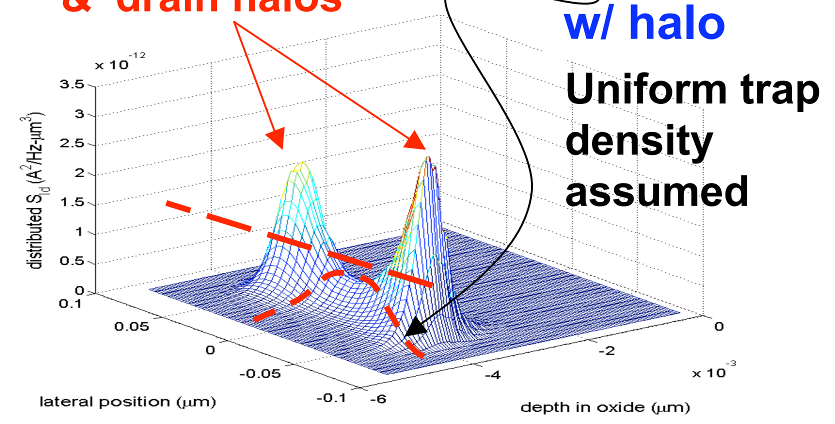
Yang LIU et al

Effect of Halo Doping



Increase of normalized drain noise due to halo doping





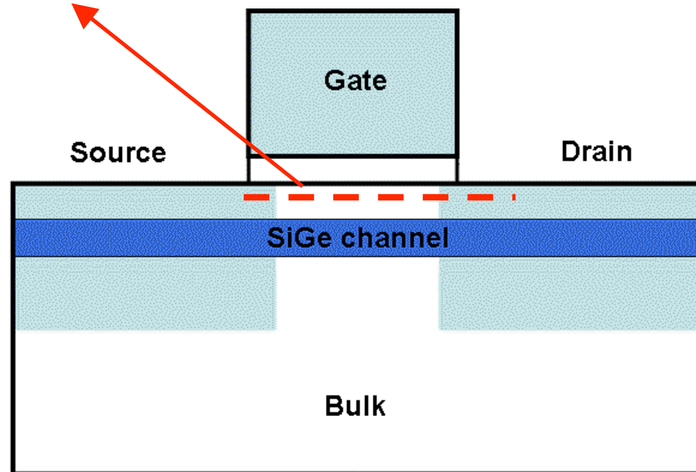
Distributed oxide noise contribution

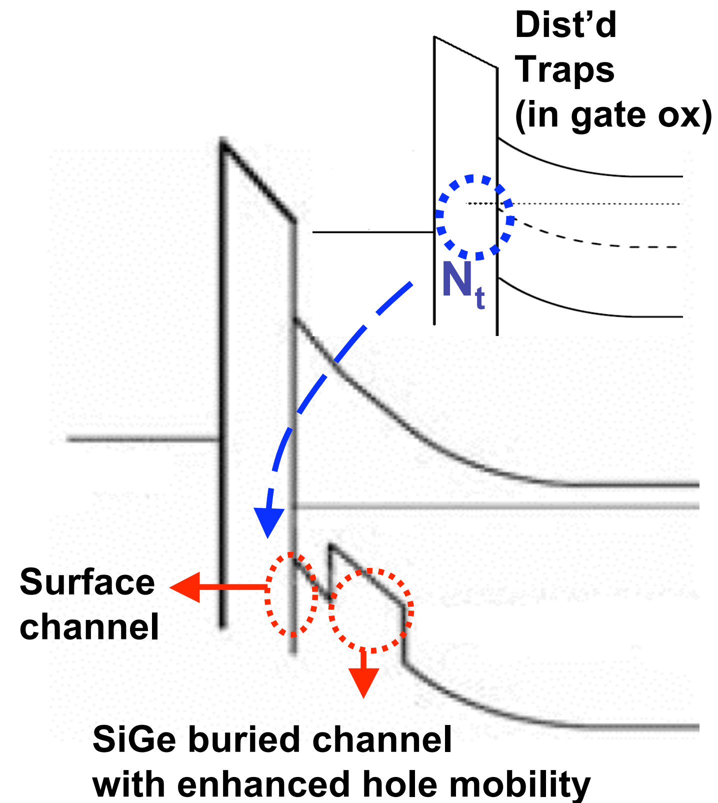
Ongoing Scaling Trends
(and modeling implications)

- High-K gate stack, needed for electrostatics and power
  - *Interface and trapping issues need to be modeled*
- High mobility and hetero-junction devices for drive current
  - *SiGe (short term); III-V (longer term)*
  - *Major emphasis on band structure engineering*

Buried channel SiGe pHMOS

- Higher Transconductance (g_m)
- Lower 1/f Noise

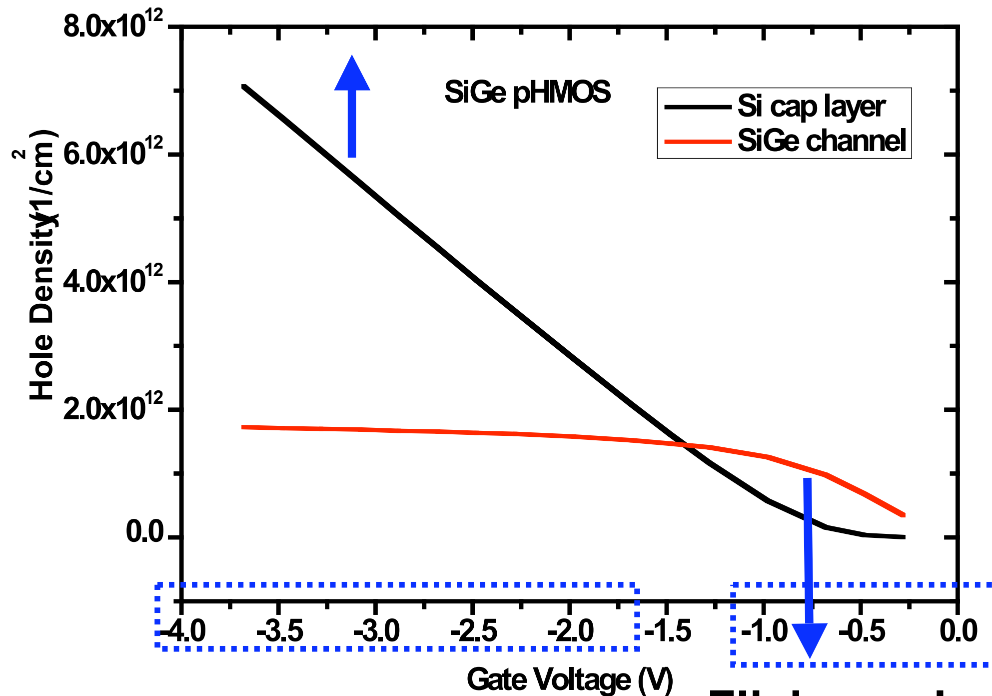




C-Y Chen, Y. Liu,
S. Cao et al, WCM 2007

Hole densities in respective channels

Flicker noise behavior is like a Si bulk pMOS



Flicker noise behavior is mainly from the conductivity fluctuations of SiGe buried channel

(TCAD model considers differences in mobility dependencies and amounts of charge)

C-Y Chen, Y. Liu, S. Cao et al, WCM 2007

Body bias dependence of noise spectrum

L=1um, W=10um
Vd=-0.5V, Vg-Vt=-0.3V
Vb=0.2V∽-0.4V (0.1V step)
0.2V
-0.4V
1/f
SiGe pHMOS
S_{Id} [A^2/Hz]
1.E-17
1.E-18
1.E-19
1.E-20
1.E-21
1.E-22
1.E-23
1.E-24
1
10
100
1000
10000
Frequency [Hz]

L=1um, W=10um
Vd=-0.5V, Vg-Vt=-0.3V
Vb=0.2V~-0.4V(0.1V step)
1/f
Bulk pMOS
(benchmark)
S_{Id} [1/Hz]
1.E-17
1.E-18
1.E-19
1.E-20
1.E-21
1.E-22
1.E-23
1.E-24
1
10
100
1000
10000
Frequency [Hz]

- **Moving charge away from oxide interface improves noise performance**
- **Implications for High-K devices as well as consideration of III-V options**

C-Y Chen, Y. Liu, S. Cao et al, WCM 2007

Hole Density in Si cap layer and SiGe channel vs. Body Bias

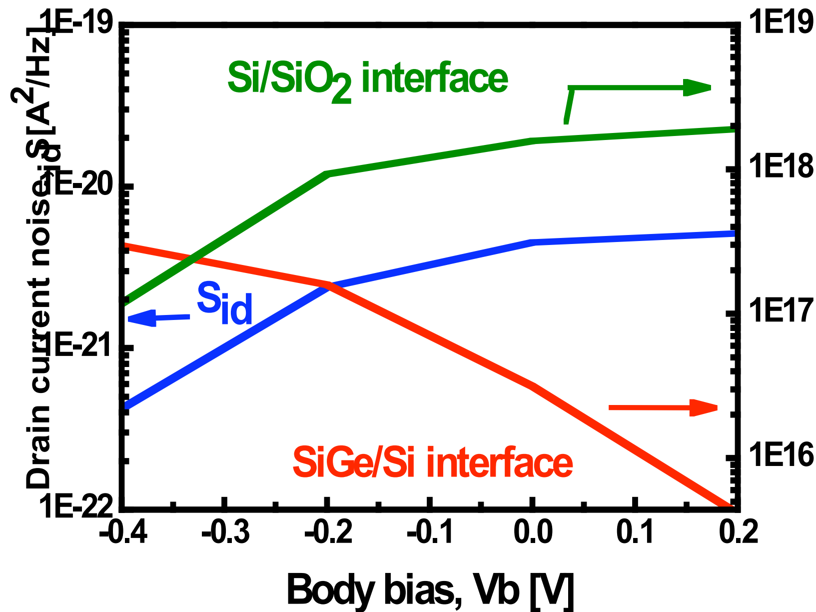


Fig.1 PROPHET simulations (both left and right y-axes)

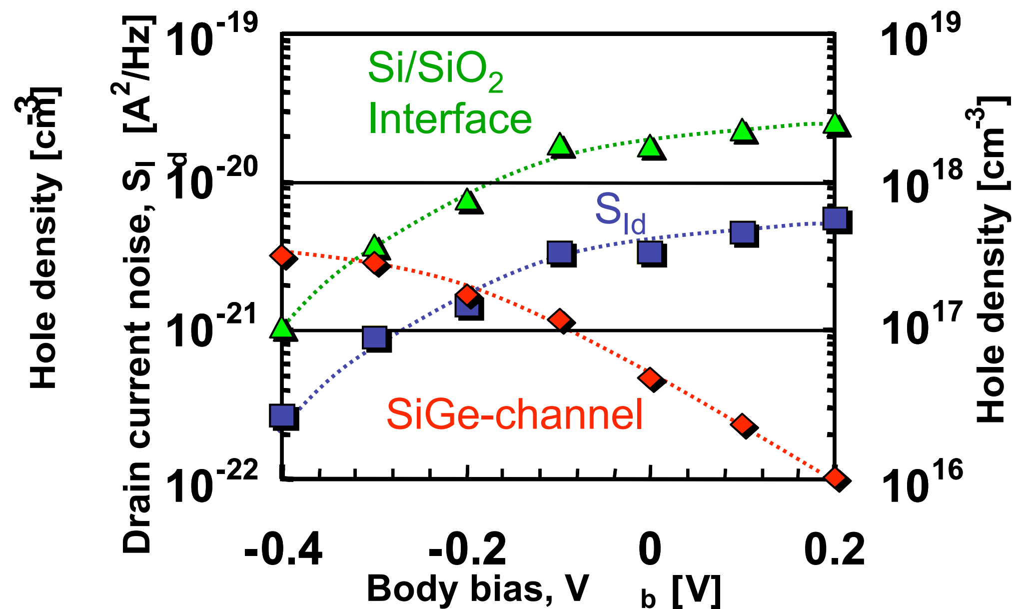


Fig.2 Medici simulations (right) and noise measurements (left)

▶ PROPHET simulations show good agreement with Medici carrier density at interfaces and measured S_{id} from Matsushita

C-Y Chen, Y. Liu, et al, SASIMI 2007

Noise Spectrum for body bias dependence

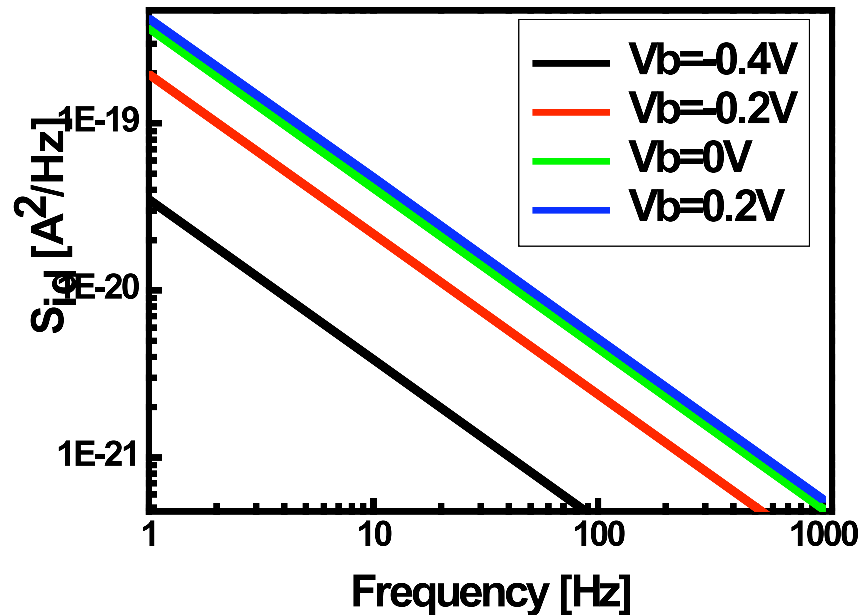


Fig. 3 PROPHET simulations

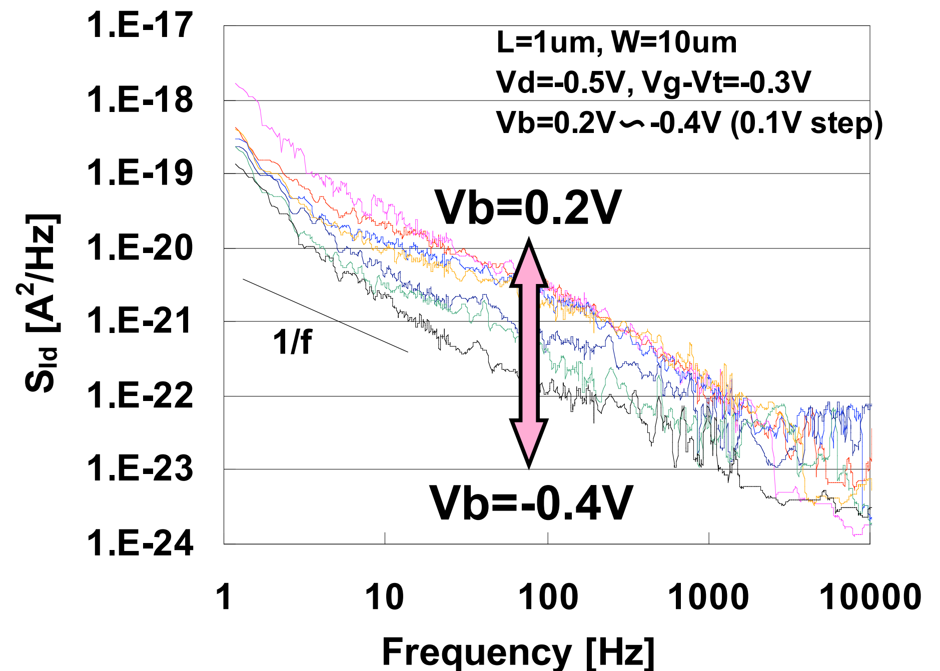
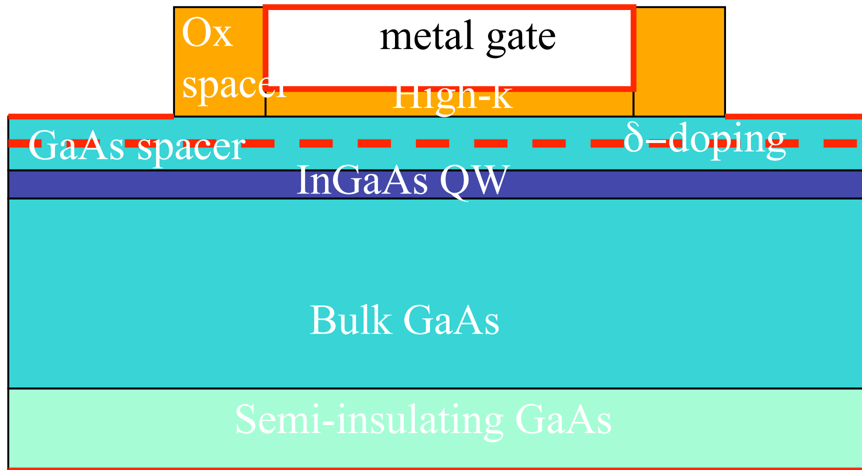


Fig.4 Low frequency noise measurements

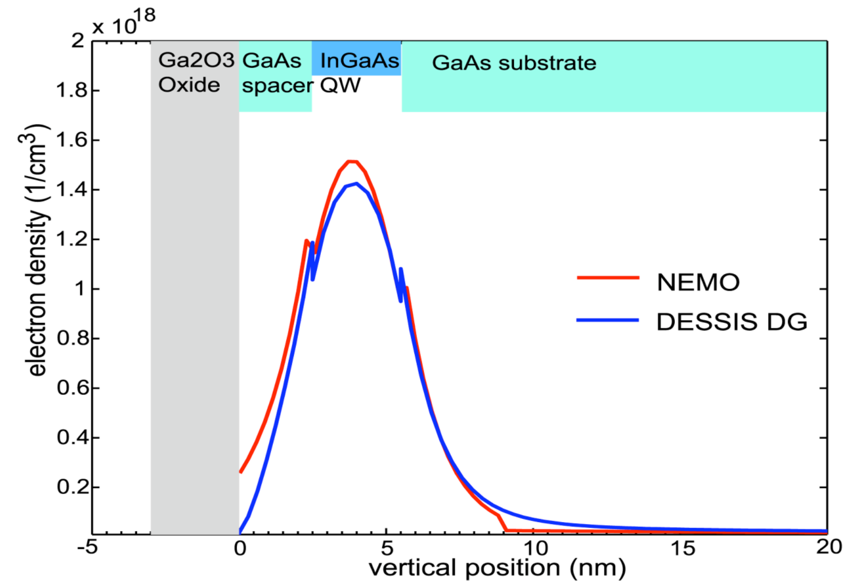
- PROPHET noise simulations show good agreement with low frequency noise measurements from Matsushita (WCM 2007).

C-Y Chen, Y. Liu, et al, SASIMI 2007

Other High-Mobility Channel Hetero-MOSFETs



Typical Example *Passlack et al., US Patent 2004*

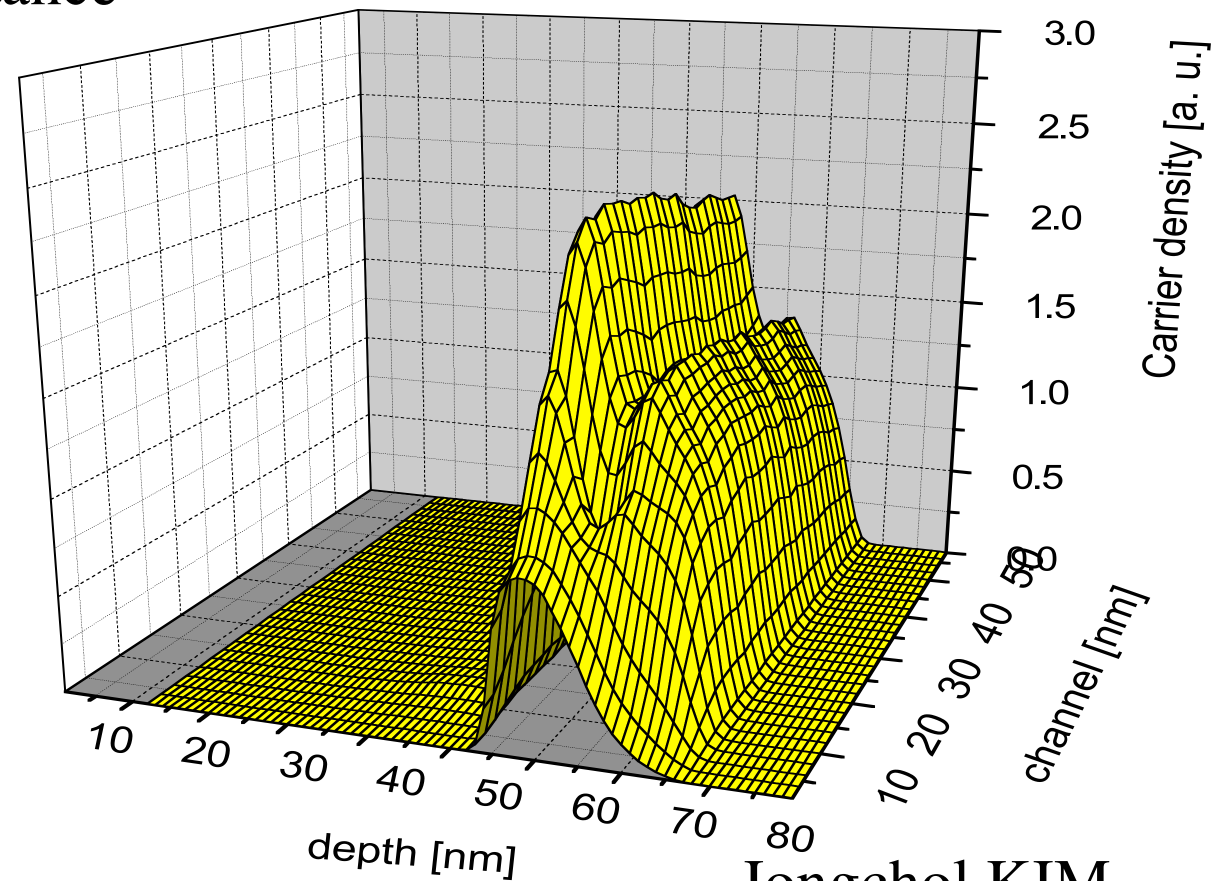


Calibration of QM effects in quantum well and equivalent density gradient (DG) approximation in commercial TCAD tool DESSIS.

Motivation: Extremely high electron mobilities; feasibility demonstrated (several groups, **del Alamo/MIT**); re-invigorates voltage scaling (power)
Challenge: Materials-based (new) scaling issues

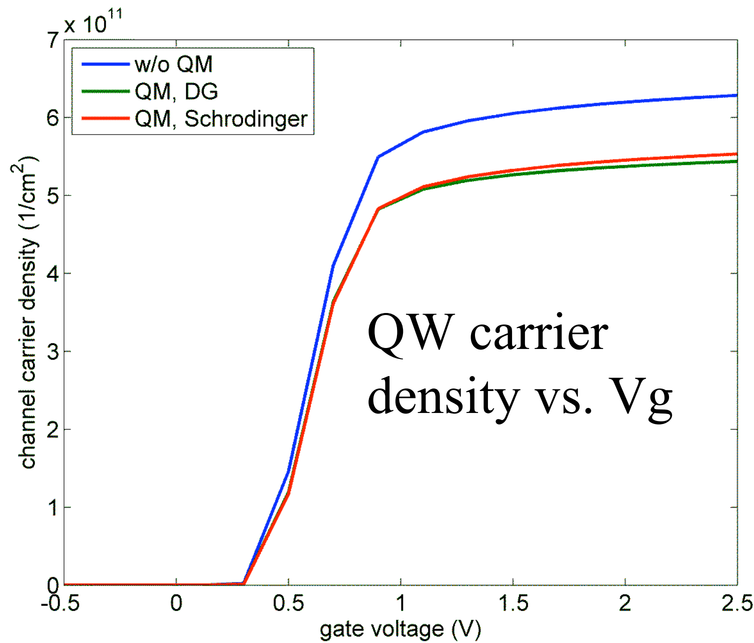
Charge Distribution within Channel

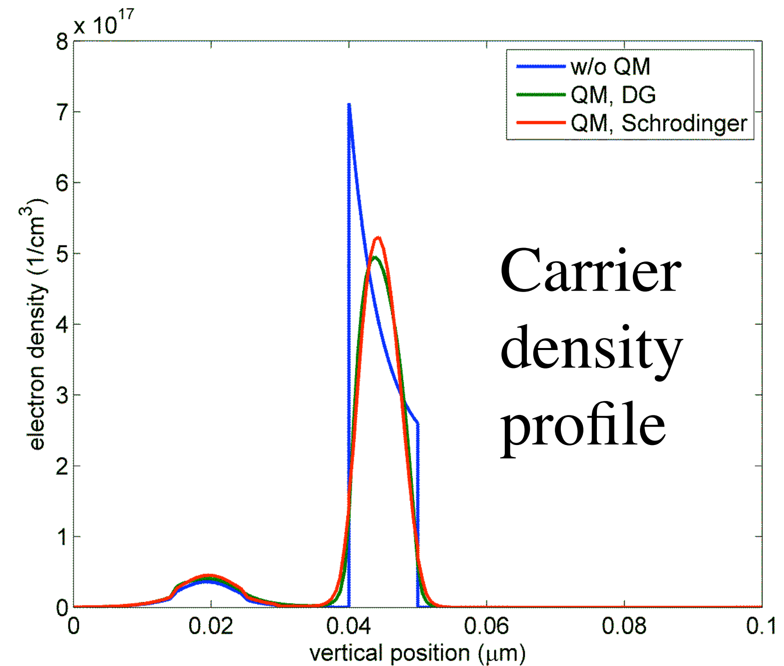
Modeling Challenges: Need to consider multiple layers of charge, different mobilities and multi-layer capacitance



Jongchol KIM

Density Gradient vs. Schrödinger Solver





RESULTS:

- Density Gradient (DG) method calibrated against Schrödinger-Poisson solver
- DG--satisfactory accuracy for 2-D device simulations

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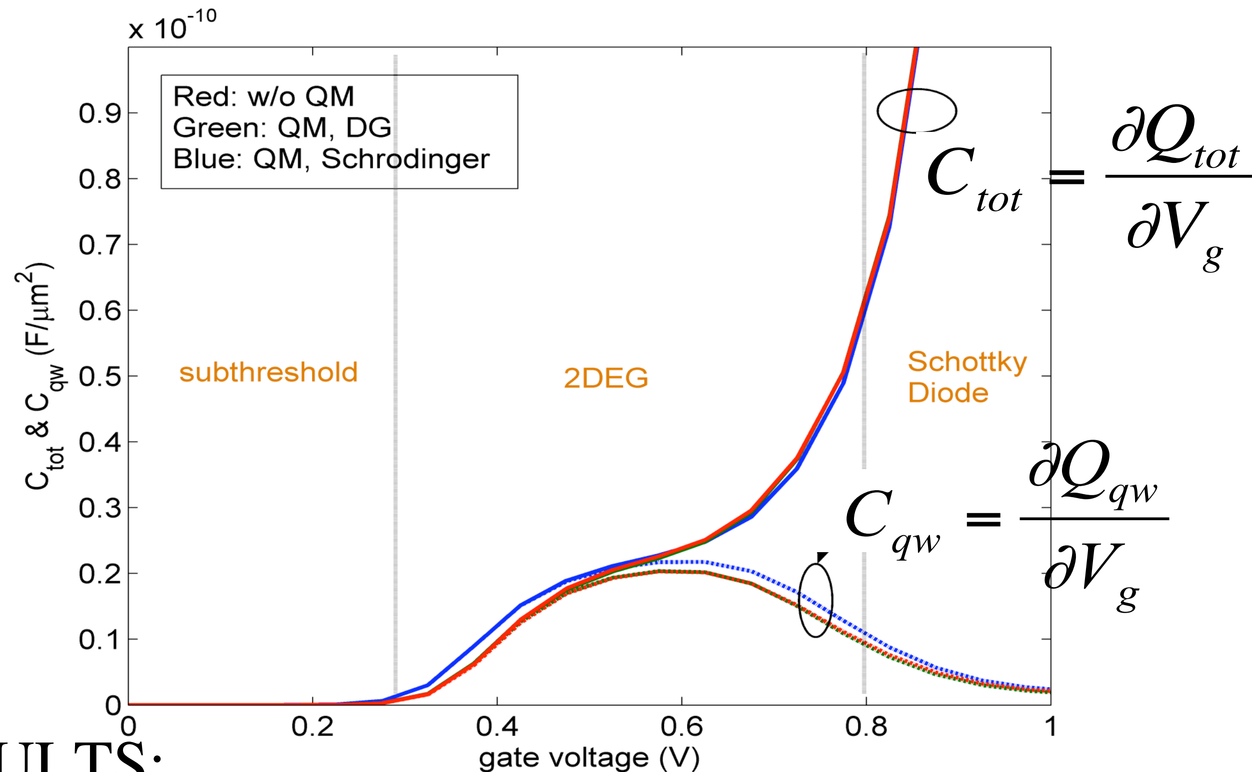
Gate Mod. Efficiency: Simulated Capacitance



RESULTS:

- Three regions of charge-formation evident: need to maintain operation below turn-on of parasitic channel
- QW effect gives 10~15% correction in C_{qw} in 2DEG regime

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Summary

- Digitally-driven scaling of MOS poses challenges for Analog Design; New materials make this even more complex
- TCAD-based modeling provides:
  - Detailed understanding of interplay between key technology model parameters
  - Approach for new materials (including challenge of calibration issues) offers further leverage
- Growing number of Compact Modeling challenges, especially due to quantum-based and other 2D/3D effects