Modeling and Parameter Extraction Experiences with PSP:
An Advanced Surface-Potential-Based MOSFET Compact Model for Circuit Simulation

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Outline

- Introduction
- PSP Parameter Extraction Strategy
- PSP Modeling Examples
- Statistical Modeling with PSP
  - Methodology of Corner Model Generation
  - Example and Verification
- PSP Runtimes
- Outlook
- Conclusion
Introduction: Basics of PSP

- PSP is the new the “Next Generation CMC Standard MOSFET Compact Model” (successor of BSIM4) for advanced digital, analog, mixed signal and RF circuit simulations.
- PSP is the merger of MOS Model 11 (Philips) and SP (PennState) - combines and enhances the advantages of MM11 and SP.
- PSP is a surface-potential-based model, which is physically the best know compact modeling approach (3’rd generation SPICE models).
- PSP use a $\Phi_S$-approximation with very high accuracy (error < 1nV).
- Non-singular velocity-field relation enabling the modeling of RF harmonic distortions including intermodulation effects (IM3).
- The $\Phi_S$-based PSP model has an accurate transition from weak to strong inversion (i.e. in moderate inversion, which is good for analog).
- PSP is symmetrical and continuous for all regions of device operation (passed all CMC benchmark tests, e.g. complete Gummel symmetry).
- Inclusion of all relevant small-geometry effects (like halo, stress, etc.).
Introduction: Structure of PSP

Geometry Scaling

Stress Model

Temperature Scaling

Model Equations

$W, L$

$MULT$

$SA, SB$

$T$

Local

Global

$V_{SB}$

$V_{GS}$

$V_{DS}$

Currents

Charges

Noise
PSP: Parameter Extraction Strategy

- I-V and C-V measurements
  - For required DC and CV measurements refer to the PSP manual at Section 7.1

- Global AC parameters (optional)

- Local parameters for each DUT

- Temperature scaling parameters

- Geometry scaling parameters

- Final global parameter set *

  * fine-tuned by optimization on multiple DUTs
PSP: Extraction of Local Parameters
Optimization Flow

- flat-band voltage/poly depletion
- (sub)-threshold parameters
- mobility/series-resistance
- velocity saturation/conductance
- gate current parameters
- $I_{\text{SUB}}$: GIDL & impact ionization

C-V characteristics
(optional; otherwise from global)

I-V characteristics
(DC-parameters)

Note: Sequence for $T_{\text{NOM}}$ - several steps will be repeated for different temperatures - (at least for $T_{\text{MAX}}$ and $T_{\text{MIN}}$)
PSP102: Extraction of Local DC-Parameters
Optimization Examples for a Wide Long Device

Transfer Characteristics

Output Characteristic

NEFF, DPHIB, VT and body-effect
CT, Sub-VT slope
MUE, Phonon scattering
THEMU, Surface scattering
Vds = 50mV, linear mode
Vds = Vdd, saturation
Vbs = 0V
XCOR, FETA, Vbs-dependence
BETN, gmmax
CS, Coulomb scattering
THESAT, VSAT
ALP, (VP) - gds:
CLM pre-factor
ALP1 for gds:
CLM above Vt
ALP2 for gds:
CLM below Vt
AX, linear/sat transition
ALP for gds:
CLM below Vt

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PSP: Extraction of Global Scaling Parameters
Methodology

Extraction of geometry-dependent parameters, e.g. for the calculation of effective mobility and doping, using physical geometrical scaling rules and some semi-empirical geometrical scaling rules (no binning).

Hint: Keep BETN and NSUB length scaling parameters fixed, as determined above, during optimization (fine-tuning) of the single device characteristics (as a physical basis for statistical model generation like fast/slow corners and MC models)!
PSP102: Extraction of Global Scaling Parameters

(1/11)

Process Parameters

$V_{FB} = V_{FBO} \cdot \left(1 + V_{FBL} \cdot \frac{L_{EN}}{L_{E}}\right) \left(1 + V_{FBW} \cdot \frac{W_{EN}}{W_{E}}\right) \left(1 + V_{FBLW} \cdot \frac{W_{EN} \cdot L_{EN}}{W_{E} \cdot L_{E}}\right)$

$S_{TFB} = S_{TFBO} \cdot \left(1 + S_{TFBL} \cdot \frac{L_{EN}}{L_{E}}\right) \left(1 + S_{TFBW} \cdot \frac{W_{EN}}{W_{E}}\right) \left(1 + S_{TFBLW} \cdot \frac{W_{EN} \cdot L_{EN}}{W_{E} \cdot L_{E}}\right)$

$D_{PHIB} = \left(D_{PHIBO} + D_{PHIBL} \left[\frac{L_{EN}}{L_{E}}\right]^{D_{PHIBLEXP}}\right) \left(1 + D_{PHIBW} \cdot \frac{W_{EN}}{W_{E}}\right) \left(1 + D_{PHIBLW} \cdot \frac{W_{EN} \cdot L_{EN}}{W_{E} \cdot L_{E}}\right)$

$^3$ global parameter extraction for devices of length-array at wide channel widths
$^4$ global parameter extraction for devices of width-array at long channel lengths
$^5$ global parameter extraction for devices of length-array at narrow channel widths
$^6$ global parameter extraction for devices of width-array at short channel length
**Table 7: Global DC-parameter extraction fine-tuning procedure at nominal temperature ($T_{\text{nom}}$)**

<table>
<thead>
<tr>
<th>Step</th>
<th>DUT</th>
<th>Optimized Parameters</th>
<th>Fitting Target</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LC</td>
<td>NSUBO, DPHIBO, ($VFBO^2$), CTO, (DNSUB, VNSUB, NSLP)(^4)</td>
<td>$\log I_d-V_g(V_b)$ at $V_{ds,\text{lin}}$</td>
<td>$V_{th0}$, body effect and sub-$V_t$ slope (bias-dependent body factor of $N_{eff}$)</td>
</tr>
<tr>
<td>2</td>
<td>LC</td>
<td>ININV LW, GC2O(^1), GC3O(^1), (CHIBO(^6))</td>
<td>$I_g(V_d)$ for $V_{gs} &gt; 0$V</td>
<td>Gate current in inversion</td>
</tr>
<tr>
<td>3</td>
<td>LC</td>
<td>GC0O(^1)</td>
<td>$I_g$ for $V_{gs} &lt; 0$V</td>
<td>Gate current in accumulation</td>
</tr>
<tr>
<td>4</td>
<td>LC</td>
<td>UO, MUEO, THEMUO(^1), CSO, FETAO(^3), XCORO</td>
<td>$I_d-V_g(V_b), \text{gm at } V_{ds,\text{lin}}$</td>
<td>Low-field mobility and mobility degradation/scattering parameters</td>
</tr>
<tr>
<td>5</td>
<td>LC</td>
<td>A1O, A2O(^1), A3O, A4O</td>
<td>$I_b-V_g(V_d)$ for $V_{gs} &gt; 0$V</td>
<td>Impact ionization parameters</td>
</tr>
<tr>
<td>6</td>
<td>LC</td>
<td>AGIDLW, BGIDLO(^1), CGIDL (^1)</td>
<td>$\log I_d-V_g(V_b)$ for $V_{gs} &lt; 0$V</td>
<td>GIDL parameters in saturation</td>
</tr>
<tr>
<td>7</td>
<td>LC</td>
<td>CTATGAT, (MEFTATGAT)(^5)</td>
<td>$\log I_d-V_g(V_b)$ for $V_{gs} \sim 0$V</td>
<td>TAT parameters in saturation</td>
</tr>
<tr>
<td>8</td>
<td>LC</td>
<td>THESATO</td>
<td>$I_d-V_d(V_b)$ at $V_{bs} = 0$V</td>
<td>Velocity saturation parameter</td>
</tr>
<tr>
<td>9</td>
<td>LC</td>
<td>ALPL, ALP1L1, ALP2L1, VPO(^1), (AXO(^5))</td>
<td>$\log g_{ds}$ at $V_{bs} = 0$V</td>
<td>CLM and saturation voltage parameters (lin/sat transition)</td>
</tr>
<tr>
<td>10</td>
<td>LA</td>
<td>NPCK, CPCK, POL1, POL2, ($VFBO^3$), DPHIBL, DPHIBLEXP, CTL, CTLEXP(^5)</td>
<td>$\log I_d-V_g(V_b)$ at $V_{ds,\text{lin}}$</td>
<td>Body effect and $V_t$-roll-up/off and sub-$V_t$ slope</td>
</tr>
<tr>
<td>11</td>
<td>LA</td>
<td>ISOVW</td>
<td>$I_g-V_g(V_d)$ for $V_{gs} \sim 0$V</td>
<td>Gate overlap current</td>
</tr>
<tr>
<td>12</td>
<td>LA</td>
<td>FBET1, LP1, FBET2, LP2, CSL, CSLEXP, XCORL, RSW1</td>
<td>$I_d-V_g(V_b), \text{gm at } V_{ds,\text{lin}}$</td>
<td>Mobility degradation/scattering and series resistance parameters</td>
</tr>
<tr>
<td>13</td>
<td>LA</td>
<td>CFL, CFLEXP, CFBO</td>
<td>$\log I_d-V_g(V_b)$ at $V_{ds,\text{sat}}$</td>
<td>DIBL effect on $V_{t,\text{sat}}$ (check gds too)</td>
</tr>
</tbody>
</table>
The IFX IC-CAP Modeling Tool for PSP: User Interface - Fine-Tuning of Global Parameters

Convenient optimization and fine tuning for single device and DC-scaling characteristics, by selection from DUT WxL matrix, using IC-CAP plot optimizer within IC-CAP multi-plot feature.
Example PSP Modeling: Id-Vg and Id-Vd

- 65nm NFET short channel characteristics - accurate DC model build (PSP102)

![Graphs showing Id-Vg and Id-Vd characteristics](image)

- $gm @ V_{ds} = 50\text{mV}$
  - transconductance

- $IdVg @ V_{ds} = 50\text{mV}$
  - transfer characteristic

- $IdVg @ V_{dd} = 1.2\text{V}$
  - transfer characteristic

- $IdVd @ V_{ds} = 0\text{V}$
  - output characteristic
Example PSP Modeling: Analog Figures

- 65nm NFET short channel characteristics - accurate analog model build (PSP102)

\[
K' = \frac{g_{msat}^2}{2 \cdot I_{dsat}}
\]

analog gain factor

\[
\text{gm3} = \frac{d^3 I_d}{d V_{gs}^3}
\]

(3rd-order derivative)

harmonic distortion

\[
V_a = -\left( \frac{I_d}{g_{ds} - V_d} \right)
\]

early voltage
### PSP Corner Model Generation Flow

#### Statistical Modeling

<table>
<thead>
<tr>
<th>Step</th>
<th>Varied Parameters</th>
<th>Target (Spec. limits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TOXO, VFBO, NSUBO, (DPHIBO)</td>
<td>wide/long $V_{tlin}$, ($I_{dlin}$, $I_{gate}$)</td>
</tr>
<tr>
<td>3</td>
<td>UO</td>
<td>wide/long $I_{dlin}$, $g_{m_max}$</td>
</tr>
<tr>
<td>4</td>
<td>LVARO, LAP $^1$, VFBL, (DPHIBL), CFL, NPCK, LPCK</td>
<td>wide/short $V_{tsat}$, $V_{tlin}$, $I_{dsat}$, body effect</td>
</tr>
<tr>
<td>6</td>
<td>RSW1, (THESATL)</td>
<td>wide/short $I_{dlin}$, $I_{dsat}$</td>
</tr>
<tr>
<td>7</td>
<td>WVARO, VFBLW, (DPHIBLW)</td>
<td>narrow/short $I_{dsat}$, $V_{tsat}$</td>
</tr>
<tr>
<td>8</td>
<td>CJORBOT, CJORSTI, CJORGAT, LOV $^1$, TOXOVO $^2$, DLQ, DWQ</td>
<td>$C_J$, $C_{ovlp}$ and $C_{gate_on}$ Ring oscillator frequency</td>
</tr>
</tbody>
</table>

---

1. LAP and LOV are correlated underdiffusion length parameters, which are uncorrelated to LVARO.
2. TOXO and TOXOVO are correlated oxide thickness parameters, which should have same variations.
## IFX Fast/Slow Corner Modeling Strategy: General Variation Scheme

<table>
<thead>
<tr>
<th>Correlated Parameters</th>
<th>fnfp (fast N/P)</th>
<th>snsp (slow N/P)</th>
<th>fnsp (skewed N/P)</th>
<th>snfp (skewed N/P)</th>
<th>Comments (for variations)</th>
</tr>
</thead>
<tbody>
<tr>
<td>channel length</td>
<td>↓↓</td>
<td>↑↑</td>
<td>↓↑*</td>
<td>↑↑*</td>
<td>poly length</td>
</tr>
<tr>
<td>channel width</td>
<td>↑↑</td>
<td>↓↓</td>
<td>↑↓*</td>
<td>↓↑*</td>
<td>S/D-diffusion width</td>
</tr>
<tr>
<td>oxide thickness</td>
<td>↓↓</td>
<td>↑↑</td>
<td>-</td>
<td>-</td>
<td>including overlap region</td>
</tr>
<tr>
<td><strong>Uncorrelated Parameters</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>effective doping</td>
<td>↓↓</td>
<td>↑↑</td>
<td>↓↑</td>
<td>↑↓</td>
<td>including halo doping</td>
</tr>
<tr>
<td>threshold voltage</td>
<td>↓↓</td>
<td>↑↑</td>
<td>↓↑</td>
<td>↑↓</td>
<td>$V_{th0}$ and $V_{tsat}$</td>
</tr>
<tr>
<td>DIBL effect / $V_{tlin}$</td>
<td>↑↑</td>
<td>↓↓</td>
<td>↑↓</td>
<td>↓↑</td>
<td>$DIBL =</td>
</tr>
<tr>
<td>low-field mobility</td>
<td>↑↑</td>
<td>↓↓</td>
<td>↑↓</td>
<td>↑↑</td>
<td>including $\mu_{eff}(L)$</td>
</tr>
<tr>
<td>series resistance</td>
<td>↓↓</td>
<td>↑↑</td>
<td>↓↑</td>
<td>↑↓</td>
<td>series resistance</td>
</tr>
<tr>
<td>leakage currents</td>
<td>↑↑</td>
<td>↓↓</td>
<td>↑↑</td>
<td>↓↑</td>
<td>$I_{sion}, I_{gater}, I_{GIDL}, I_{TAT}$</td>
</tr>
<tr>
<td>overlap capacitances</td>
<td>↑↑</td>
<td>↓↓</td>
<td>↑↓</td>
<td>↓↑</td>
<td>correlated by $TOX_{OV}, L_{OV}$</td>
</tr>
<tr>
<td>junction capacitances</td>
<td>↓↓</td>
<td>↑↑</td>
<td>↓↑</td>
<td>↑↓</td>
<td>junction capacitance</td>
</tr>
</tbody>
</table>

↑ means parameter is increased, ↓ means parameter is decreased; * means with reduced variations

1 dedicated MS (Mixed Signal) corner methodology
Example PSP Statistical Modeling:

- 65nm NFET/PFET short channel devices – FF/SS cases vs. Monte-Carlo (MC) (PSP102)
Improved Modeling Approach for Effective Doping (IFX Proposal for PSP103: from 3Q06 CMC Meeting)

- **PSP102**: Pocket doping **NPCK** and pocket length **LPCK** parameter have almost no influence on Vt-roll-up/off, only on body effect (unphysical). Threshold voltage will be mainly modeled by **DPHIB** parameters (offset voltage of $\Phi_B$).

- Proposal for **PSP103**: Pocket doping parameters **NPCK** and **LPCK** have an influence on Vt-roll-up/off and body effect as well (as they should be). **DPHIB** parameters can be used optional for Vt-adjustment.
PSP103: Proposal for modified geometrical scaling rule of effective doping

\[ N_{\text{sub0,eff}} = \text{NSUBO} \cdot \text{MAX} \left[ 1 + \text{NSUBW} \cdot \frac{W_E}{W_{\text{SEG}}} \cdot \ln \left( 1 + \frac{W_E}{W_{\text{SEG}}} \right), 10^{-3} \right] \]

\[ N_{\text{pck,eff}} = \text{NPCK} \cdot \text{MAX} \left[ 1 + \text{NPCKW} \cdot \frac{W_E}{W_{\text{SEG}}} \cdot \ln \left( 1 + \frac{W_E}{W_{\text{SEG}}} \right), 10^{-3} \right] \]

\[ L_{\text{pck,eff}} = \text{LPCK} \cdot \text{MAX} \left[ 1 + \text{LPCKW} \cdot \frac{W_E}{W_{\text{SEG}}} \cdot \ln \left( 1 + \frac{W_E}{W_{\text{SEG}}} \right), 10^{-3} \right] \]

\[ a = 7.5 \cdot 10^0 \]

\[ b = \sqrt{N_{\text{sub0,eff}}} + 0.5 \cdot \sqrt{N_{\text{pck,eff}}} - \sqrt{N_{\text{sub0,eff}}} \]

\[ \begin{align*}
N_{\text{sub0,eff}} + N_{\text{pck,eff}} \cdot \left[ 2 - \frac{L_E}{L_{\text{pck,eff}}} \right] & \quad \text{for } L_E < L_{\text{pck,eff}} \\
N_{\text{sub0,eff}} + N_{\text{pck,eff}} \cdot \frac{L_{\text{pck,eff}}}{L_E} & \quad \text{for } L_{\text{pck,eff}} \leq L_E \leq 2 \cdot L_{\text{pck,eff}} \\
\sqrt{N_{\text{sub0,eff}}} + a \cdot \ln \left( 1 + 2 \cdot \frac{L_{\text{pck,eff}}}{L_E} \cdot \left[ \exp \left( \frac{b}{a} \right) - 1 \right] \right)^2 & \quad \text{for } L_E > 2 \cdot L_{\text{pck,eff}}
\end{align*} \]

\[ \text{NEFF} = \frac{\text{NSUB} \left[ 1 - \text{FOL1} \cdot \frac{L_{\text{EN}}}{L_E} - \text{FOL2} \cdot \left( \frac{L_{\text{EN}}}{L_E} \right)^2 \right]}{1} \]

\[ ^1 \text{Introduction of one new local parameter NSUB} \]

(Note: In PSP102 \text{N}_{\text{sub}} is an internal variable)
Improved Modeling Approach for Effective Doping (cont’d)

PSP103: Proposal for modified internal model equation of $\Phi_B$ (for Vt-adjustment)

$$\Phi_B^{\text{eff}} = \text{MAX}\left(\text{DPHIB} + 2 \cdot \Phi_T \cdot \ln\left(\frac{\text{NSUB}}{n_i}\right), 0.05\right)$$

Without FOL1 and FOL2 !
(Note: PSP102 use ln(NEFF/ni) *)

PSP102/103: Internal model equation of $\gamma_0$ (for body-effect) remains unchanged

$$\gamma_0 = \sqrt{\frac{2 \cdot q \cdot \varepsilon_i \cdot \text{NEFF}}{C_{ox}}}$$

With FOL1 and FOL2, i.e. RSCE of body-effect

- PSP103 Proposal:
  $\Phi_B$- and $\gamma_0$-equation share the same global parameters NSUBO, NPCK and LPCK by the NSUB-scaling rule (since also part of the NEFF-scaling rule).
  Additional reverse short channel effect parameters FOL1 and FOL2 will have an influence just on body effect (and will not decrease the Vt as in PSP102 and therefore mustn’t be compensated by DPHIB parameters *).
  DPHIB parameters can be used optional for Vt-adjustment and fine-tuning.
PSP102.1 Runtime Performance:

Summary

- With PSP102.1 (with JUNCAP2-Express) we expect for most of our circuits about 30% longer (TR) simulation times than with BSIM4.3
- No convergence problems with our PSP102 C-code versions so far!
Table 1: Actual transient analysis results - Test circuits with overall CPU times for PSP102.1_JUNCAP2Express_testversion/BSIM4.3 (i.e. incl. parasitic C/R’s)

<table>
<thead>
<tr>
<th>Circuit</th>
<th># MOSFETs</th>
<th>Model</th>
<th># iterations (OP + TRAN)</th>
<th>CPU time overall</th>
<th>Ratio PSP/BSIM4 CPU time overall</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFX 65nm Flash A/D Converter</td>
<td>20679</td>
<td>BSIM4, PSP</td>
<td>40 + 47118 16 + 45052</td>
<td>13357</td>
<td>1.18</td>
</tr>
<tr>
<td>IFX 65nm ring oscillator INV</td>
<td>622</td>
<td>BSIM4, PSP</td>
<td>6 + 44299 6 + 42243</td>
<td>595</td>
<td>1.13</td>
</tr>
<tr>
<td>IFX 65nm SRAM arrays</td>
<td>59160</td>
<td>BSIM4, PSP</td>
<td>12 + 112 10 + 126</td>
<td>95</td>
<td>1.36</td>
</tr>
</tbody>
</table>

Table 2: Actual transient analysis results - Test circuits with MOSFET load CPU times per iterations for PSP102.1_JUNCAP2Express_testversion/BSIM4.3

<table>
<thead>
<tr>
<th>Circuit</th>
<th># FETs</th>
<th>Model</th>
<th># iterations (OP + TRAN)</th>
<th>CPU time MOS load</th>
<th>CPU time MOS load per iterat.</th>
<th>Ratio PSP/BSIM4 CPU MOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFX 65nm Flash A/D Converter</td>
<td>20679</td>
<td>BSIM4, PSP</td>
<td>40 + 47118 16 + 45052</td>
<td>9876</td>
<td>210.00 ms 308.00 ms</td>
<td>1.47</td>
</tr>
<tr>
<td>IFX 65nm ring oscillator INV</td>
<td>622</td>
<td>BSIM4, PSP</td>
<td>6 + 44299 6 + 42243</td>
<td>290</td>
<td>6.55 ms 9.18 ms</td>
<td>1.40</td>
</tr>
<tr>
<td>IFX 65nm SRAM arrays</td>
<td>59160</td>
<td>BSIM4, PSP</td>
<td>12 + 112 10 + 126</td>
<td>67</td>
<td>600.00 ms 865.00 ms</td>
<td>1.44</td>
</tr>
</tbody>
</table>
Outlook: Next PSP102.2 Release (September 2007)

- JUNCAP2 Express
  → gives further simulation speed improvement

- Well proximity effect
  → same as in BSIM4 (CMC standard WPE model)

- Multi-finger devices support
  → analogous to NF (& SD) in BSIM4

- Parasitic resistances (optional nodes)
  - Gate resistance
  - Bulk resistance

- EPSOX
  → dielectric constant parameter needed for metal gates

- DELVTO and FACTUO
  → beneficial for handling layout effects and device mismatch

- Lmin, Lmax, Wmin and Wmax
PSP102.2: Dielectric Constant as Parameter - needed for Metal Gates

- Decouple gate current and capacitance fittings
- Introduce new parameters $\text{EPSOX}$ in local, $\text{EPSOXO}$ in global and $\text{POEPSOX}$ in binning.
- No additional geometrical scaling or binning: $\text{EPSOX} = \text{EPSOXO}$, $\text{EPSOX} = \text{POEPSOX}$
Work-function difference $\Phi_{ms}$ due to metal gate is covered in PSP already, due to the flat-band voltage parameter $V_{FB}$, $VFBO$ (even with a non-silicon semiconductor $\Phi_s$).

$$V_{FB} = \Phi_{ms} - \frac{Q_o}{C_{OX}} = (\Phi_m - \Phi_s) - \frac{Q_o}{C_{OX}} = \left[ \Phi_m - \left( \chi + \frac{E_g}{2q} + \psi_B \right) \right] - \frac{Q_o}{C_{OX}}$$

Other device effects related to metal gates
- history effects ?
- ...
Potential SiGe-channel option for 32nm

- Should be no issue for flat-band voltage VFB
- Requires modification of mobility model, $E_g$, $n_i$, etc.

→ Has to be addressed at PSP team a.s.a.p.
Conclusion

- PSP provides accurate description of I-V and C-V characteristics over complete bias, temperature and geometry range (proven for C65/C45).
- PSP is a powerful new compact model for advanced CMOS technologies (like C65, C45, C32 and beyond).
- PSP is very suitable for statistical modeling and extrapolations due to its strong physical basis.
- Especially mixed signal/analog and RF will benefit from the PSP model (e.g. harmonic distortion)
- Digital/library design should benefit as well (because of better fitting of output characteristics, etc.)
- 1’st suggestion for an improved modeling approach of effective doping (halo formulation) for PSP103 has already made at the CMC meeting
- With PSP102.1 we expect for most of our circuits a slow down factor PSP/BSIM4 about 1.3 (with JUNCAP2-Express).
- Future PSP102.2, PSP103 versions are very promising for new material options like high-k/metal gates, SiGe-channel, etc.
Addendum: Runtime Performance Estimation

- Last column of tables 2 reflect the performance ratio of the models better than last column of tables 1. The reason is, that the share of CPU time spent in MOS evaluation compared to the overall CPU time varies with the type of the circuit (e.g.: no parasitics, many parasitics). We experienced for the majority of our circuits (simulated with BSIM4) a share of the MOS evaluation compared to the overall CPU time in the range of 2/3 to 3/4.

- From this and with the assumption that PSP102 is about 1.4-1.5 times slower in the pure MOS evaluation compared to BSIM4 (see table 2) and with the further assumption that we need the same number of iterations for BSIM4 and PSP102, we estimate that the overall CPU time ratio PSP/BSIM4 for most of our circuits will be in the range of \((2/3 \times 1.45 + 1/3)\) and \((3/4 \times 1.45 + 1/4)\).

- This means: With PSP102 we expect for most of our circuits a slow down factor PSP/BSIM4 between 1.3 to 1.34 (with Juncap2-Express).

  - Note: The SiMKit2.5 PSP102.1 implementation is still about 30% slower than our direct C-code implementation (Compiler dependent, investigations in progress at IFX/QI).
The **TOX** parameter in PSP is defined as the physical oxide thickness (QM-effect and poly depletion effect are separate).

All electrical quantities in PSP are based on a fixed dielectric constant for SiO₂ of 3.9 (i.e. absolute permittivity of oxide $\varepsilon_{ox} = \varepsilon_0 \cdot \varepsilon_{SiO2}$ is pinned to SiO₂ in the model).

In modern MOSFET devices medium-k dielectrics are common to reduce the gate leakage currents, at same drive capability (i.e. $C_{ox}$).

*E.g.*: A nitrided oxide with a physical thickness of $TOX_r = 2 nm$ is related to an $\varepsilon_r$ of 4.8.

Medium/high-k dielectric can be modeled as an “equivalent oxide” with thickness, adjusted for SiO₂ (3.9) → $TOX_{EOT}$:

$$TOX_{EOT} = \frac{\varepsilon_{SiO2}}{\varepsilon_r} \cdot TOX_r = \frac{3.9}{4.8} \cdot 2 nm = 1.625 nm$$

$TOX_{EOT}$ gives a correct scaling for charges/capacitances and current gain factor (i.e. set PSP TOX parameter to the calculated $TOX_{EOT}$ value: $C_{ox} = \varepsilon_{ox} / TOX$).

But $TOX_{EOT}$ gives a wrong scaling for gate tunneling currents, since above value is too low (for the tunneling distance) and have to be compensated with gate current parameter coefficients (unphysical). Gate currents have to scale always with the real physical oxide thickness (here $TOX_r$ of that oxinitride)!
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