

Modeling and Parameter Extraction Experiences with PSP: An Advanced Surface-Potential-Based MOSFET Compact Model for Circuit Simulation

Joachim Assenmacher
IFAG COM BTS TD DIF CM

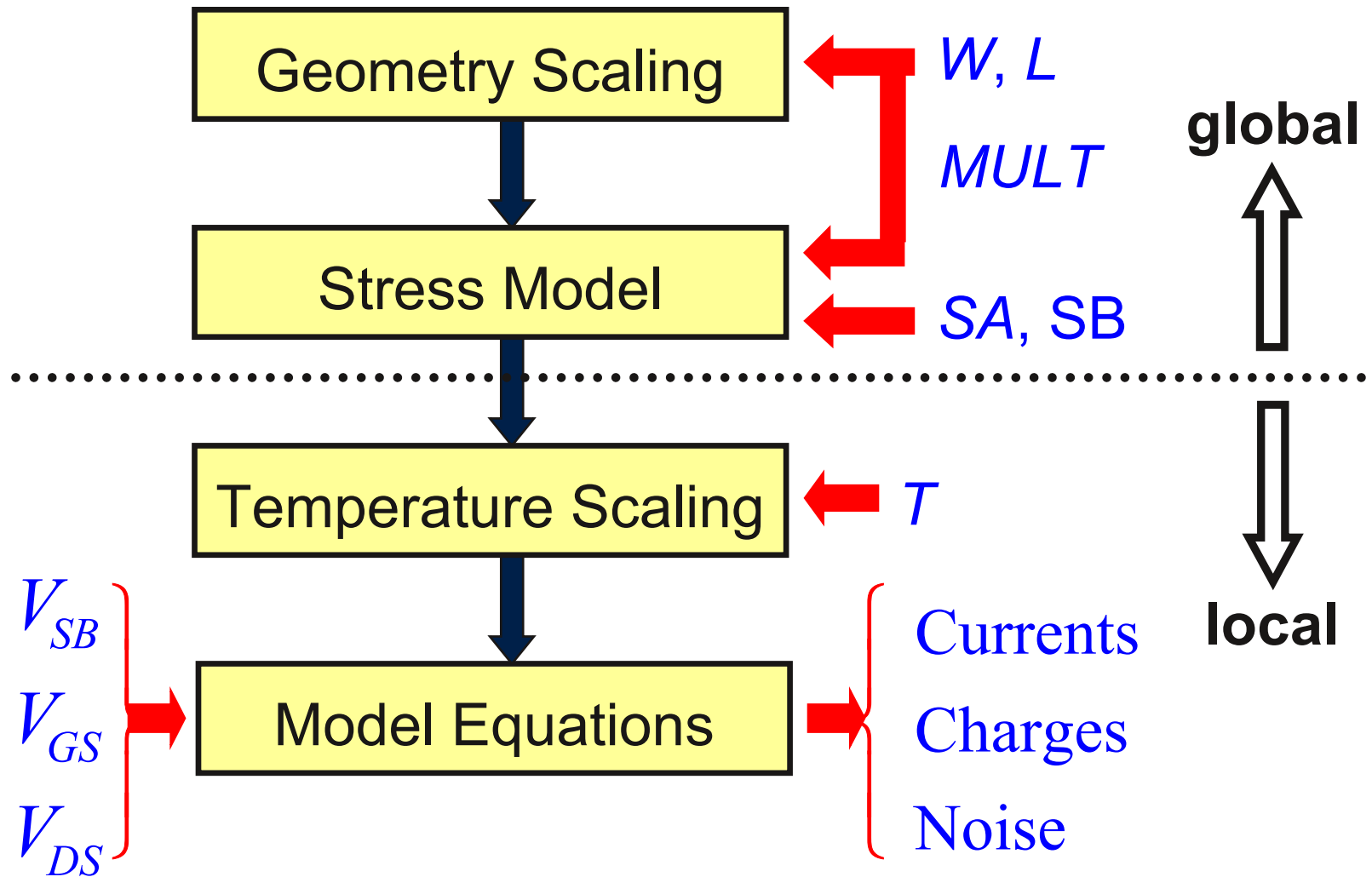
Outline

- Introduction
- PSP Parameter Extraction Strategy
- PSP Modeling Examples
- Statistical Modeling with PSP
 - Methodology of Corner Model Generation
 - Example and Verification
- PSP Runtimes
- Outlook
- Conclusion

Introduction: Basics of PSP

- PSP is the new the “Next Generation CMC Standard MOSFET Compact Model” (successor of BSIM4) for advanced digital, analog, mixed signal and RF circuit simulations.
- PSP is the merger of MOS Model 11 (Philips) and SP (PennState) - combines and enhances the advantages of MM11 and SP.
- PSP is a surface-potential-based model, which is physically the best know compact modeling approach (3’rd generation SPICE models).
- PSP use a Φ_S -approximation with very high accuracy (error < 1nV).
- Non-singular velocity-field relation enabling the modeling of RF harmonic distortions including intermodulation effects (IM3).
- The Φ_S -based PSP model has an accurate transition from weak to strong inversion (i.e. in moderate inversion, which is good for analog).
- PSP is symmetrical and continuous for all regions of device operation (passed all CMC benchmark tests, e.g. complete Gummel symmetry).
- Inclusion of all relevant small-geometry effects (like halo, stress, etc.).

Introduction: Structure of PSP



PSP: Parameter Extraction Strategy

I-V and C-V measurements

→ For required DC and CV measurements refer to the PSP manual at Section 7.1

global AC parameters (optional)

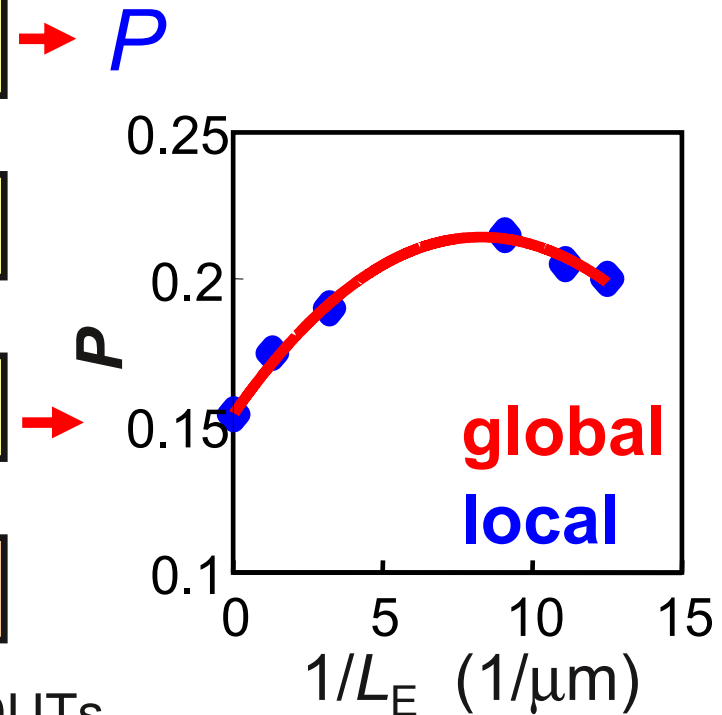
local parameters for each DUT → P

temperature scaling parameters

geometry scaling parameters → P

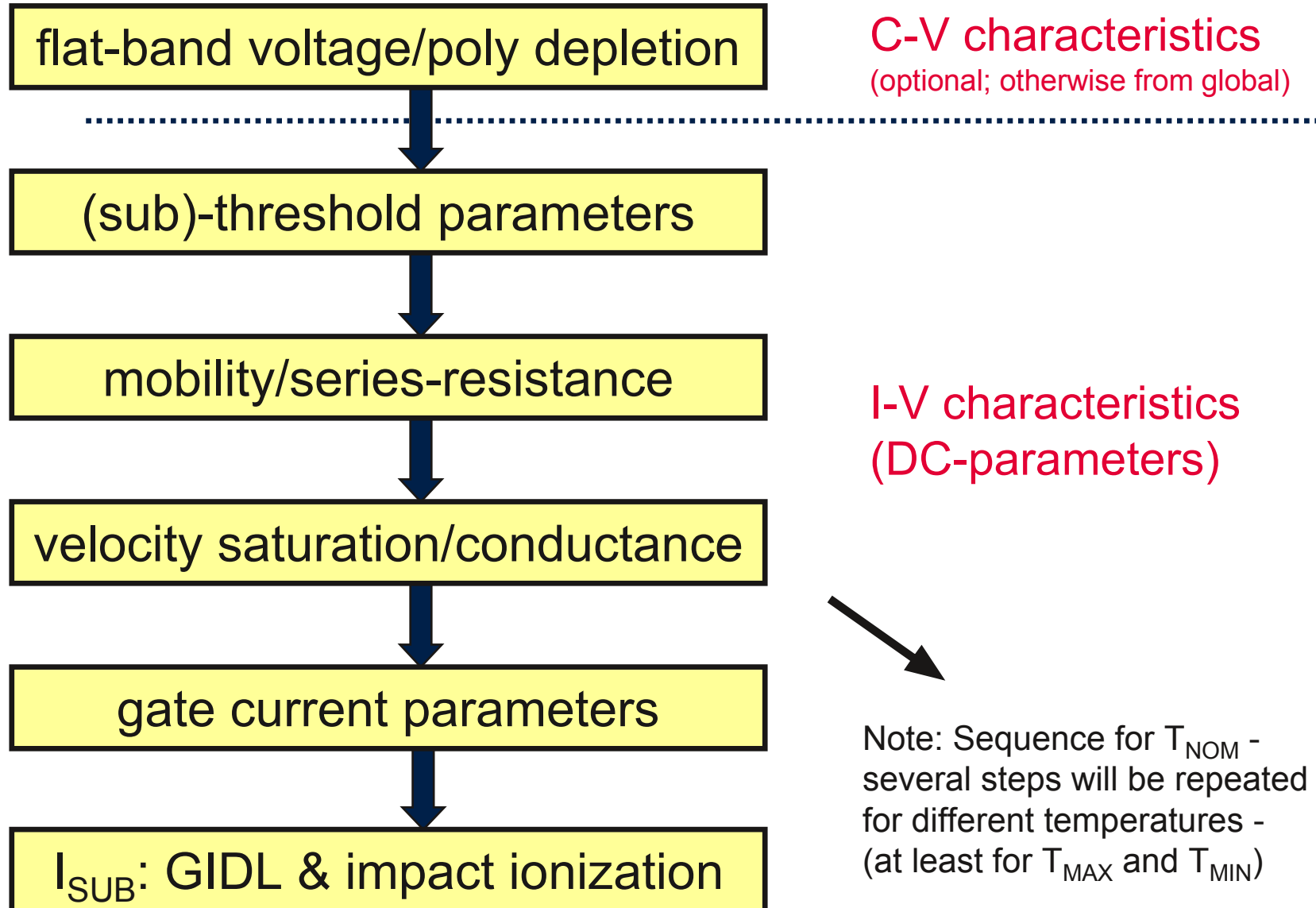
final global parameter set *

* fine-tuned by optimization on multiple DUTs

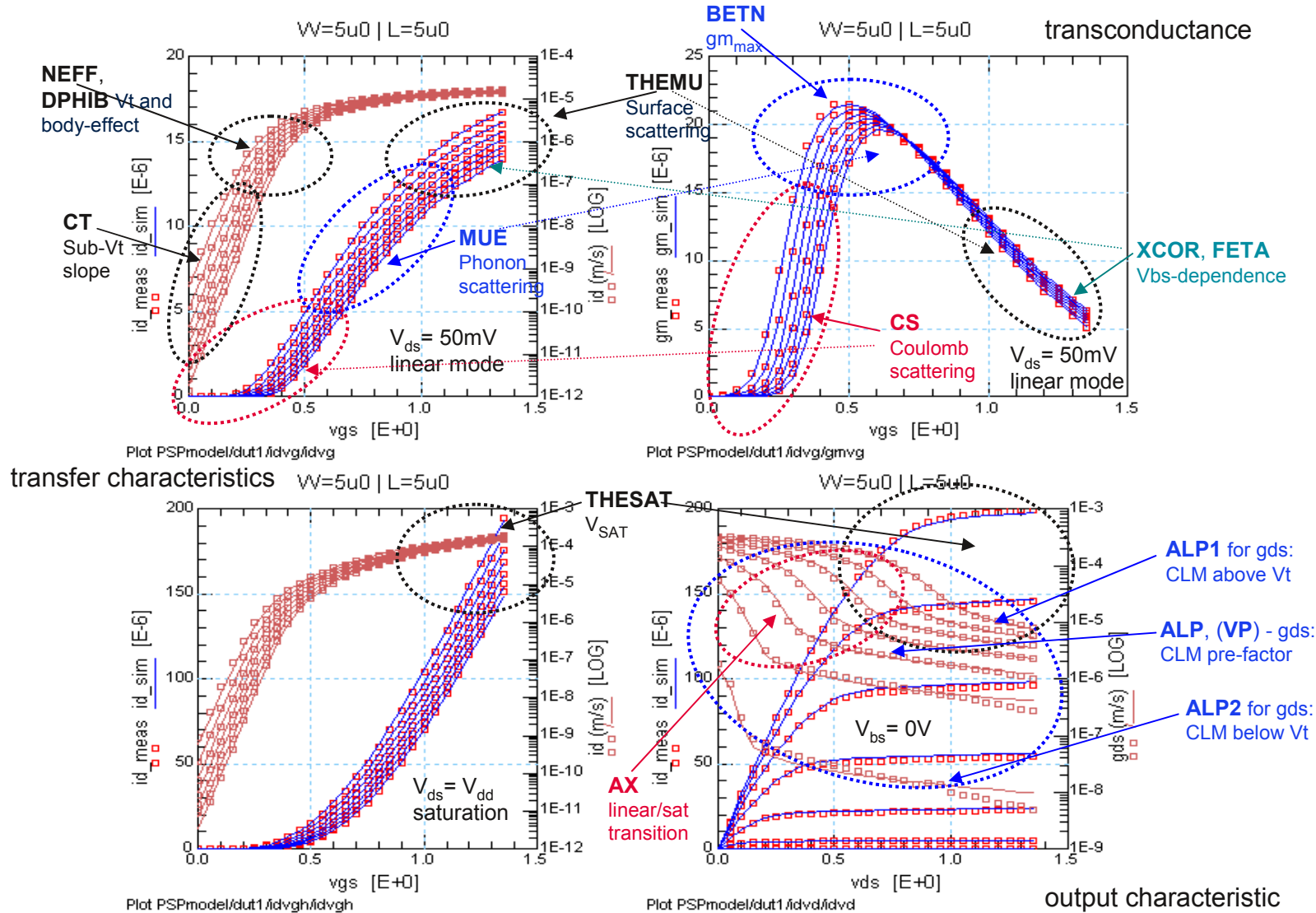


PSP: Extraction of Local Parameters

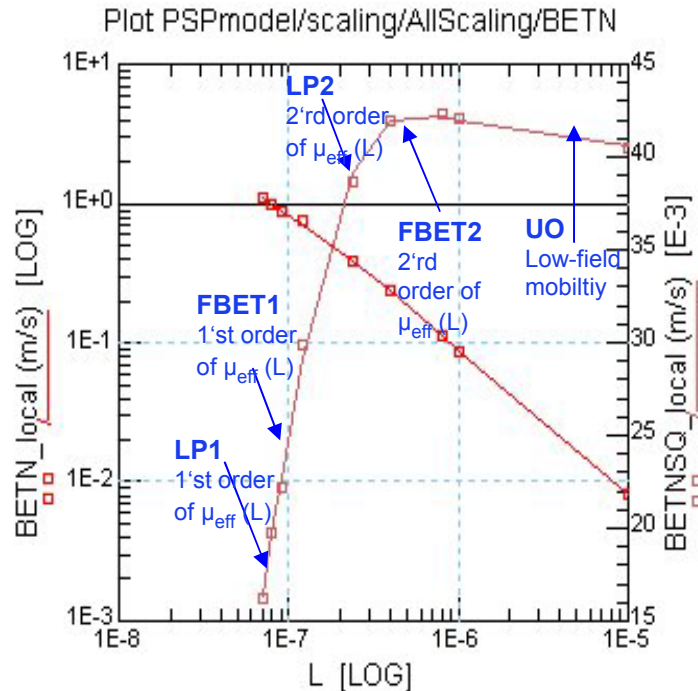
Optimization Flow



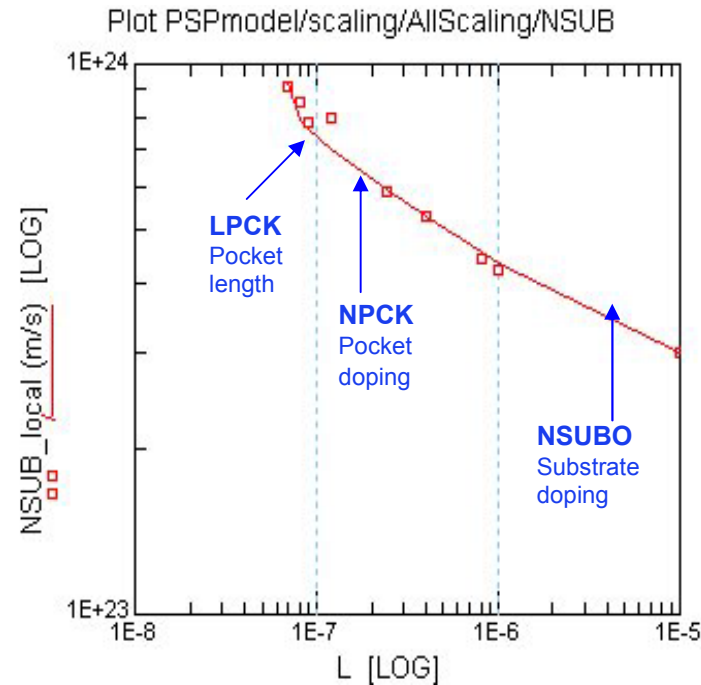
PSP102: Extraction of Local DC-Parameters Optimization Examples for a Wide Long Device



PSP: Extraction of Global Scaling Parameters Methodology



Effective mobility vs. channel length



Effective doping vs. channel length

Extraction of geometry-dependent parameters, e.g. for the calculation of effective mobility and doping, using physical geometrical scaling rules and some semi-empirical geometrical scaling rules (no binning).

Hint: Keep BETN and NSUB length scaling parameters fixed, as determined above, during optimization (fine-tuning) of the single device characteristics (as a physical basis for statistical model generation like fast/slow corners and MC models)!

PSP102: Extraction of Global Scaling Parameters (1/11)



Process Parameters

Local Global
↓ ↓

$$VFB = VFBO \cdot \left(1 + VFBL \cdot \frac{LEN}{LE}\right) \cdot \left(1 + VFBW \cdot \frac{WEN}{WE}\right) \cdot \left(1 + VFBLW \cdot \frac{WEN \cdot LEN}{WE \cdot LE}\right)$$

$$STVFB = STVFBO \cdot \left(1 + STVFBL \cdot \frac{LEN}{LE}\right) \cdot \left(1 + STVFBW \cdot \frac{WEN}{WE}\right) \cdot \left(1 + STVFBLW \cdot \frac{WEN \cdot LEN}{WE \cdot LE}\right)$$

$$DPHIB = \left(DPHIBO + DPHIBL \cdot \left[\frac{LEN}{LE} \right]^{DPHIBLEXP} \right) \cdot \left(1 + DPHIBW \cdot \frac{WEN}{WE}\right) \cdot \left(1 + DPHIBLW \cdot \frac{WEN \cdot LEN}{WE \cdot LE}\right)$$

- ³ global parameter extraction for devices of **length-array at wide channel widths**
- ⁴ global parameter extraction for devices of **width-array at long channel lengths**
- ⁵ global parameter extraction for devices of **length-array at narrow channel widths**
- ⁶ global parameter extraction for devices of **width-array at short channel length**

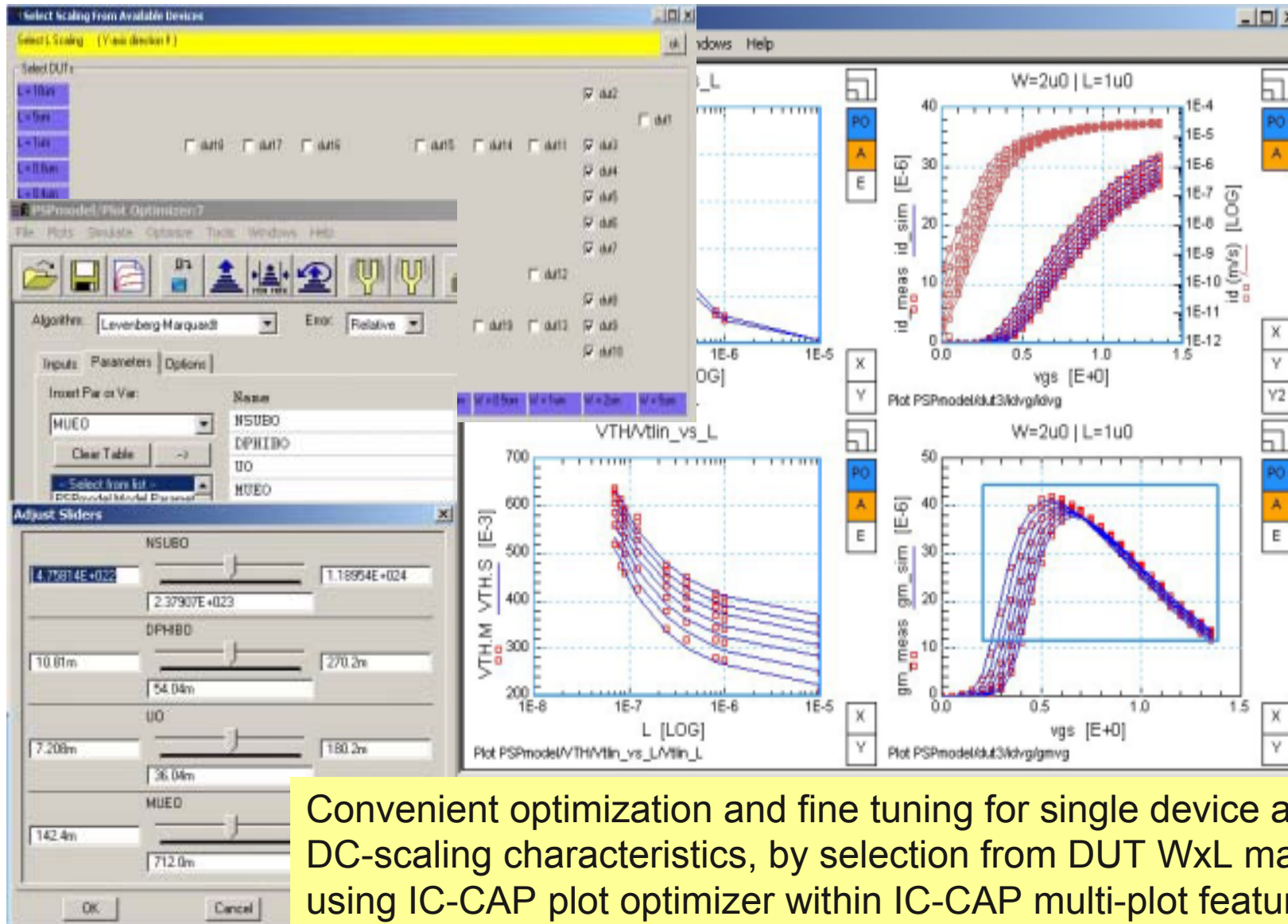
PSP102: Optimization of Global Parameters (1/4)



Table 7: Global DC-parameter extraction fine-tuning procedure at nominal temperature (T_{NOM})

Step	DUT	Optimized Parameters	Fitting Target	Comments
1	LC	NSUBO, DPHIBO, (VFBO²), CTO, (DNSUB, VNSUB, NSLP)⁴	log Id-Vg(Vb) at $V_{ds_{in}}$	Vth0, body effect and sub-Vt slope (bias-dependent body factor of N_{eff})
2	LC	IGINVLW, GC2O¹, GC3O¹, (CHIBO⁶)	Ig-Vg(Vd) for $V_{gs} > 0V$	Gate current in inversion
3	LC	GCOO¹	Ig-Vg for $V_{gs} < 0V$	Gate current in accumulation
4	LC	UO, MUEO, THEMUO¹, CSO, FETAO³, XCORO	Id-Vg(Vb), gm at $V_{ds_{in}}$	Low-field mobility and mobility degradation/scattering parameters
5	LC	A1O, A2O¹, A3O, A4O	Ib-Vg(Vd) for $V_{gs} > 0V$	Impact ionization parameters
6	LC	AGIDLW, BGIDLO¹, CGIDLO¹	log Id-Vg(Vb) for $V_{gs} < 0V$	GIDL parameters in saturation
7	LC	STATGAT, (MEFFTATGAT ²)	log Id-Vg(Vb) for $V_{gs} \sim 0V$	TAT parameters in saturation
8	LC	THESATO	Id-Vd(Vg) at $V_{bs} = 0V$	Velocity saturation parameter
9	LC	ALPL, ALP1L1, ALP2L1, VPO ¹ , (AXO ⁵)	log gds at $V_{bs} = 0V$	CLM and saturation voltage parameters (lin/sat transition)
10	LA	NPCK, LPCK, FOL1, FOL2, (VFBL ²), DPHIBL, DPHIBLEXP, CTL, CTLEXP	log Id-Vg(Vb) at $V_{ds_{in}}$	Body effect and Vt-roll-up/off and sub-Vt slope
11	LA	IGOVW	Ig-Vg(Vd) for $V_{gs} \sim 0V$	Gate overlap current
12	LA	FBET1, LP1, FBET2, LP2, CSL, CSLEXP, XCORL, RSW1	Id-Vg(Vb), gm at $V_{ds_{in}}$	Mobility degradation/scattering and series resistance parameters
13	LA	CFL, CFLEXP, CFBO	log Id-Vg(Vb) at $V_{ds_{sat}}$	DIBL effect on $V_{t_{sat}}$ (check gds too)

The IFX IC-CAP Modeling Tool for PSP: User Interface - Fine-Tuning of Global Parameters

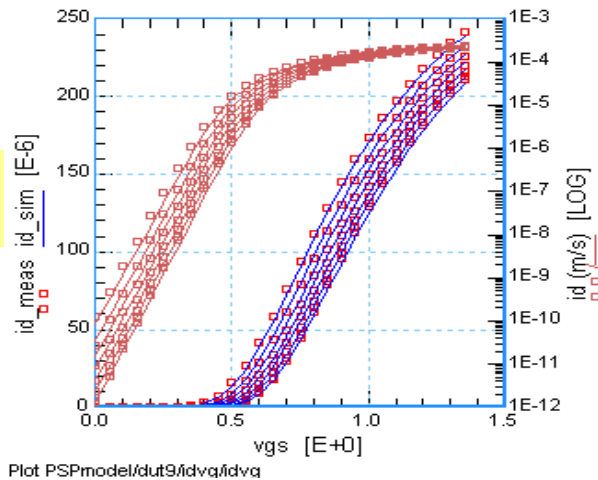


Convenient optimization and fine tuning for single device and DC-scaling characteristics, by selection from DUT WxL matrix, using IC-CAP plot optimizer within IC-CAP multi-plot feature.

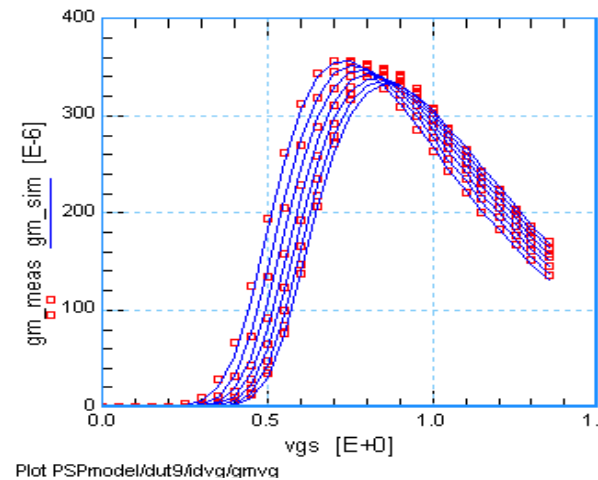
Example PSP Modeling: Id-Vg and Id-Vd

- 65nm NFET short channel characteristics - accurate DC model build (PSP102)

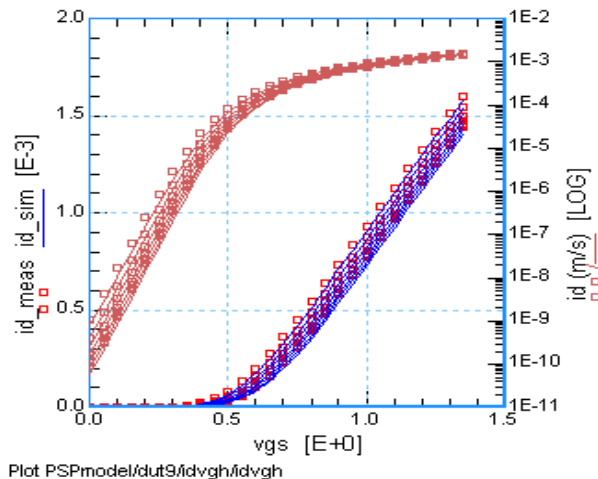
IdVg @ $V_{ds}=50mV$
transfer characteristic



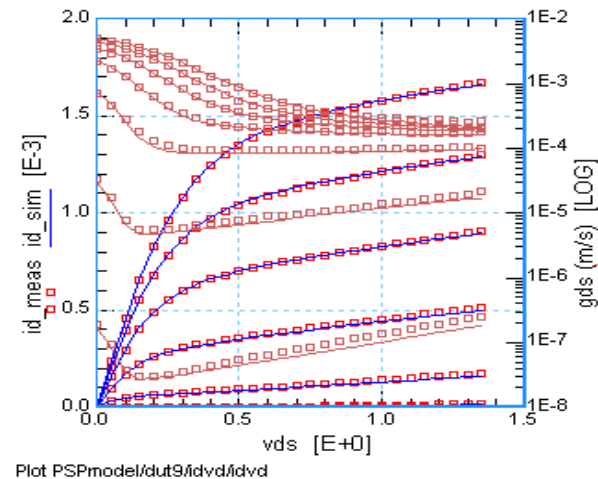
gm @ $V_{ds}=50mV$
transconductance



IdVg @ $V_{dd}=1.2V$
transfer characteristic



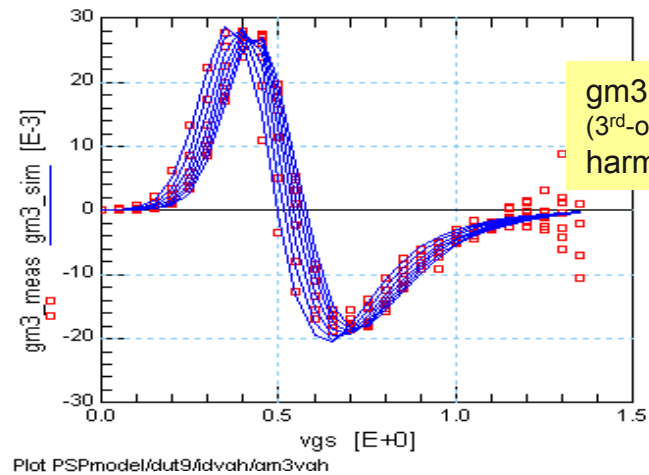
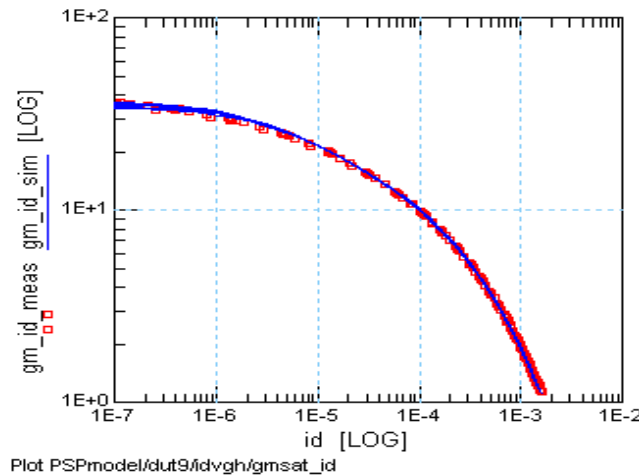
IdVd @ $V_{bs}=0V$
output characteristic



Example PSP Modeling: Analog Figures

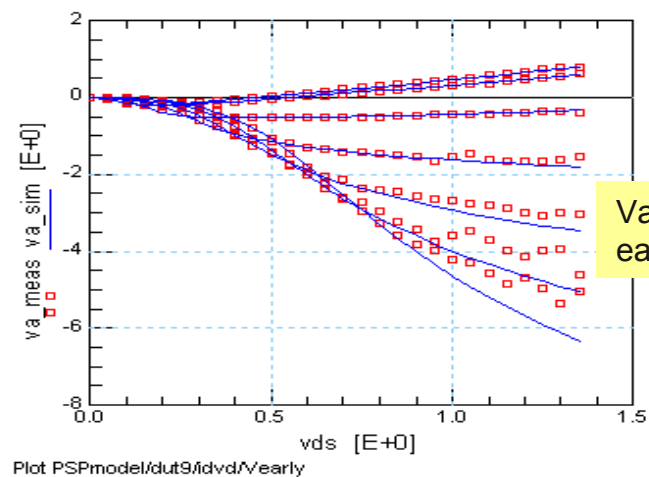
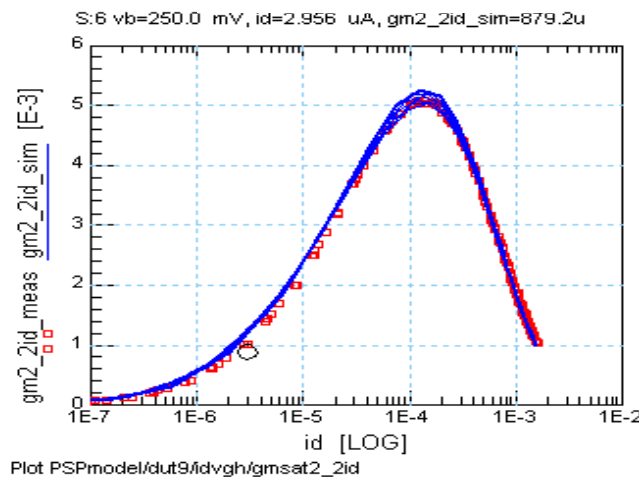
- 65nm NFET short channel characteristics - accurate analog model build (PSP102)

$g_{m_{sat}}/I_{d_{sat}}$



$g_{m3} = d^3I_d/dV_{gs}^3$
(3rd-order derivative)
harmonic distortion

$K' := g_{m_{sat}}^2 / (2 \cdot I_{d_{sat}})$
analog gain factor



$V_a = -(I_d/g_{ds} - V_d)$
early voltage

PSP Corner Model Generation Flow

Statistical Modeling



Step	Varied Parameters	Target (Spec. limits)
1	TOXO, VFBO, NSUBO, (DPHIBO)	wide/long V_{tlin} , (I_{dlin} , I_{gate})
3	UO	wide/long I_{dlin} , g_{m_max}
4	LVARO, LAP¹, VFBL, (DPHIBL), CFL, NPCK, LPCK	wide/short V_{tsat} , V_{tlin} , I_{dsat} , body effect
6	RSW1, (THESATL)	wide/short I_{dlin} , I_{dsat}
7	WVARO, VFBLW, (DPHIBLW)	narrow/short I_{dsat} , V_{tsat}
8	CJORBOT, CJORSTI, CJORGAT, LOV¹, TOXOVO², DLQ, DWQ	C_J , C_{ovlp} and C_{gate_on} Ring oscillator frequency

¹ LAP and LOV are correlated underdiffusion length parameters, which are uncorrelated to LVARO.

² TOXO and TOXOVO are correlated oxide thickness parameters, which should have same variations.

IFX Fast/Slow Corner Modeling Strategy: General Variation Scheme



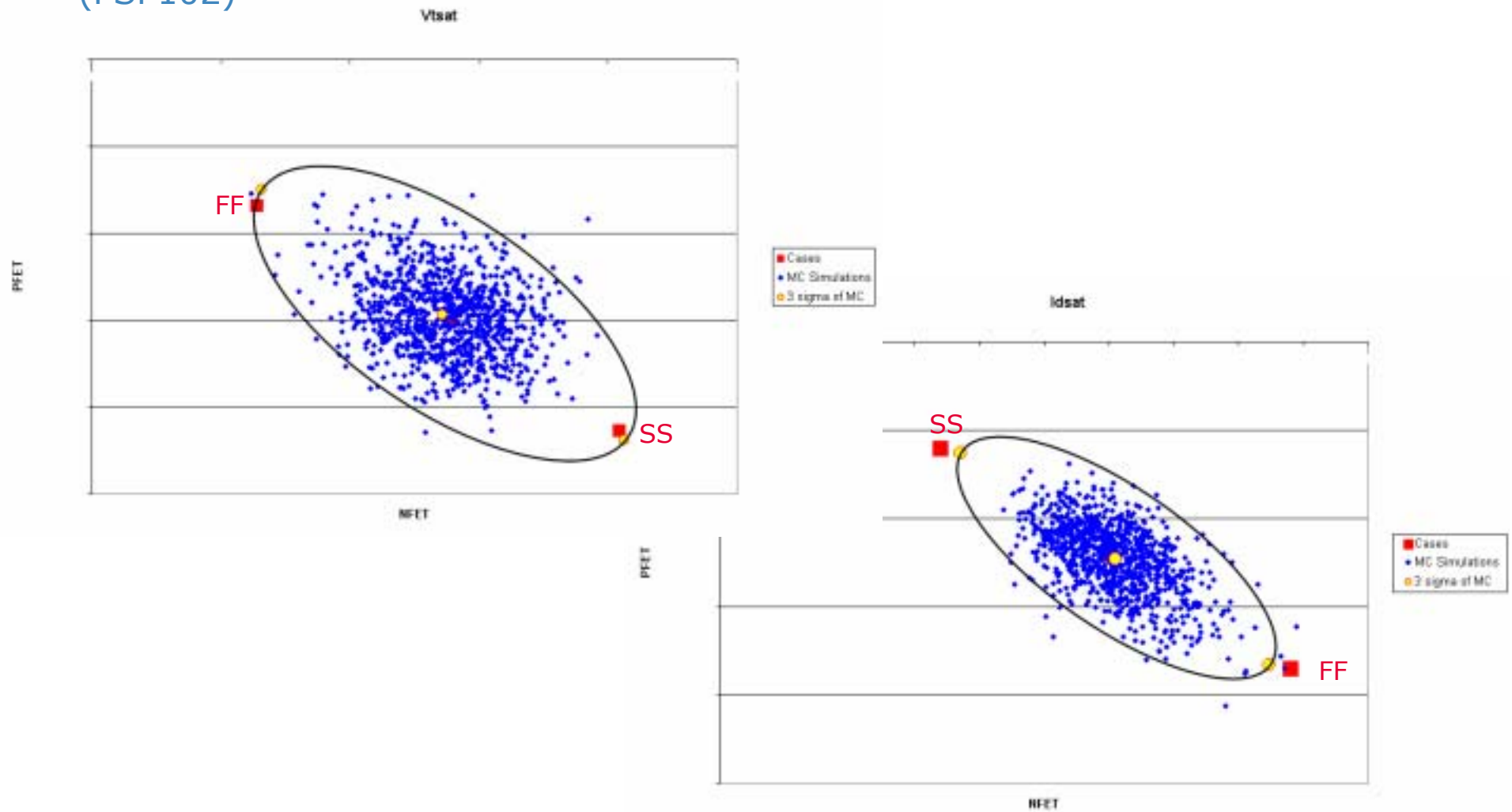
Correlated Parameters	fnfp (fast N/P)	snsf (slow N/P)	fnsp (skewed N/P)	snfp (skewed N/P)	Comments (for variations)
channel length	↓ ↓	↑ ↑	↓ ↑ *	↑ ↓ *	poly length
channel width	↑ ↑	↓ ↓	↑ ↓ *	↓ ↑ *	S/D-diffusion width
oxide thickness	↓ ↓	↑ ↑	-	-	including overlap region
Uncorrelated Parameters					
effective doping	↓ ↓	↑ ↑	↓ ↑	↑ ↓	including halo doping
threshold voltage	↓ ↓	↑ ↑	↓ ↑	↑ ↓	V_{th0} and V_{tsat}
DIBL effect / V_{tlin}	↑ ↑	↓ ↓	↑ ↓	↓ ↑	$DIBL = V_{tlin} - V_{tsat} $
low-field mobility	↑ ↑	↓ ↓	↑ ↓	↓ ↑	including $\mu_{eff}(L)$
series resistance	↓ ↓	↑ ↑	↓ ↑	↑ ↓	series resistance
leakage currents	↑ ↑	↓ ↓	↑ ↓	↓ ↑	I_{soff} , I_{gate} , I_{GIDL} , I_{TAT}
overlap capacitances	↑ ↑ ¹	↓ ↓	↑ ↓	↓ ↑	correlated by TOX_{OV} , L_{OV}
junction capacitances	↓ ↓	↑ ↑	↓ ↑	↑ ↓	junction capacitance

↑ means parameter is increased, ↓ means parameter is decreased; * means with reduced variations

¹ dedicated MS (Mixed Signal) corner methodology

Example PSP Statistical Modeling:

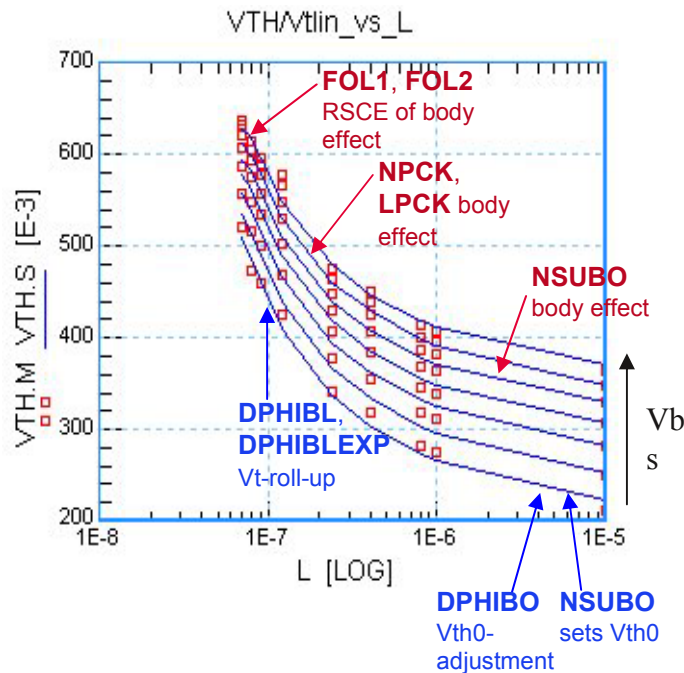
- 65nm NFET/PFET short channel devices – FF/SS cases vs. Monte-Carlo (MC) (PSP102)



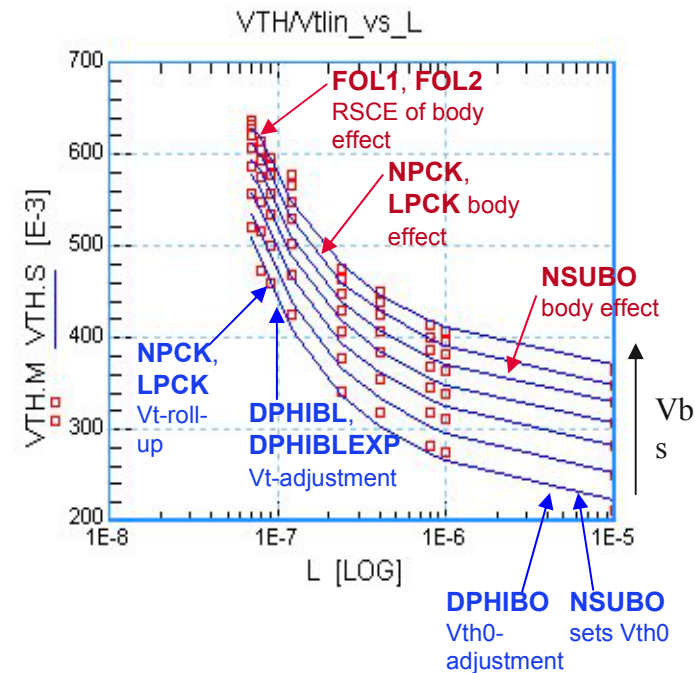
Improved Modeling Approach for Effective Doping (IFX Proposal for PSP103: from 3Q06 CMC Meeting)



PSP102: Actual situation



PSP103: Proposal



- PSP102: Pocket doping **NPCK** and pocket length **LPCK** parameter have almost no influence on Vt-roll-up/off, only on body effect (unphysical). Threshold voltage will be mainly modeled by **DPHIB** parameters (offset voltage of Φ_B).
- Proposal for PSP103: Pocket doping parameters **NPCK** and **LPCK** have an influence on Vt-roll-up/off and body effect as well (as they should be). **DPHIB** parameters can be used optional for Vt-adjustment.

Improved Modeling Approach for Effective Doping (cont'd)



PSP103: Proposal for modified geometrical scaling rule of effective doping

$$N_{sub0, eff} = \text{NSUBO} \cdot \text{MAX} \left(\left[1 + \text{NSUBW} \cdot \frac{W_{EN}}{W_E} \cdot \ln \left(1 + \frac{W_E}{\text{WSEG}} \right) \right], 10^{-3} \right)$$

$$N_{pck, eff} = \text{NPCK} \cdot \text{MAX} \left(\left[1 + \text{NPCKW} \cdot \frac{W_{EN}}{W_E} \cdot \ln \left(1 + \frac{W_E}{\text{WSEGP}} \right) \right], 10^{-3} \right)$$

$$L_{pck, eff} = \text{LPCK} \cdot \text{MAX} \left(\left[1 + \text{LPCKW} \cdot \frac{W_{EN}}{W_E} \cdot \ln \left(1 + \frac{W_E}{\text{WSEGP}} \right) \right], 10^{-3} \right)$$

$$a = 7.5 \cdot 10^{10}$$

$$b = \sqrt{N_{sub0, eff} + 0.5 \cdot N_{pck, eff}} - \sqrt{N_{sub0, eff}}$$

$$\text{NSUB} = \begin{cases} N_{sub0, eff} + N_{pck, eff} \cdot \left[2 - \frac{L_E}{L_{pck, eff}} \right] & \text{for } L_E < L_{pck, eff} \\ N_{sub0, eff} + N_{pck, eff} \cdot \frac{L_{pck, eff}}{L_E} & \text{for } L_{pck, eff} \leq L_E \leq 2 \cdot L_{pck, eff} \\ \left[\sqrt{N_{sub0, eff}} + a \cdot \ln \left(1 + 2 \cdot \frac{L_{pck, eff}}{L_E} \cdot \left[\exp \left(\frac{b}{a} \right) - 1 \right] \right) \right]^2 & \text{for } L_E > 2 \cdot L_{pck, eff} \end{cases}$$

$$\text{NEFF} = \text{NSUB} \cdot \left(1 - \text{FOL1} \cdot \frac{L_{EN}}{L_E} - \text{FOL2} \cdot \left[\frac{L_{EN}}{L_E} \right]^2 \right)$$

¹ Introduction of one new local parameter **NSUB**
(Note: In PSP102 N_{sub} is an internal variable)

Improved Modeling Approach for Effective Doping (cont'd)



PSP103: Proposal for modified internal model equation of Φ_B (for V_t -adjustment)

$$\Phi_B^{cl} = \text{MAX} \left(\text{DPHIB} + 2 \cdot \Phi_T \cdot \ln \left[\frac{\text{NSUB}}{n_i} \right], 0.05 \right)$$

Without **FOL1** and **FOL2** !
(Note: PSP102 use $\ln(\text{NEFF}/n_i)$ *)

PSP102/103: Internal model equation of γ_0 (for body-effect) remains unchanged

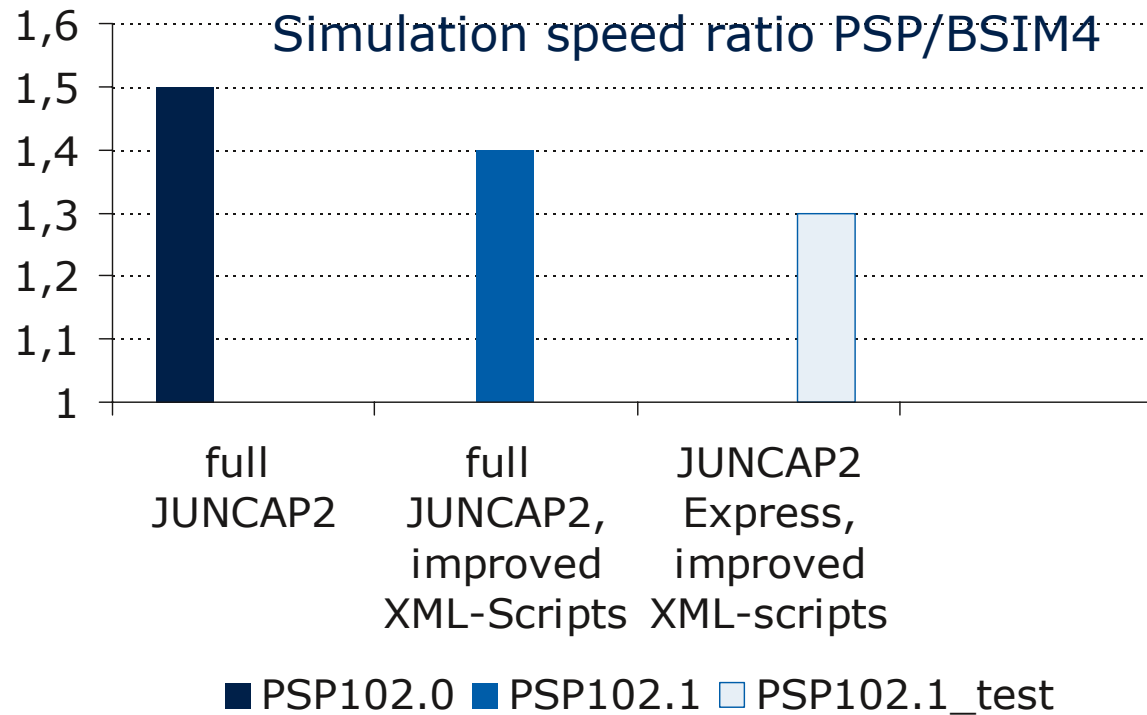
$$\gamma_0 = \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot \text{NEFF}}}{C_{ox}}$$

With **FOL1** and **FOL2**, i.e. RSCE of body-effect

- **PSP103 Proposal:**

Φ_B - and γ_0 -equation share the same global parameters **NSUBO**, **NPCK** and **LPCK** by the **NSUB**-scaling rule (since also part of the **NEFF**-scaling rule). Additional reverse short channel effect parameters **FOL1** and **FOL2** will have an influence just on body effect (and will not decrease the V_t as in PSP102 and therefore mustn't be compensated by DPHIB parameters *). **DPHIB** parameters can be used optional for V_t -adjustment and fine-tuning.

PSP102.1 Runtime Performance: Summary



- With PSP102.1 (with JUNCAP2-Express) we expect for most of our circuits about 30% longer (TR) simulation times than with BSIM4.3
- No convergence problems with our PSP102 C-code versions so far!

Runtime Performance Evaluation of PSP102

with IFX/QI in-house simulator (direct C-code implementation)



- Table 1: Actual transient analysis results - Test circuits with overall CPU times for PSP102.1_JUNCAP2Express_testversion/BSIM4.3 (i.e. incl. parasitic C/R's)

Circuit	# MOSFETs	Model	# iterations (OP + TRAN)	CPU time overall	Ratio PSP/BSIM4 CPU time overall
IFX 65nm Flash A/D Converter	20679	BSIM4 PSP	40 + 47118 16 + 45052	13357 15799	1.18
IFX 65nm ring oscillator INV	622	BSIM4 PSP	6 + 44299 6 + 42243	595 670	1.13
IFX 65nm SRAM arrays	59160	BSIM4 PSP	12 + 112 10 + 126	95 129	1.36

- Table 2: Actual transient analysis results - Test circuits with MOSFET load CPU times per iterations for PSP102.1_JUNCAP2Express_testversion/BSIM4.3

Circuit	# FETs	Model	# iterations (OP + TRAN)	CPU time MOS load	CPU time MOS load per iterat.	Ratio PSP/BSIM4 CPU MOS
IFX 65nm Flash A/D Converter	20679	BSIM4 PSP	40 + 47118 16 + 45052	9876 13877	210.00 ms 308.00 ms	1.47
IFX 65nm ring oscillator INV	622	BSIM4 PSP	6 + 44299 6 + 42243	290 388	6.55 ms 9.18 ms	1.40
IFX 65nm SRAM arrays	59160	BSIM4 PSP	12 + 112 10 + 126	67 109	600.00 ms 865.00 ms	1.44

Outlook: Next PSP102.2 Release (September 2007)



- JUNCAP2 Express
 - gives further simulation speed improvement
- Well proximity effect
 - same as in BSIM4 (CMC standard WPE model)
- Multi-finger devices support
 - analogous to NF (& SD) in BSIM4
- Parasitic resistances (optional nodes)
 - Gate resistance
 - Bulk resistance
- EPSOX
 - dielectric constant parameter needed for metal gates
- DELVTO and FACTUO
 - beneficial for handling layout effects and device mismatch
- Lmin, Lmax, Wmin and Wmax

PSP102.2: Dielectric Constant as Parameter - needed for Metal Gates



- Decouple gate current and capacitance fittings
- Introduce new parameters **EPSOX** in local, **EPSOXO** in global and **POEPSOX** in binning.
- No additional geometrical scaling or binning:
 $EPSOX = \mathbf{EPSOXO}$, $EPSOX = \mathbf{POEPSOX}$

- Work-function difference Φ_{ms} due to metal gate is covered in PSP already, due to the flat-band voltage parameter **VFB**, **VFBO** (even with a non-silicon semiconductor Φ_s).

$$VFB = \Phi_{ms} - \frac{Q_o}{C_{OX}} = (\Phi_m - \Phi_s) - \frac{Q_o}{C_{OX}} = \left[\Phi_m - \left(\chi + \frac{E_g}{2q} + \psi_B \right) \right] - \frac{Q_o}{C_{OX}}$$

- Other device effects related to metal gates
 - history effects ?
 - ...

Future PSP103 Release (spring 2008 ?) - Non-Silicon Channel Modeling



- Potential SiGe-channel option for 32nm
 - Should be no issue for flat-band voltage VFB
 - Requires modification of mobility model, E_g , n_i , etc. ?
 - Has to be addressed at PSP team a.s.a.p.

Conclusion

- PSP provides accurate description of I-V and C-V characteristics over complete bias, temperature and geometry range (proven for C65/C45).
- PSP is a powerful new compact model for advanced CMOS technologies (like C65, C45, C32 and beyond).
- PSP is very suitable for statistical modeling and extrapolations due to its strong physical basis.
- Especially mixed signal/analog and RF will benefit from the PSP model (e.g. harmonic distortion)
- Digital/library design should benefit as well (because of better fitting of output characteristics, etc.)
- 1st suggestion for an improved modeling approach of effective doping (halo formulation) for PSP103 has already made at the CMC meeting
- With PSP102.1 we expect for most of our circuits a slow down factor PSP/BSIM4 about 1.3 (with JUNCAP2-Express).
- Future PSP102.2, PSP103 versions are very promising for new material options like high-k/metal gates, SiGe-channel, etc.

Addendum: Runtime Performance Estimation

- Last column of tables 2 reflect the performance ratio of the models better than last column of tables 1. The reason is, that the share of CPU time spent in MOS evaluation compared to the overall CPU time varies with the type of the circuit (e.g.: no parasitics, many parasitics). We experienced for the majority of our circuits (simulated with BSIM4) a share of the MOS evaluation compared to the overall CPU time in the range of 2/3 to 3/4.
- From this and with the assumption that PSP102 is about 1.4-1.5 times slower in the pure MOS evaluation compared to BSIM4 (see table 2) and with the further assumption that we need the same number of iterations for BSIM4 and PSP102, we estimate that the overall CPU time ratio PSP/BSIM4 for most of our circuits will be in the range of $(2/3 \times 1.45 + 1/3)$ and $(3/4 \times 1.45 + 1/4)$.
- This means: With PSP102 we expect for most of our circuits a slow down factor PSP/BSIM4 between 1.3 to 1.34 (with Juncap2-Express).
 - Note: The SiMKit2.5 PSP102.1 implementation is still about 30% slower than our direct C-code implementation (Compiler dependent, investigations in progress at IFX/QI).

Backup: IFX Proposal for PSP102 Model Improvement at 3Q06 CMC Meeting - Introduction of a Dielectric Constant Parameter in PSP102.2/103



- The **TOX** parameter in PSP is defined as the physical oxide thickness (QM-effect and poly depletion effect are separate).
- All electrical quantities in PSP are based on a fixed dielectric constant for SiO₂ of 3.9 (i.e. absolute permittivity of oxide $\epsilon_{ox} = \epsilon_0 \cdot \epsilon_{SiO_2}$ is pinned to SiO₂ in the model).
- In modern MOSFET devices medium-k dielectrics are common to reduce the gate leakage currents, at same drive capability (i.e. C_{ox}).
E.g.: A nitrided oxide with a physical thickness of $TOX_r = 2nm$ is related to an ϵ_r of 4.8.
- Medium/high-k dielectric can be modeled as an "equivalent oxide" with thickness, adjusted for SiO₂ (3.9) → TOX_{EOT} :

$$TOX_{EOT} = \frac{\epsilon_{SiO_2}}{\epsilon_r} \cdot TOX_r = \frac{3.9}{4.8} \cdot 2nm = 1.625 nm$$

- TOX_{EOT} gives a correct scaling for charges/capacitances and current gain factor (i.e. set PSP **TOX** parameter to the calculated TOX_{EOT} value: $C_{ox} = \epsilon_{ox} / \mathbf{TOX}$).
- But TOX_{EOT} gives a wrong scaling for gate tunneling currents, since above value is too low (for the tunneling distance) and have to be compensated with gate current parameter coefficients (unphysical). Gate currents have to scale always with the real physical oxide thickness (here TOX_r of that oxinitride)!

A person wearing a white lab coat, a white face mask, and safety glasses is working in a laboratory. They are holding a piece of equipment, possibly a pipette or a small container, and appear to be focused on their task. The background is slightly blurred, showing laboratory equipment and shelves.

We commit.

We innovate.

We partner.

We create value.



Never stop thinking