Accuracy and Speed Performance of HiSIM Versions 231 and 240

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Outline

● Overview of Compact-Modeling Approaches
  ● Accuracy Aspects of HiSIM2.3.1 and 2.4.0
  ● Speed Versus Accuracy Trade-Off and Position of Leading Compact Models
● Conclusion
Basic Compact Model Approaches for the MOSFET

Threshold-Voltage-Based Models (e.g. BSIM3, BSIM4)

- currents expressed as functions of applied voltages
- different equations for:
  - sub-threshold region
  - linear region
  - saturation region

\[
I_{ds} = \mu C_{ox} \frac{W}{L} \left\{ (V_{gs} - V_{th}) V_{ds} - \left( \frac{1}{2} + \frac{\sqrt{2\epsilon Si q N_{sub}}}{4C_{ox} \sqrt{2\Phi_B}} \right) V_{ds}^2 \right\}
\]

New Generation of Surface-Potential-Based Models

- implicit equation for surface potential
- currents determined from drift and diffusion term of current density equation
- developed calculation methods for the surface potential:
  - iterative solution with the exact surface-potential equation \(\Rightarrow\) HiSIM
  - approximate explicit solution by 1\textsuperscript{st} & 2\textsuperscript{nd} order perturbation theory, after prior conditioning of the surface-potential equation \(\Rightarrow\) PSP

New Generation of Inversion-Charge-Based Models

- additional approximation to solve for inversion charge
  \(\Rightarrow\) EKV, BSIM5, AMC
HiSIM Development History

1990 JJAP       Sub-1µm MOSFETs       short-channel effect model
1991 SISPAD     “                        1st surface-potential-based model
1994 ICCAD      “                        parameter extraction strategy
1995 Siemens    Flash-EEPROM           simulation time & stability verification
1998 STARC      100-nm MOSFET           concurrent device/circuit development

Release Activity

2001 Oct.       release to vendors     HiSIM1.0.0  source code and manual
2002 Jan.       release to public      “                        “
       June       “                        HiSIM1.1.0 “                        “
       Oct.       “                        HiSIM1.1.1 “                        “
2003 Oct.       Test release to STARC clients HiSIM2.0.0  source code and manual
2005 May        release to CMC members   HiSIM2.0.0 “                        “
       July       “                        HiSIM2.0.0 + Verilog-A code
       Oct.       “                        HiSIM2.2.0 “                        “
2006 Jan.       release to vendors     HiSIM2.3.0 “                        “
2006 Dec.       “                        HiSIM2.3.1 “                        “
2007 March

HiSIM2.4.0
## Modeled Phenomena in HiSIM2.4.0

<table>
<thead>
<tr>
<th>[Phenomena]</th>
<th>[Subjects]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Short Channel:</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Reverse-short Channel:</strong></td>
<td>impurity pile-up pocket implant</td>
</tr>
<tr>
<td><strong>Poly-Depletion:</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Quantum-Mechanical:</strong></td>
<td></td>
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<tr>
<td><strong>Channel-Length Modulation:</strong></td>
<td></td>
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<tr>
<td><strong>Narrow-Channel:</strong></td>
<td></td>
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<tr>
<td><strong>Temperature Dependency:</strong></td>
<td>thermal voltage bandgap $n$ phonon scattering maximum velocity</td>
</tr>
<tr>
<td><strong>Mobility Models:</strong></td>
<td>universal high Field</td>
</tr>
<tr>
<td><strong>Shallow-Trench Isolation:</strong></td>
<td>threshold voltage mobility leakage current</td>
</tr>
<tr>
<td><strong>Capacitances:</strong></td>
<td>intrinsic overlap lateral-field induced fringing</td>
</tr>
<tr>
<td><strong>Non-Quasi-Static:</strong></td>
<td>transient time-domain AC frequency-domain</td>
</tr>
<tr>
<td><strong>Noise:</strong></td>
<td>1/f thermal induced gate cross-correlation</td>
</tr>
<tr>
<td><strong>Leakage Currents:</strong></td>
<td>substrate current gate current GIDL current</td>
</tr>
<tr>
<td><strong>Source/Drain Resistances:</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Junction Diode:</strong></td>
<td>currents capacitances</td>
</tr>
</tbody>
</table>

- **Binning Option**
- **DFM Option**
## HiSIM Availability in Commercial EDA Software

<table>
<thead>
<tr>
<th>Type of EDA Software</th>
<th>HiSIM2.3.1</th>
<th>HiSIM2.4.0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Model Parameter Extraction</strong></td>
<td>Accelicon-MBP, BSIM ProPlus, EXPARA, ICCAP (Nov 07), UTMOST4</td>
<td>EXPARA, UTMOST4</td>
</tr>
<tr>
<td><strong>Circuit Simulation</strong></td>
<td>ADS, Eldo, FineSime, Hspice, HSIM, Nexxim, SmartSpice, Spectre, Ultrasim</td>
<td>Eldo, FineSim, Hspice, HSIM, Nexxim, SmartSpice, Spectre (Dec 07), Ultrasim (Dec 07)</td>
</tr>
</tbody>
</table>

HiSIM versions 231 and 240 are available in many commercial EDA tools for circuit analysis.
Outline

● Overview of Compact-Modeling Approaches

● Accuracy Aspects of HiSIM 2.3.1 and 2.4.0
  - Model Consistency Aspects
  - Surface-Potential Accuracy
  - Derivatives
  - Predictability, Variation Estimate
  - Inter-Modulation, Noise

● Speed Versus Accuracy Trade-Off and Position of Leading Compact Models

● Conclusion
The surface potential consistently determines charges, capacitances and currents under all operating conditions.
The absolute values of the HiSIM surface potential compare well with 2D simulation.
HiSIM accurately reproduces even the bias dependence of the surface-potential derivatives.
HiSIM can model even advanced 45nm technology very accurately without the necessity of binning.
The current derivatives of a 45nm technology can likewise be well reproduced with HiSIM.
HiSIM preserves Gummel symmetry under drain and source exchange up to 3rd derivatives.
Typical Extraction Result for 90nm CMOS (NMOS)

Source: Fujitsu (HiSIM231)

Small-error fitting is normally achieved without binning

\[ Error = 3.5 \text{[\%]} \]

\[ @V_g \geq V_{th} + 0.1 \text{[V]} \]

\[ L : 0.1 \leftrightarrow 5.02 \text{[\mu m]} \]

\[ Error = \sqrt{n \sum_{i=1}^{n} \text{Err}(i)^2} \]

\[ \text{Err}(i) = \frac{(\text{Sim}_i - \text{Meas}_i)}{\text{Meas}_i} \]
Typical Extraction Result for 90nm CMOS (PMOS)

Source: Fujitsu (HiSIM231)

Error = 2.7 [%]

@\(V_g \geq V_{th} + 0.1 [V]\)

\[L : 0.1 \Leftrightarrow 5.02 [\mu m]\]

PMOS, NMOS fitting approximately with equal quality
Predictability Test: Nominal Extraction

Source: Fujitsu (HiSIM231)

<table>
<thead>
<tr>
<th></th>
<th>Vds</th>
<th>Vgs</th>
<th>Vbs</th>
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<tbody>
<tr>
<td>ld1</td>
<td>1.2</td>
<td>1.2</td>
<td>0.0</td>
</tr>
<tr>
<td>ld2</td>
<td>1.2</td>
<td>1.2</td>
<td>-1.2</td>
</tr>
<tr>
<td>ld3</td>
<td>0.8</td>
<td>0.8</td>
<td>0.0</td>
</tr>
<tr>
<td>ld4</td>
<td>1.2</td>
<td>0.8</td>
<td>0.0</td>
</tr>
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</table>
Predictability Test: Changed Channel Dose

Source: Fujitsu (HiSIM231)

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</table>
Substrate-doping parameter correlates well with physical substrate doping value

Source: Fujitsu (HiSIM231)
Variation Prediction

**Ion variation**

Combined $I_{on}$, $V_{th}$ variation plot

Correct correlation between device and process parameters is required.

Surface-potential models like HiSIM are needed.

**$V_{th}$ variation**

Data: HiSIM231

(without pocket)
Inter-Wafer Variation Prediction

Prediction of inter-wafer variation for $I_{on}$, $V_{th}$ possible

Data: HiSIM231
Variation predictability is good even for derivatives

Data: HiSIM231
Inter-Wafer Variation Prediction: $g_{ds}$

Long Channel

Data: HiSIM231

Short Channel

Variation predictability is good even for derivatives
Evaluation of Derivative Characteristics

- Model: BSIM3v3, HiSIM2.3.1
- Device: 0.25um NMOS (Low Vth) \( W/L = 8\mu m / 4\mu m \)
- Condition:
  - Test1
    \( V_d = 0\sim 2V \) (0.02V step), \( V_g = 1.0\sim 2.5V \) (0.25V step), \( V_s = 1V, V_b = 0V \)
  - Test2
    \( V_d = 0\sim 2V \) (0.02V step), \( V_g = 1\sim 3V \) (0.5V step), \( V_s = 2\sim 0V \) (\( V_d \) synchronous), \( V_b = 0V \)

Source: Sony (HiSIM231)
Derivatives at Elevated Bias

HiSIM2.3.1 is in excellent agreement with measurement

Source: Sony (HiSIM231)
Derivatives for Source-Drain Interchange at 0V

HiSIM2.3.1 is in excellent agreement with measurement

Source: Sony (HiSIM231)
Evaluation of IM3 Characteristics (250nm CMOS)

- Model: BSIM3v3, HiSIM2.3.1
- Device: 0.25um NMOS (Low Vth)  W/L = 8um / 4um
- Conditions:
  - Input: 3.5/4.5MHz 2-tone, Output: Po1 3.5/4.5MHz, IM3: 2.5/5.5MHz
  - Simulation: Spectre-RF PSS Analysis

Source: Sony (HiSIM231)
IM3 Simulation in Comparison to Measurement

Accurate reproduction of IM3 measurements with HiSIM

Source: Sony (HiSIM231)
Evaluation of IM3 Characteristics (90nm CMOS)

- Model: BSIM4, HiSIM2.3.1, PSP102
- Device: 90nm technology, NMOS transistor, W/L = 8um / 4um
- Simulation condition
  - Input: 3.5/4.5MHz 2-tone, Output: Po1 3.5/4.5MHz, IM3: 2.5/5.5MHz
  - Simulation: PSS analysis of Spectre-RF

Source: Toshiba
IM3 Results for BSIM4, PSP102 and HiSIM2.3.1

Slope in IM3 Analysis (90nm CMOS)
BSIM4 : 2.0 (in large disagreement with theory)
PSP102 : 2.7 (in improved agreement with the theory)
HiSIM2.3 : 3 (in perfect agreement with the theory)

Source: Toshiba
1/f-Noise Evaluation

1/f noise model of BSIM model

\[ FN = \frac{q^2 V_{tn} I_{ds}}{C_{ox} L_{eff}^2 f_{EF}} \times 10^8 \left[ Noia \times \log \left( \frac{N_0 + 2 \times 10^{14}}{N_l + 2 \times 10^{14}} \right) + Noib \left( N_0 - N_l \right) + \frac{Noic}{2} \left( N_0^2 - N_l^2 \right) \right] \]

\[ + \frac{V_{tn} I_{ds} \Delta L_{clm}}{W_{eff} L_{eff}^2 f_{EF}} \times 10^8 \times \frac{Noia + Noib \times N_l - Noic \times N_l^2}{(N_l + 2 \times 10^{14})^2} \]

1/f noise model of HiSIM model

Very simple equation and high accuracy

Trap density

\[ S_{Idc} = \frac{I_{ds}^{NFTRP}}{\beta f (L_{eff} - \Delta L) W_{eff}} \left[ \frac{1}{(N_0 + N^*)(N_L + N^*)} + \frac{2 \mu E_{NFA}^{NFALP}}{N_L - N_0} \ln \left( \frac{N_L + N^*}{N_0 + N^*} \right) + \left( \mu E_{NFA}^{NFALP} \right)^2 \right] \]

Mobility fluctuation

Source: Toshiba
Simulation Results Compared with Measurements

HiSIM2.3.1 accurately reproduces $1/f$ measurements

Source: Toshiba (HiSIM2.3.1)
Outline

● Overview of Compact-Modeling Approaches
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● Conclusion
Is it possible to combine high speed and high accuracy to obtain an “ideal” MOSFET model?
High Cost Functions in the Source Code

The number of high-cost functions in the HiSIM2 source code is not larger than for advanced Vth-based models.

Data Source: Silvaco, Oct. 2005
Breakdown of HiSIM’s Model Evaluation Time

Iteration for surface-potential determination requires only a small fraction of the total model evaluation time.

Data: HiSIM2.4.0
Model Evaluation Time Comparison

- Model evaluation time of HiSIM2.4.0 is 20% improved and shorter than BSIM4.5.0.

$L = W = 1\mu m$

$V_{ds} = 1V, V_{bs} = 0$
Runtime Comparison of Compact Models

HiSIM2 executes faster than non-iterative surface-potential models as well as the latest Vth-based models.

Simulated Circuit Types:
(90nm CMOS, productively used circuits)
ADC, Active Driver, PLL, I/O Module, VCO, DLL, Parity Checker, MUX Buffer

Simulator:
SmartSpice 64bit, Version 3.3.0B

Data Source:
Simucad, Dec. 2006
Runtime of Inverter Chains with Different Length

Propagation delay times are equalized for all models.

Source: NEC
Runtime Comparison in 3 Different Simulators

Inverter chains with up to 2024 transistors

HiSIM2.3.1 computational runtimes are comparable to BSIM4. The relative runtimes of PSP102.1 consistently increase as a function of the transistor number.

Source: NEC
HiSIM2.4.0 is faster than BSIM4.5.0 and has comparable memory consumption. PSP runtimes increase strongly above 50K transistors.

Source: Simucad
Large RF Circuit Simulation Performance

- Ran on Opteron with 8 2.8GHz CPU and RH.4 OS
- FineSim Spice v2007.03.01

### GHz PLL Pre-Layout
- **MOSFET**: 3k
- **Resistor**: 0.05k
- **Capacitor**: 0.7k
- **Vsource**: 0.02k
- **Fvco=\frac{M}{N} \times F_{ref}=\text{GHz}
- **Tran**: 100us, TYP 1.0v, 25C

<table>
<thead>
<tr>
<th>MOS Model</th>
<th>Relative Runtime Pre-Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSIM 4.21</td>
<td>1.28</td>
</tr>
<tr>
<td>HiSIM 231</td>
<td>1</td>
</tr>
</tbody>
</table>

### GHz PLL Post-Layout
- **MOSFET**: 4k
- **Resistor**: 150k
- **Capacitor**: 60k
- **Vsource**: 0.02k
- **Fvco=\frac{M}{N} \times F_{ref}=\text{GHz}
- **Tran**: 100us, TYP 1.0v, 25C

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<tr>
<td>BSIM 4.21</td>
<td>1.66</td>
</tr>
<tr>
<td>HiSIM 231</td>
<td>1</td>
</tr>
</tbody>
</table>

Source: Magma
Conclusion

- HiSIM2.3.1 and 2.4.0 are a highly accurate MOSFET model based on the full iterative surface-potential concept.
- HiSIM2.3.1 and 2.4.0 have no runtime disadvantage in comparison to surface-potential models using a non-iterative approximation, but rather an advantage.
- HiSIM2.3.1 and 2.4.0 have even shorter computer runtime than the most advanced Vth-based models.

HiSIM2 (Versions 231 and 240) is a compact MOSFET model concept with optimized accuracy/speed trade-off.