

# Accuracy and Speed Performance of HiSIM Versions 231 and 240

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# Outline


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- **Overview of Compact-Modeling Approaches**
- Accuracy Aspects of HiSIM2.3.1 and 2.4.0
- Speed Versus Accuracy Trade-Off and Position of Leading Compact Models
- Conclusion

# Basic Compact Model Approaches for the MOSFET

## Threshold-Voltage-Based Models (e. g. BSIM3, BSIM4)

- currents expressed as functions of applied voltages
- different equations for:
  - sub-threshold region
  - linear region
  - saturation region


$$I_{ds} = \mu C_{ox} \frac{W}{L} \left\{ (V_{gs} - V_{th}) V_{ds} - \left( \frac{1}{2} + \frac{\sqrt{2\epsilon_{Si} q N_{sub}}}{4C_{ox}} \sqrt{2\Phi_B} \right) V_{ds}^2 \right\}$$

## New Generation of Surface-Potential-Based Models

$$C_{ox}(V_G' - \phi_S(y)) = \sqrt{\frac{2\epsilon_{Si} q N_{sub}}{\beta}} \left[ \exp\{-\beta(\phi_S(y) - V_{bs})\} + \beta(\phi_S(y) - V_{bs}) - 1 + \frac{n_{p0}}{p_{p0}} \left\{ \exp(\beta(\phi_S(y) - \phi_f(y))) - \exp(\beta(V_{bs} - \phi_f(y))) \right\} \right]^{\frac{1}{2}}$$

- implicit equation for surface potential
- currents determined from drift and diffusion term of current density equation
- developed calculation methods for the surface potential:
  - iterative solution with the exact surface-potential equation  $\Rightarrow$  HiSIM
  - approximate explicit solution by 1<sup>st</sup> & 2<sup>nd</sup> order perturbation theory, after prior conditioning of the surface-potential equation  $\Rightarrow$  PSP

## New Generation of Inversion-Charge-Based Models

- additional approximation to solve for inversion charge  
 $\Rightarrow$  EKV, BSIM5, AMC

# HiSIM Development History

1990 JJAP	Sub-1 $\mu$ m MOSFETs	short-channel effect model
1991 SISPAD	“	1 <sup>st</sup> surface-potential-based model
		parameter extraction strategy
<b>1994 ICCAD</b>	“	<b>simulation time &amp; stability verification</b>
1995 Siemens	Flash-EEPROM	concurrent device/circuit development
1998 STARC	100-nm MOSFET	collaboration start

## Release Activity

2001 Oct.	release to vendors	HiSIM1.0.0	source code and manual
2002 Jan.	release to public	“	“
June	“	HiSIM1.1.0	“
Oct.	“	HiSIM1.1.1	“
2003 Oct.	Test release to STARC clients	HiSIM2.0.0	source code and manual
2005 May	release to CMC members	HiSIM2.0.0	“
July	“		+ Verilog-A code
Oct.	“	HiSIM2.2.0	“
2006 Jan.	release to vendors	HiSIM2.3.0	“
<b>2006 Dec.</b>	“	<b>HiSIM2.3.1</b>	
<b>2007 March</b>		<b>HiSIM2.4.0</b>	

# Modeled Phenomena in HiSIM2.4.0

[Phenomena]	[Subjects]	[Phenomena]	[Subjects]
Short Channel:		Non-Quasi-Static:	transient time-domain AC frequency-domain
Reverse-short Channel:	impurity pile-up pocket implant	Noise:	1/f thermal induced gate cross-correlation
Poly-Depletion:		Leakage Currents:	substrate current gate current GIDL current
Quantum-Mechanical:		Source/Drain Resistances:	
Channel-Length Modulation:		Junction Diode:	currents capacitances
Narrow-Channel:			
Temperature Dependency:	thermal voltage bandgap $n_i$ phonon scattering maximum velocity		
Mobility Models:	universal high Field		
Shallow-Trench Isolation:	threshold voltage mobility leakage current		
Capacitances:	intrinsic overlap lateral-field induced fringing		

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**Binning Option**  
**DFM Option**

# HiSIM Availability in Commercial EDA Software

Type of EDA Software	HiSIM2.3.1	HiSIM2.4.0
Model Parameter Extraction	Accelicon-MBP, BSIM ProPlus, EXPARA, ICCAP (Nov 07), UTMOST4	EXPARA, UTMOST4
Circuit Simulation	ADS, Eldo, FineSime, Hspice, HSIM, Nexxim, SmartSpice, Spectre, Ultrasim	Eldo, FineSim, Hspice, HSIM, Nexxim, SmartSpice, Spectre (Dec 07), Ultrasim (Dec 07)

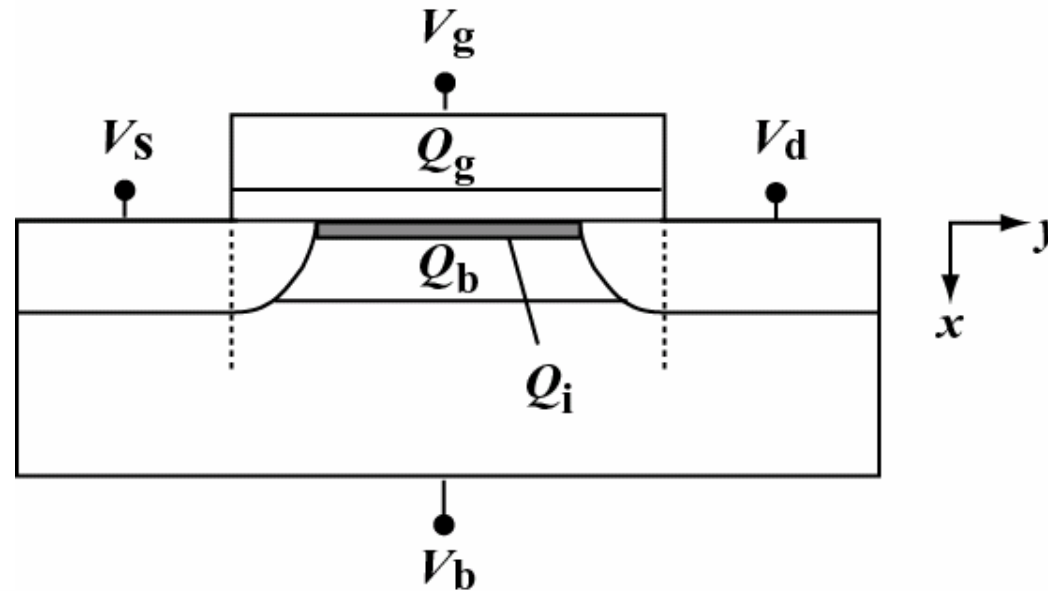
HiSIM versions 231 and 240 are available in many commercial EDA tools for circuit analysis.

# Outline

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- Overview of Compact-Modeling Approaches
- **Accuracy Aspects of HiSIM2.3.1 and 2.4.0**
  - Model Consistency Aspects
  - Surface-Potential Accuracy
  - Derivatives
  - Predictability, Variation Estimate
  - Inter-Modulation, Noise
- Speed Versus Accuracy Trade-Off and Position of Leading Compact Models
- Conclusion

# Consistency Property of Surface-Potential Model



$$I_{ds} = q \frac{W}{L} \int v Q_i dy$$

$v = \mu E$ : velocity

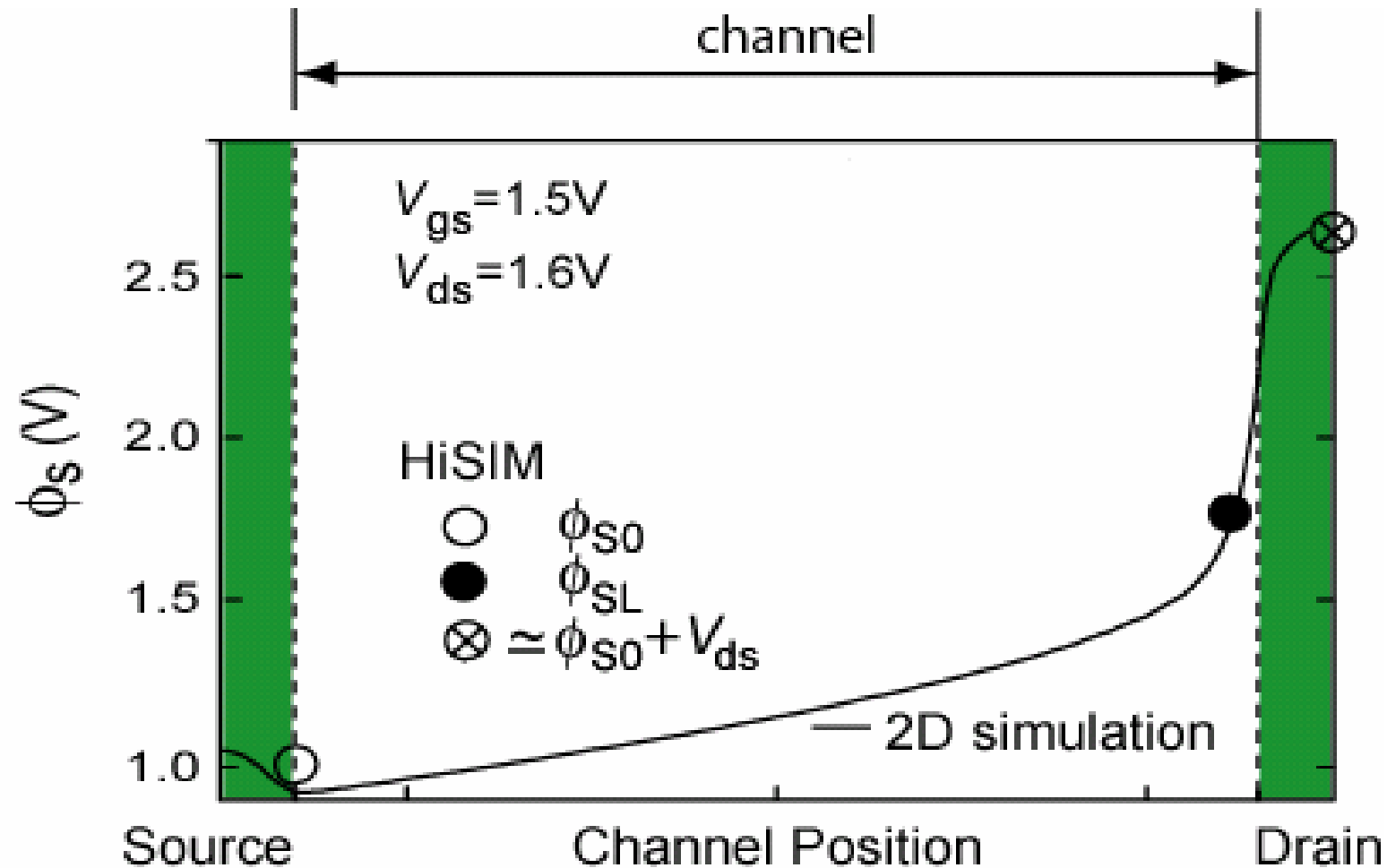
$$Q(\phi)$$

$$C_{jk} = \frac{dQ_j}{dV_k}$$

$$\frac{1}{\mu_0} = \frac{1}{\mu_{CB}} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} : \text{mobility}$$

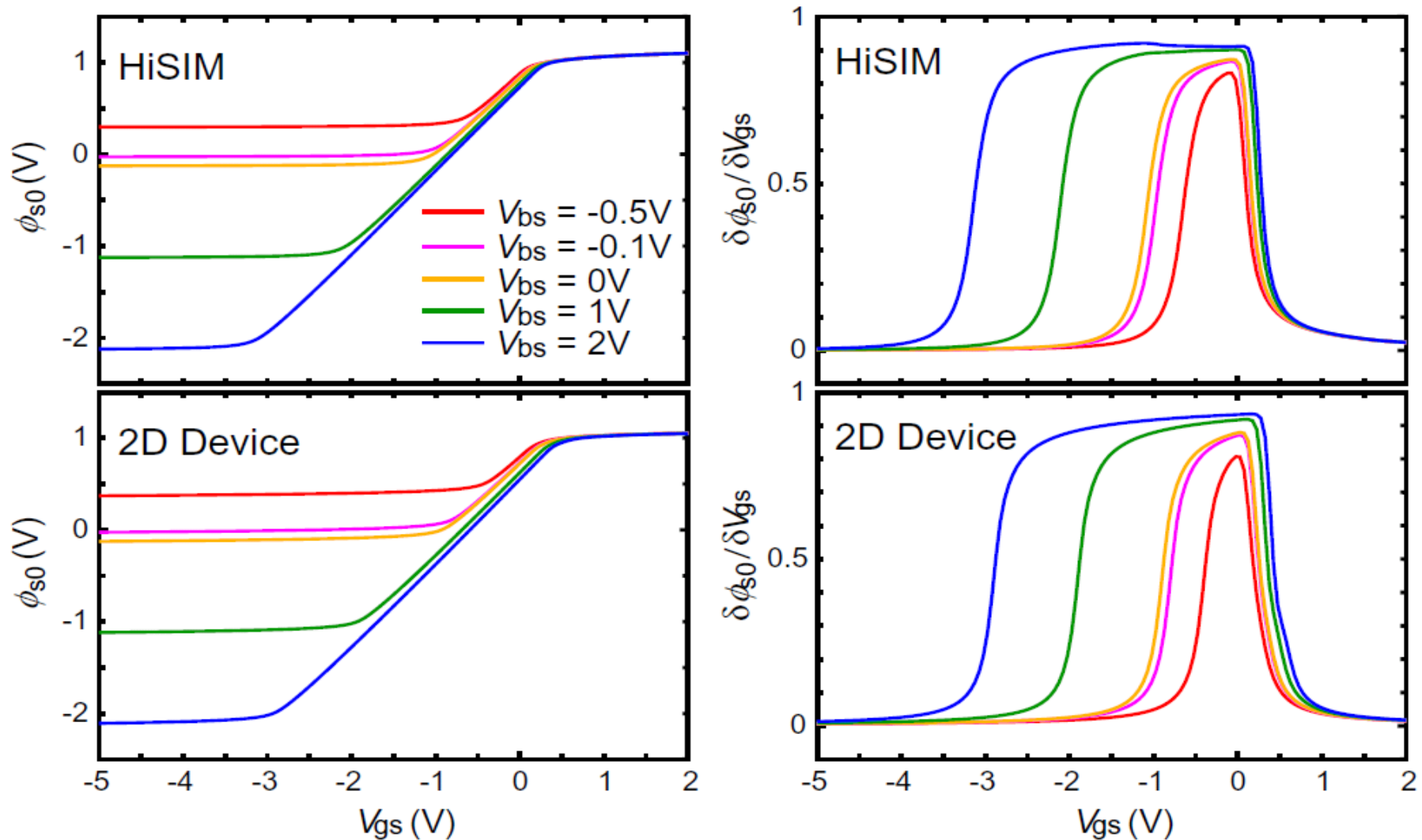
The surface potential consistently determines charges, capacitances and currents under all operating conditions.

# HiSIM Surface Potential at Source and Drain



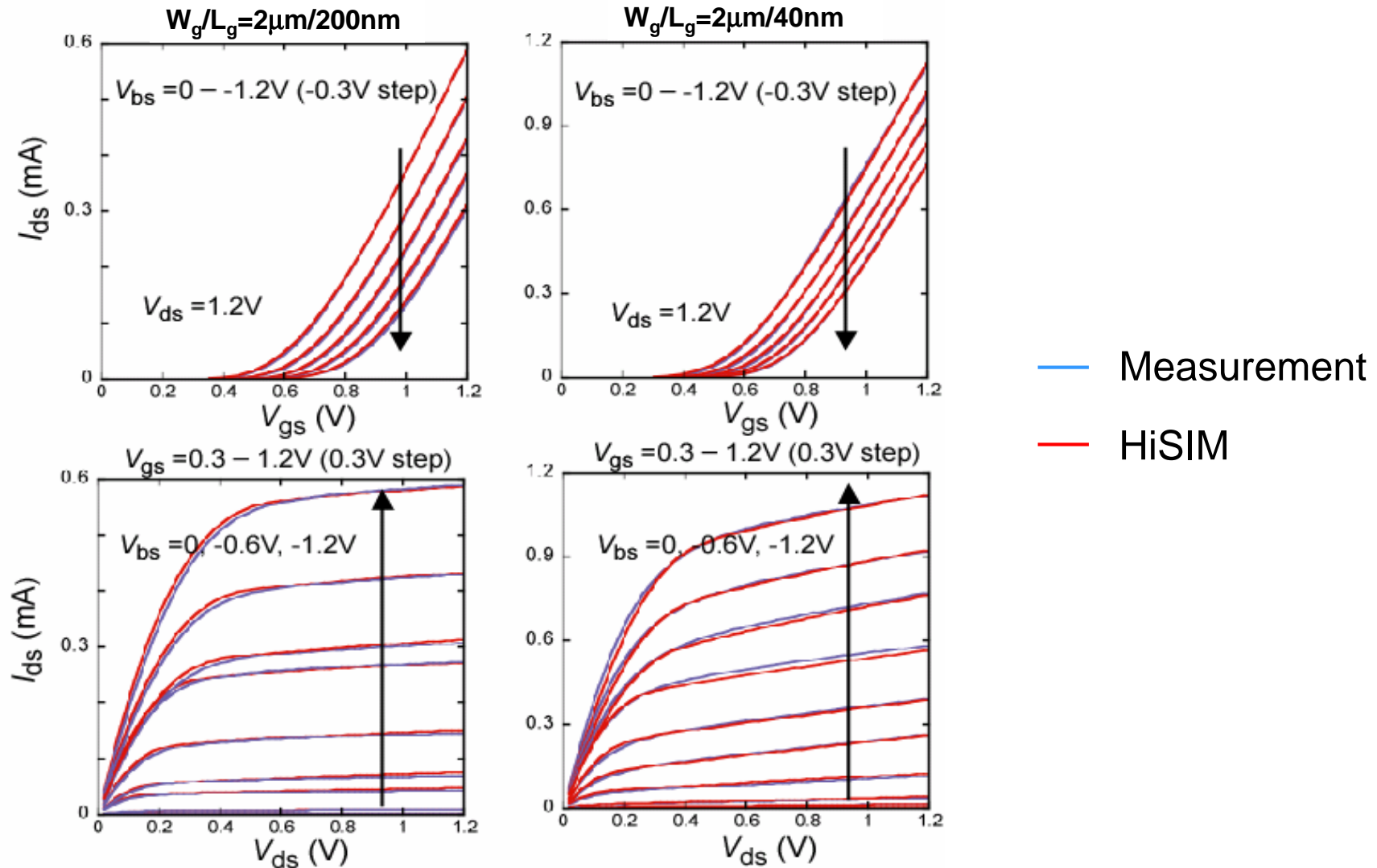
The absolute values of the HiSIM surface potential compare well with 2D simulation.

# Bias Dependence & Derivatives of Surface Potential



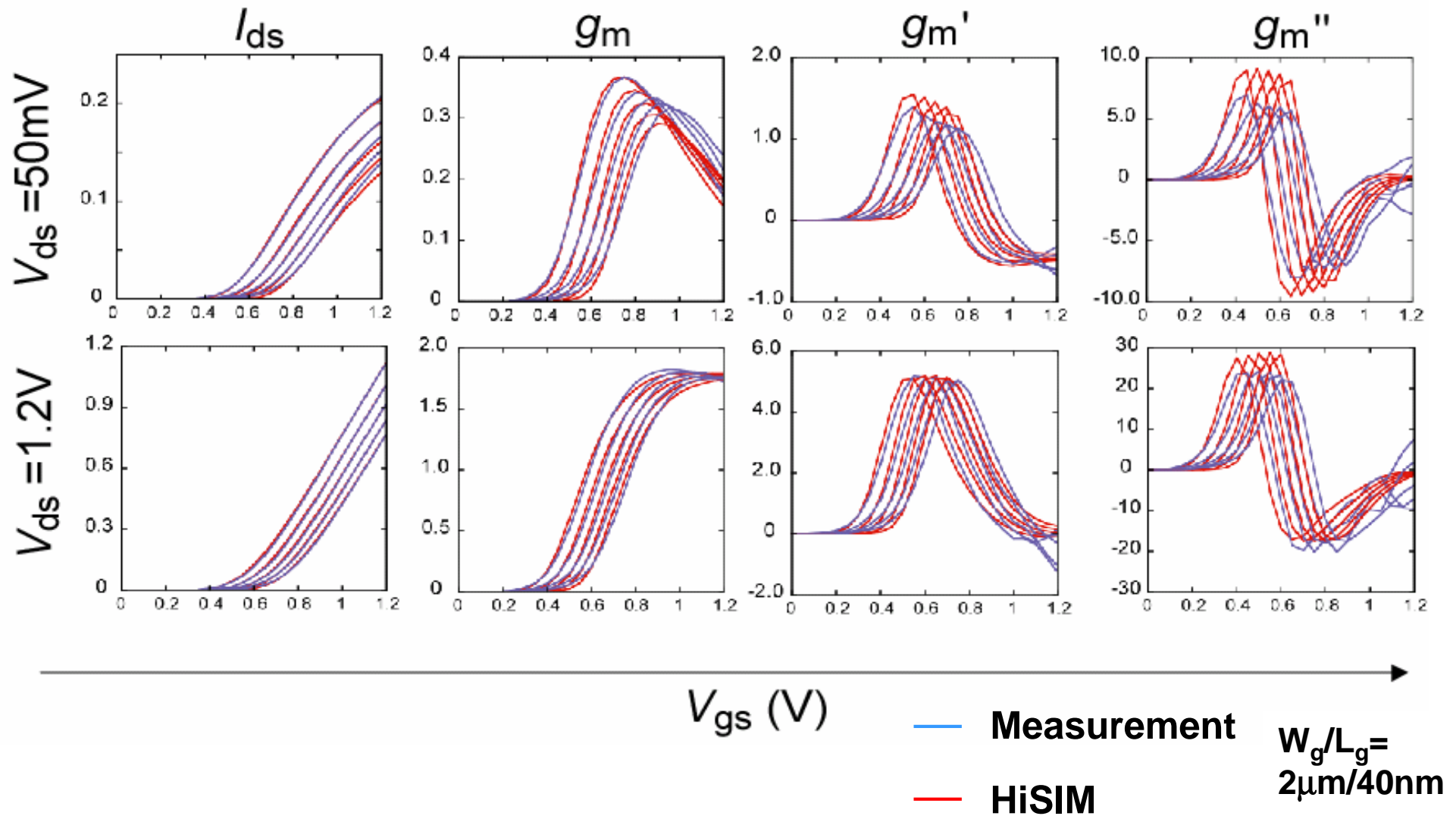
HiSIM accurately reproduces even the bias dependence of the surface-potential derivatives.

# Model Extraction for Advanced 45nm Technology



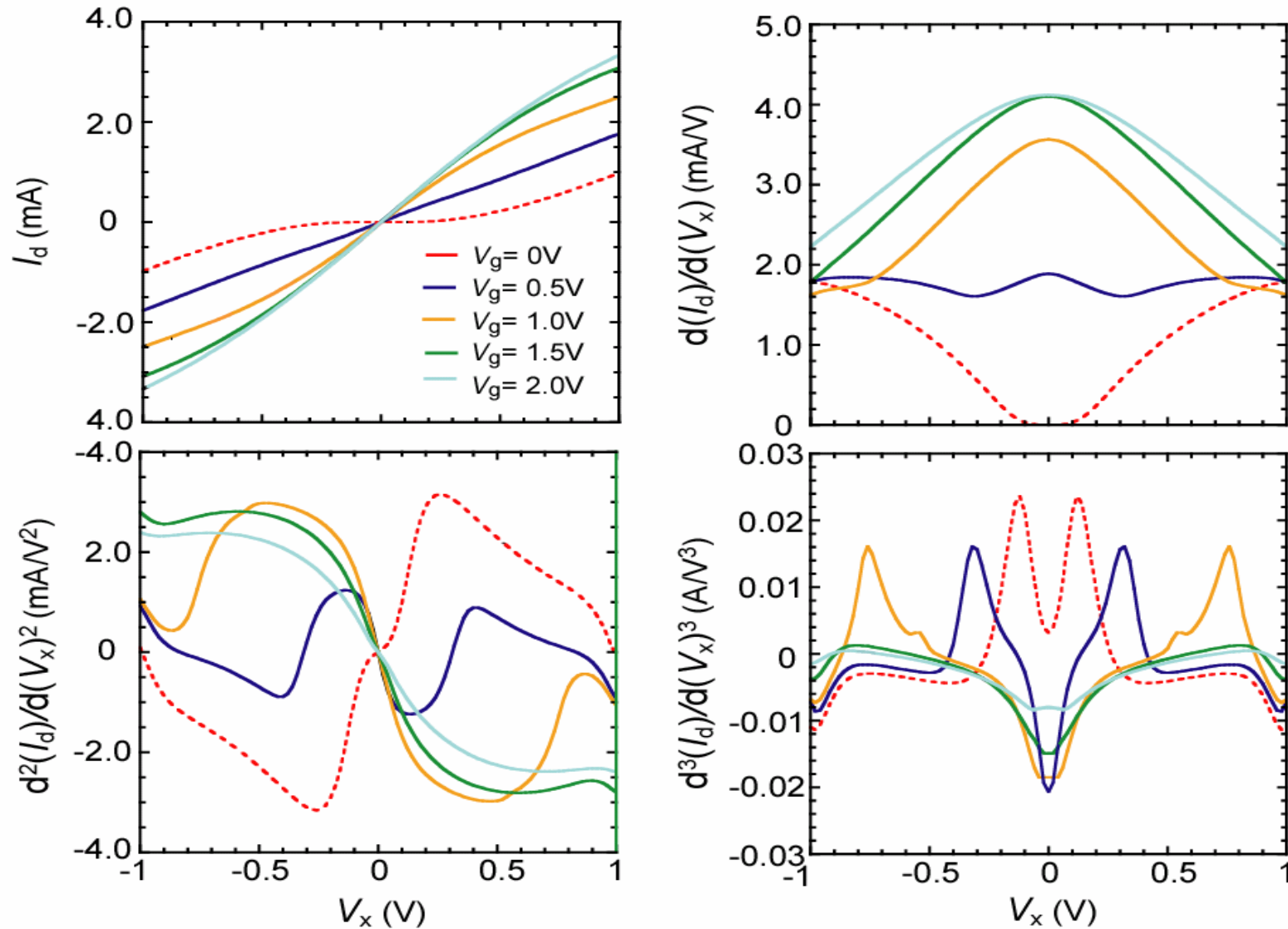
HiSIM can model even advanced 45nm technology very accurately without the necessity of binning.

# Current Derivatives for Advanced 45nm Technology



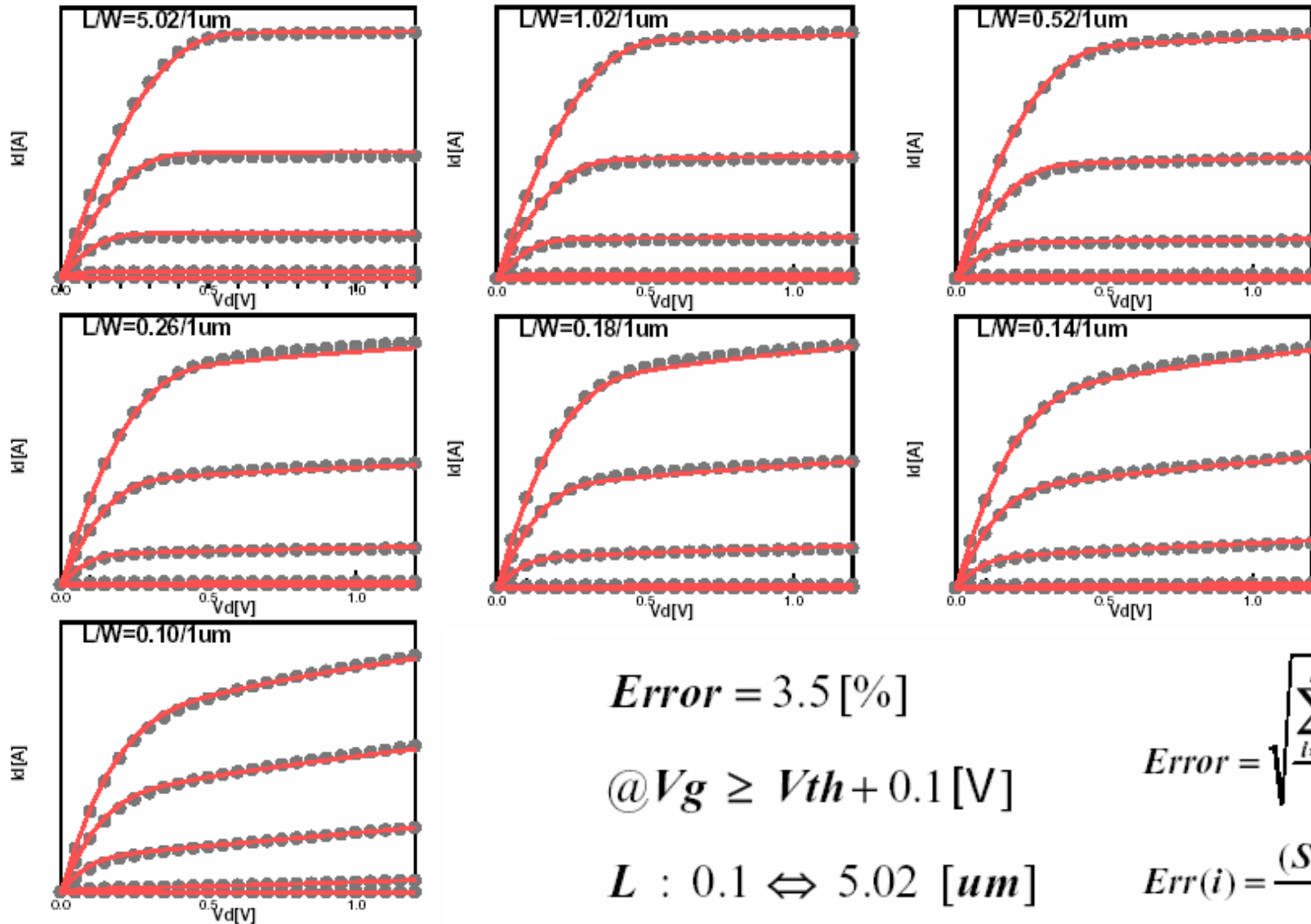
The current derivatives of a 45nm technology can likewise be well reproduced with HiSIM.

# Gummel-Symmetry Properties



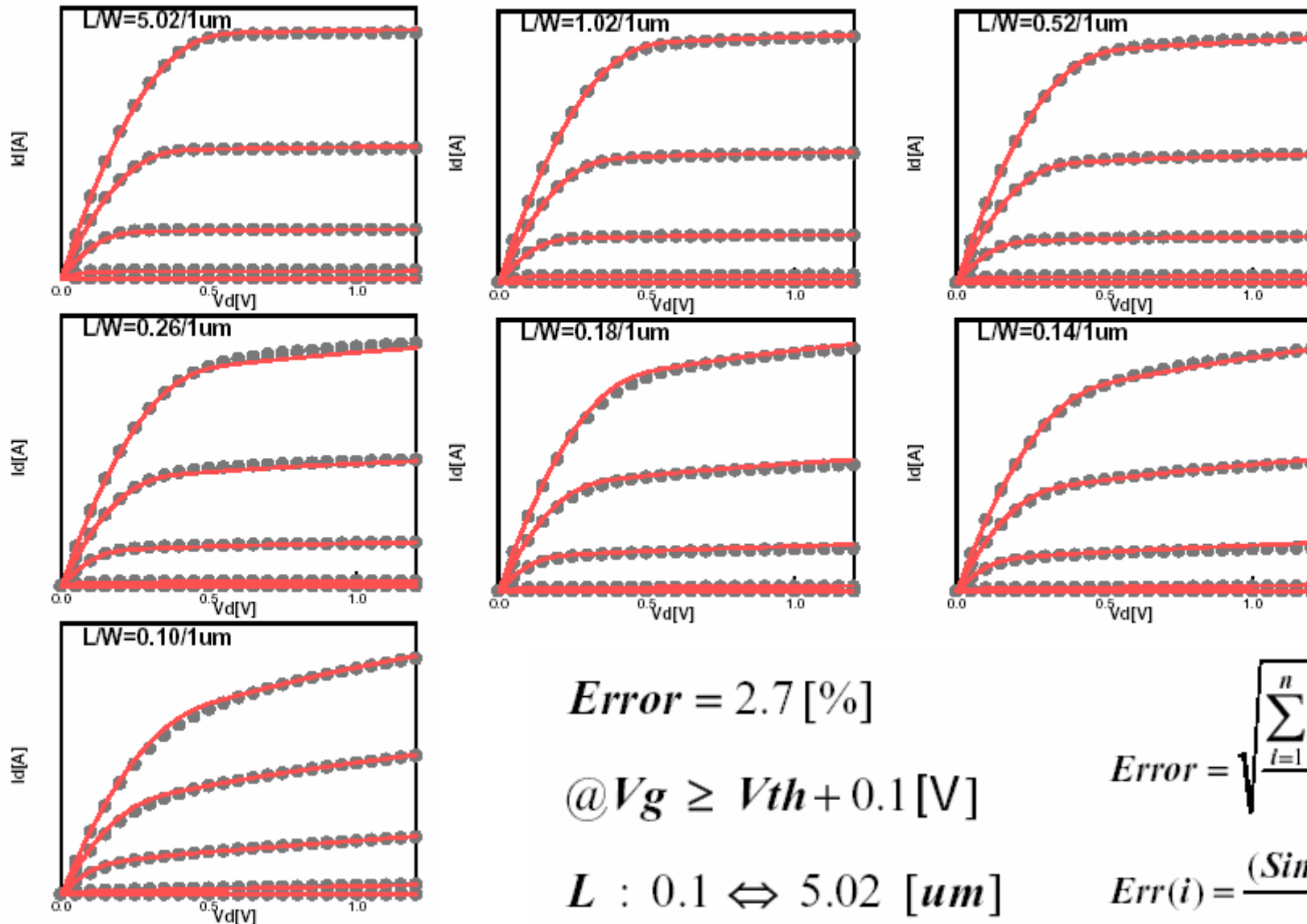
HiSIM preserves Gummel symmetry under drain and source exchange up to 3<sup>rd</sup> derivatives.

# Typical Extraction Result for 90nm CMOS (NMOS)



Small-error fitting is normally achieved without binning

# Typical Extraction Result for 90nm CMOS (PMOS)



Source:  
Fujitsu  
(HiSIM231)

$$Error = 2.7 [\%]$$

$$@Vg \geq Vth + 0.1 [V]$$

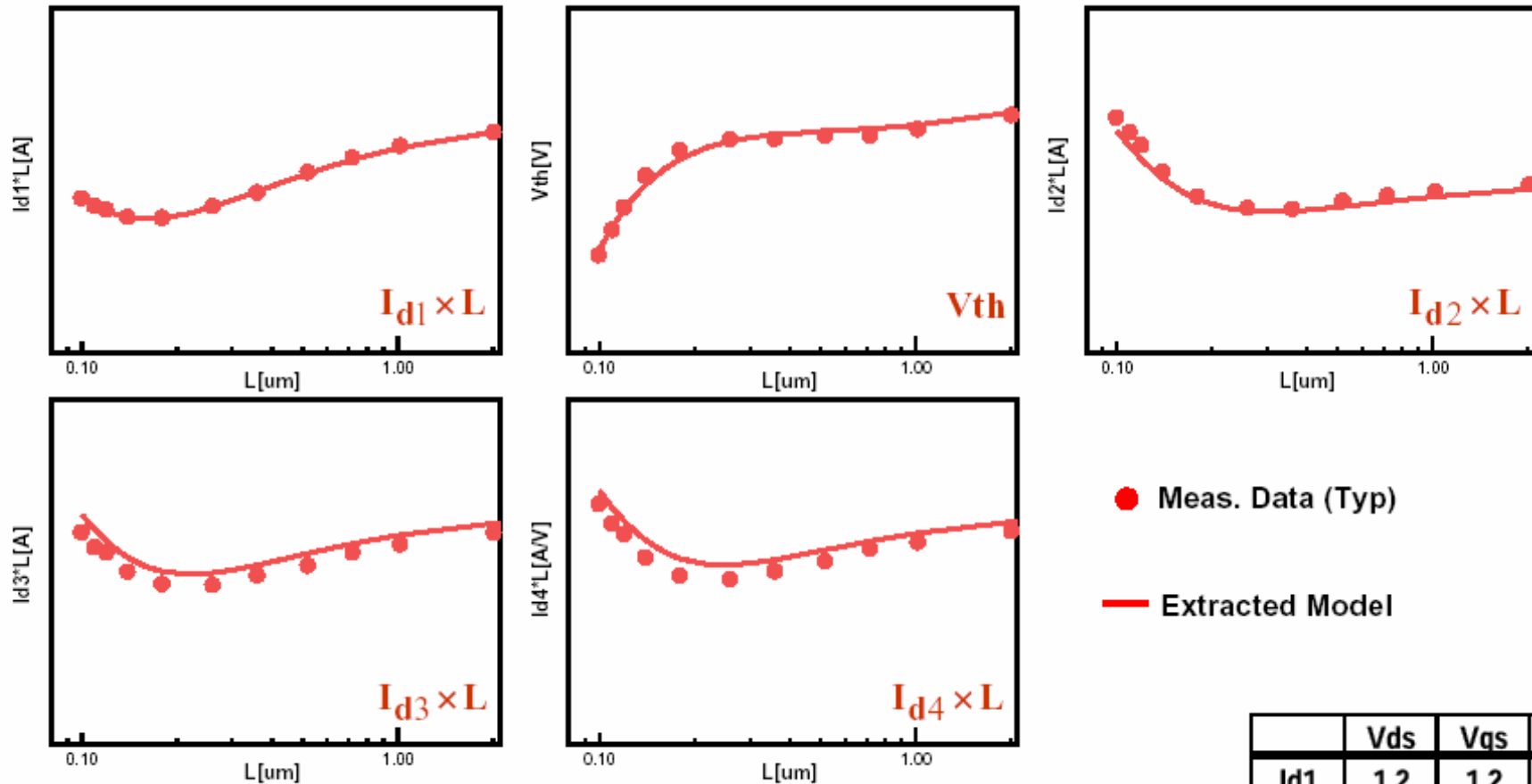
$$L : 0.1 \Leftrightarrow 5.02 [um]$$

$$Error = \sqrt{\frac{\sum_{i=1}^n Err(i)^2}{n}}$$

$$Err(i) = \frac{(Sim_i - Meas_i)}{Meas_i}$$

PMOS, NMOS fitting approximately with equal quality

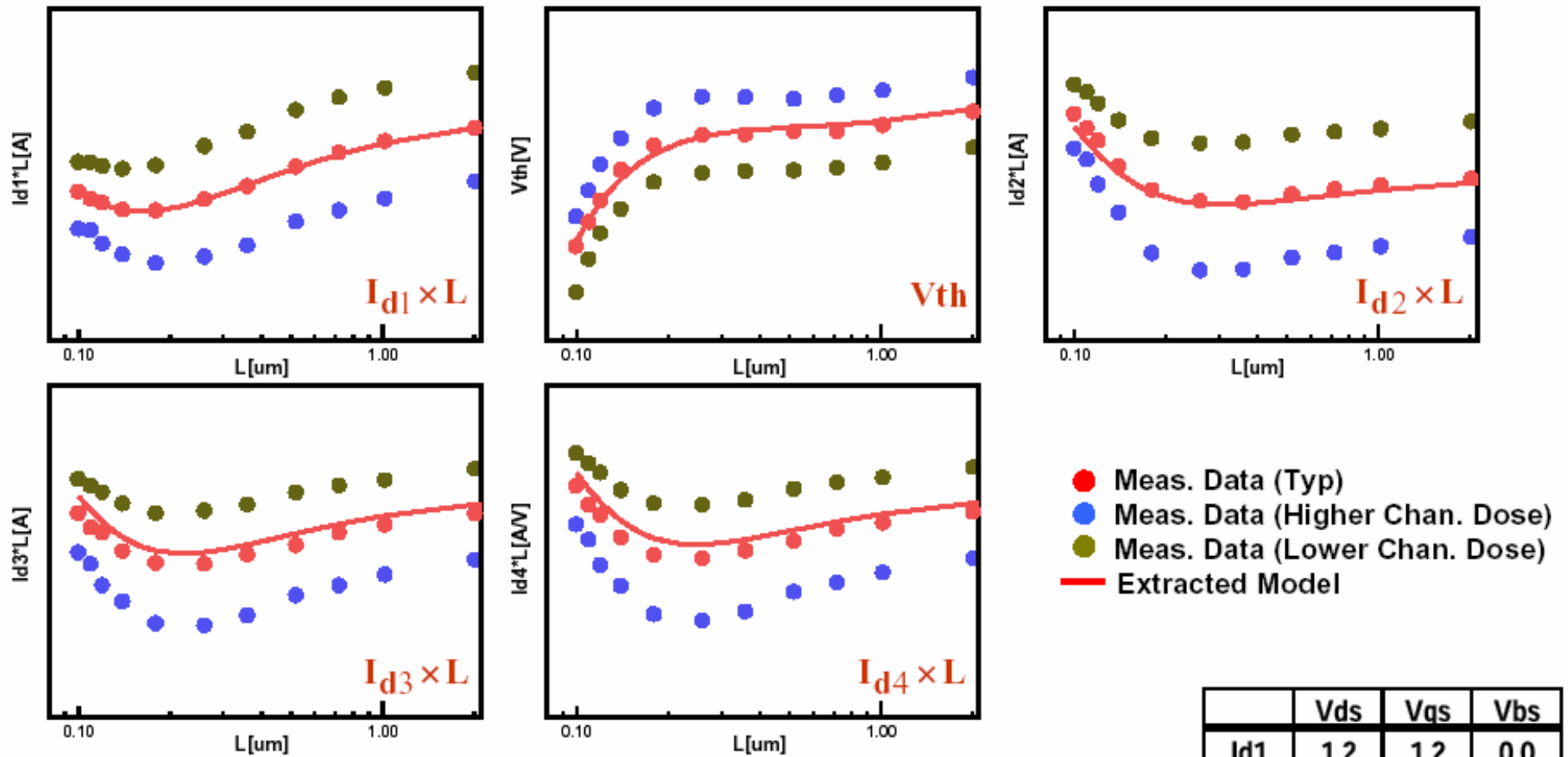
# Predictability Test: Nominal Extraction



Source: Fujitsu (HiSIM231)

	$V_{ds}$	$V_{gs}$	$V_{bs}$
$I_{d1}$	1.2	1.2	0.0
$I_{d2}$	1.2	1.2	-1.2
$I_{d3}$	0.8	0.8	0.0
$I_{d4}$	1.2	0.8	0.0

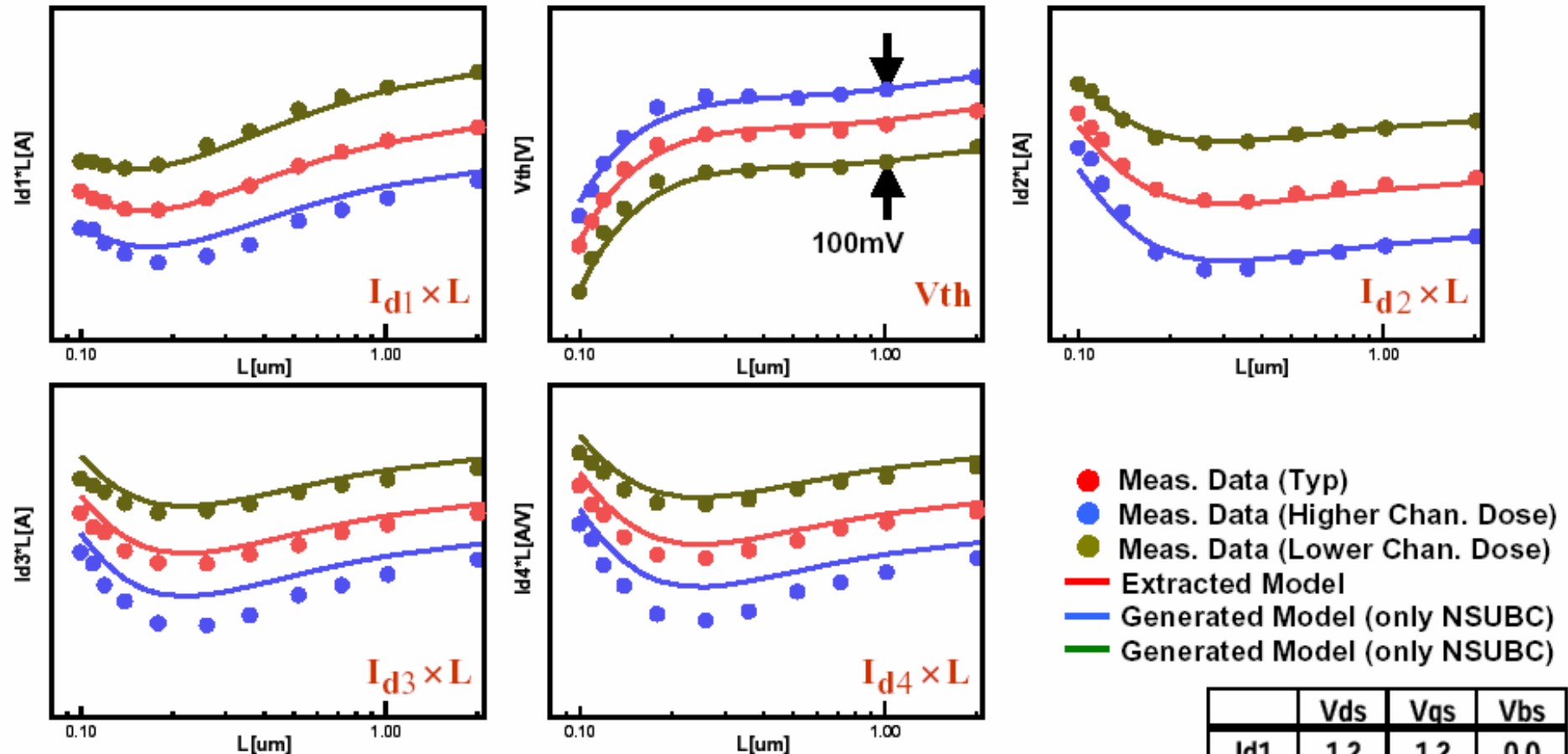
# Predictability Test: Changed Channel Dose



Source: Fujitsu (HiSIM231)

	Vds	Vgs	Vbs
Id1	1.2	1.2	0.0
Id2	1.2	1.2	-1.2
Id3	0.8	0.8	0.0
Id4	1.2	0.8	0.0

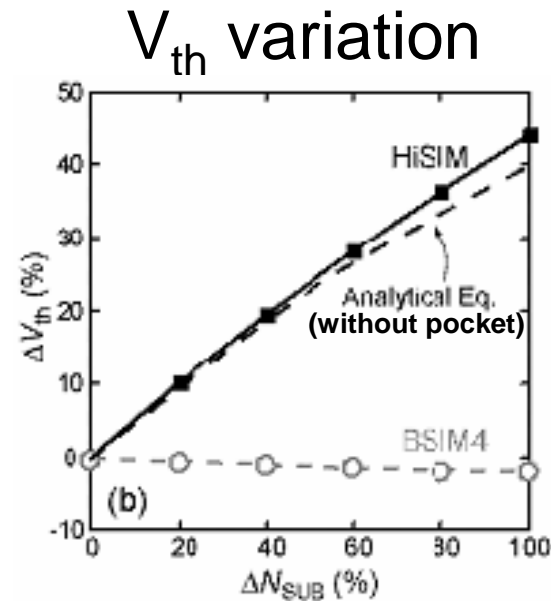
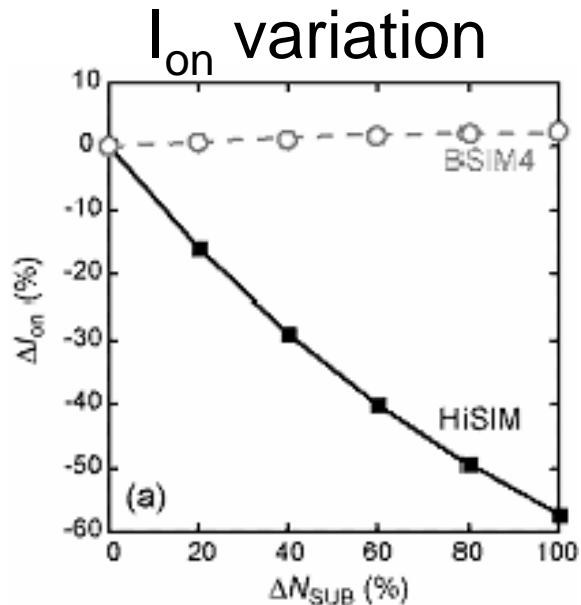
# Predictability Test: Adjustment of Substrate Doping



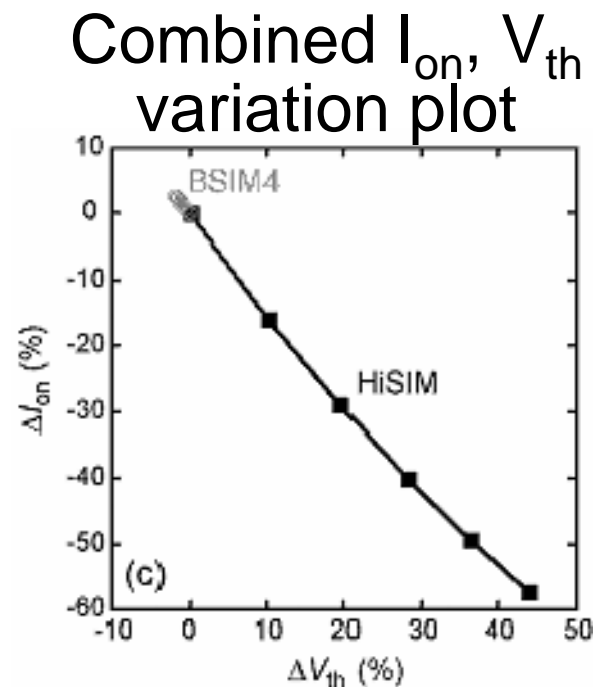
Source: Fujitsu (HiSIM231)

Substrate-doping parameter correlates well with physical substrate doping value

# Variation Prediction



Data:  
HiSIM231



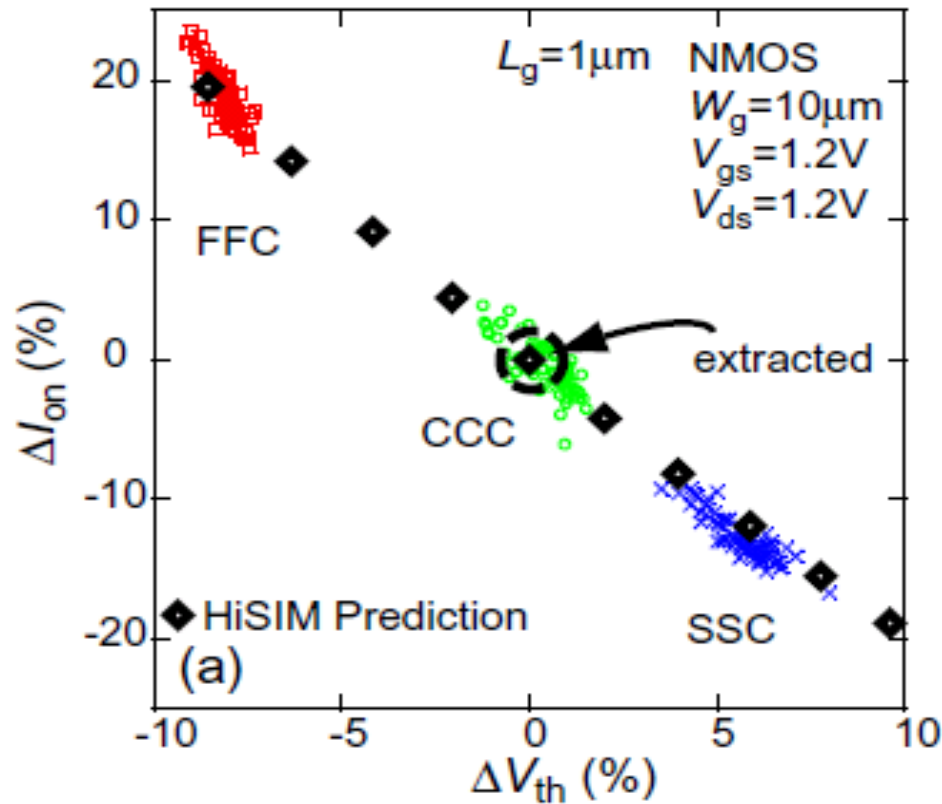
Correct correlation between device and process parameters is required.



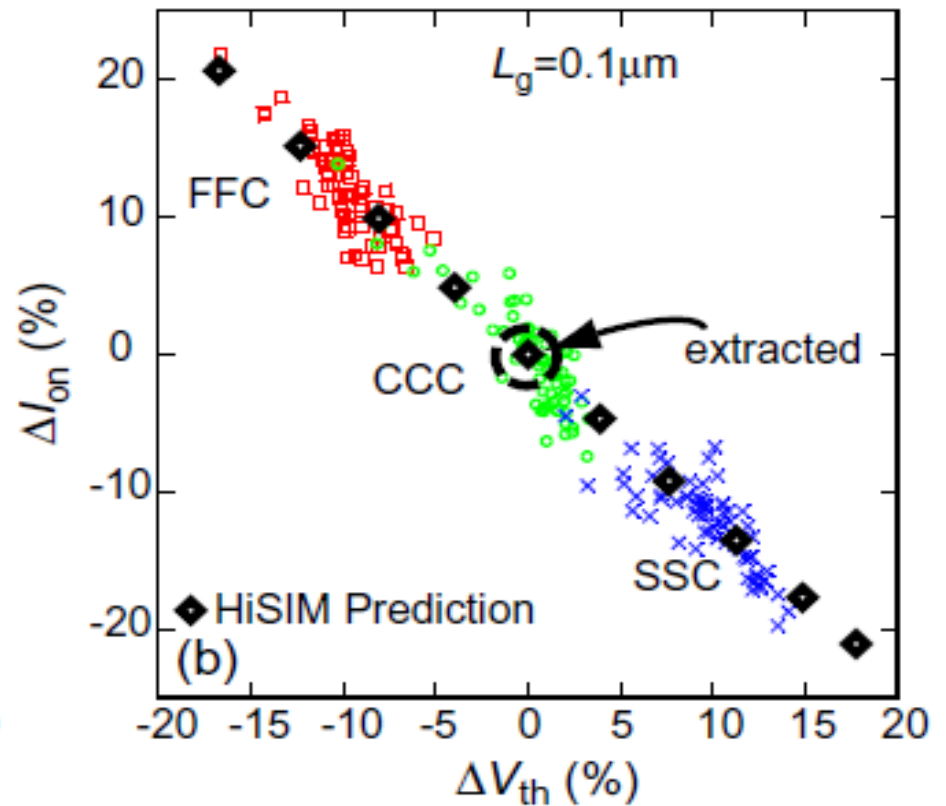
Surface-potential models like HiSIM are needed.

# Inter-Wafer Variation Prediction

## Long Channel



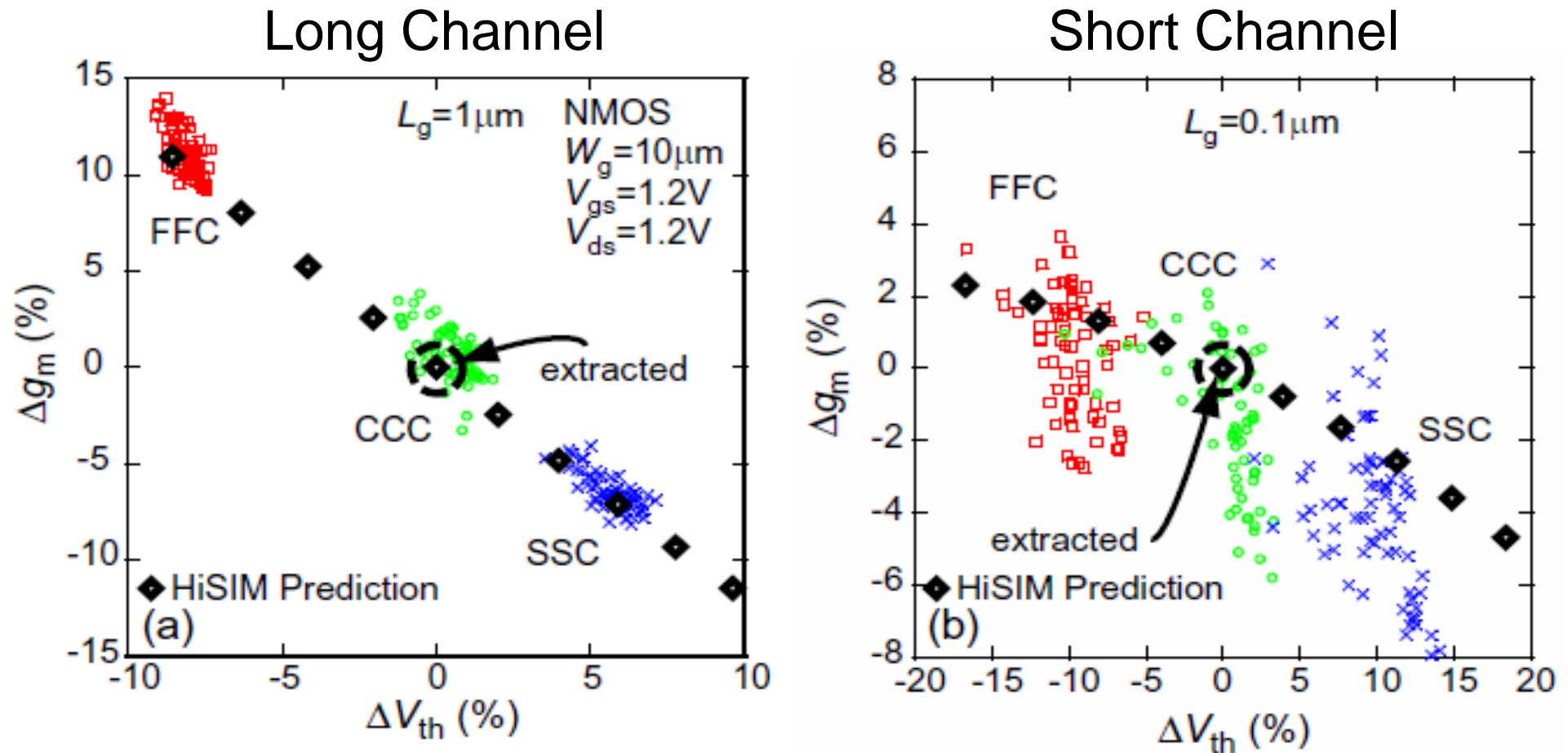
## Short Channel



Data: HiSIM231

Prediction of inter-wafer variation for  $I_{on}$ ,  $V_{th}$  possible

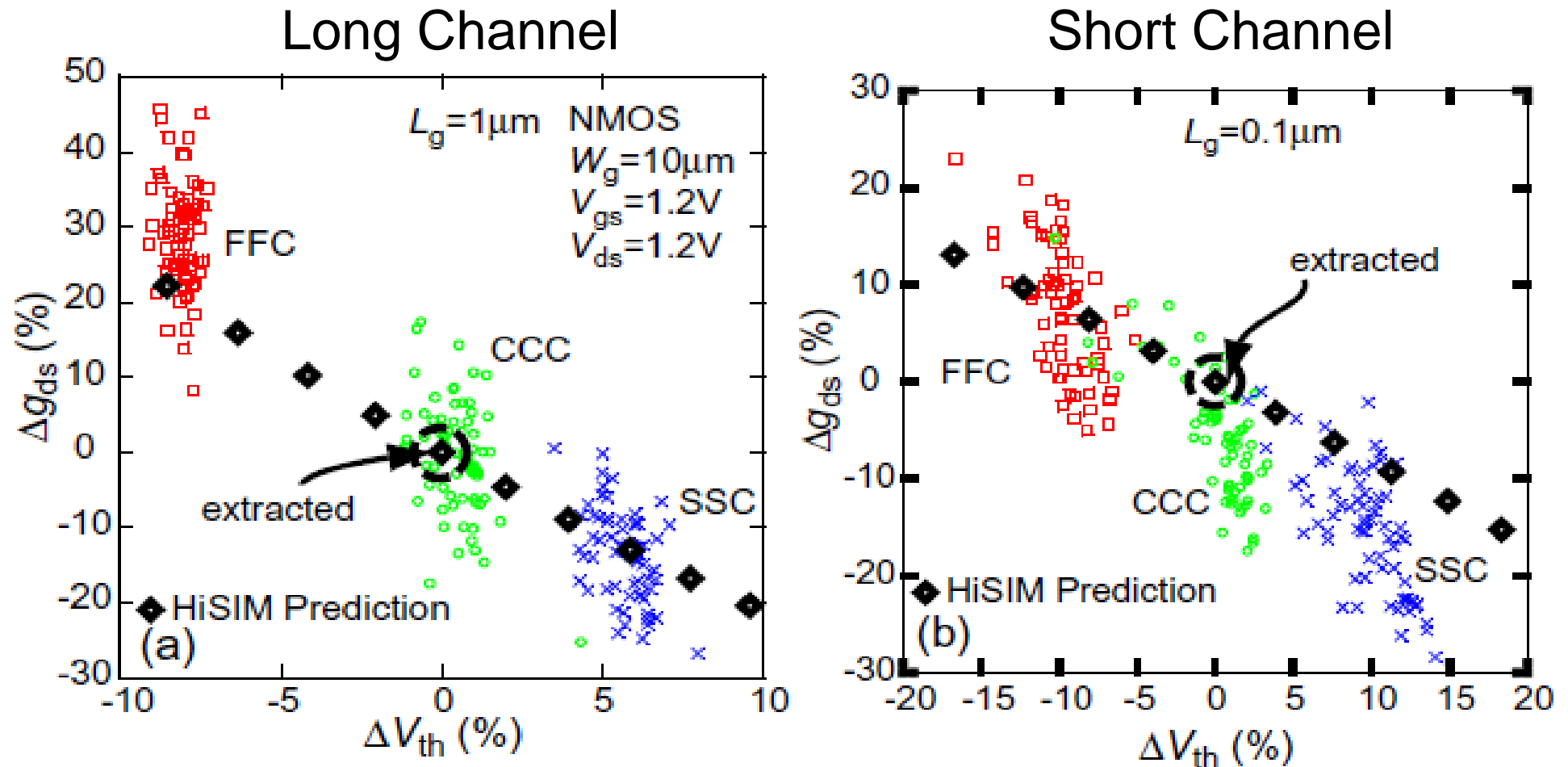
# Inter-Wafer Variation Prediction: $g_m$



Data: HiSIM231

Variation predictability is good even for derivatives

# Inter-Wafer Variation Prediction: $g_{ds}$

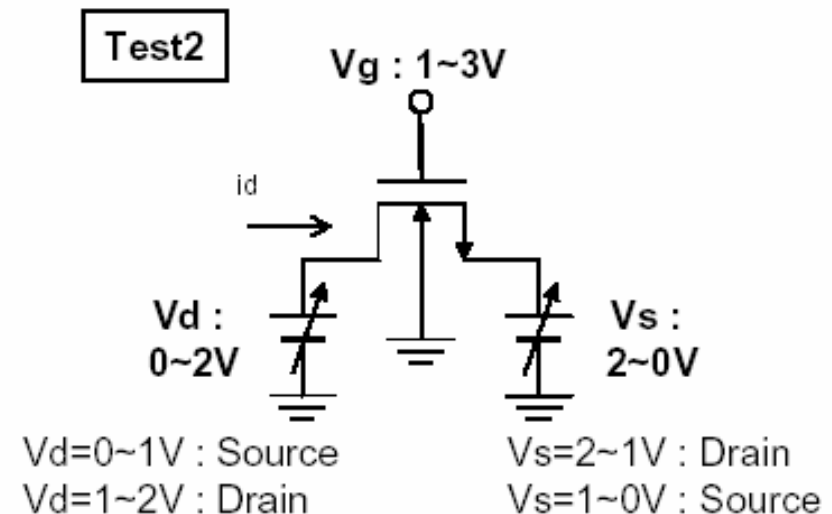
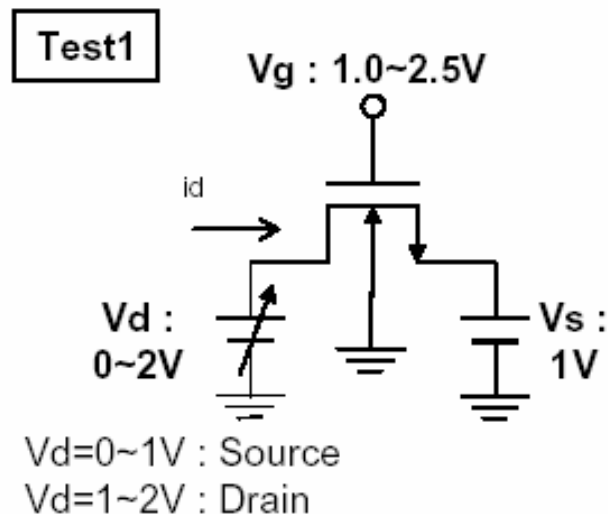


Data: HiSIM231

Variation predictability is good even for derivatives

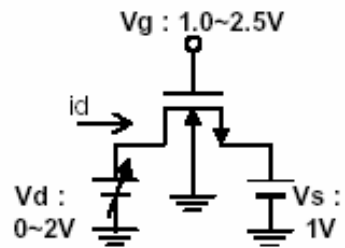
# Evaluation of Derivative Characteristics

- Model : BSIM3v3, HiSIM2.3.1
- Device : 0.25um NMOS(Low  $V_{th}$ )  $W/L = 8\mu\text{m} / 4\mu\text{m}$
- Condition :
  - Test1  
 $v_d=0\sim 2\text{V}$ (0.02V step),  $v_g=1.0\sim 2.5\text{V}$ (0.25V step),  $v_s=1\text{V}$ ,  $v_b=0\text{V}$
  - Test2  
 $v_d=0\sim 2\text{V}$ (0.02V step),  $v_g=1\sim 3\text{V}$ (0.5V step),  $v_s=2\sim 0\text{V}$ ( $v_d$  synchronous),  $v_b=0\text{V}$



Source: Sony (HiSIM231)

# Derivatives at Elevated Bias



Source: Sony (HiSIM231)

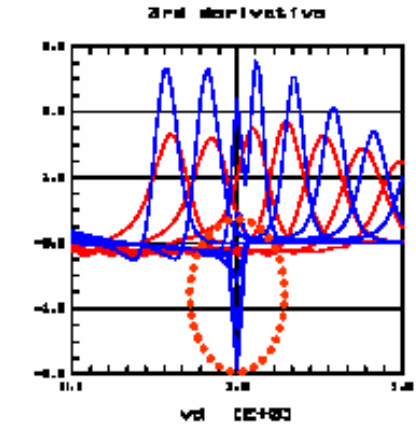
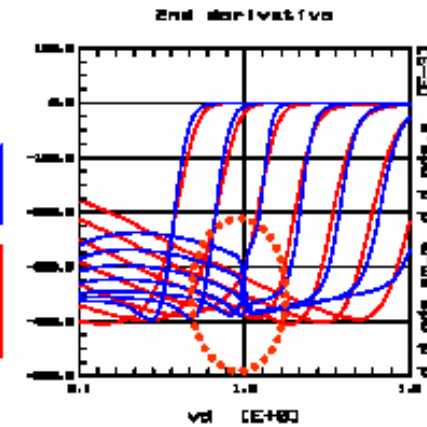
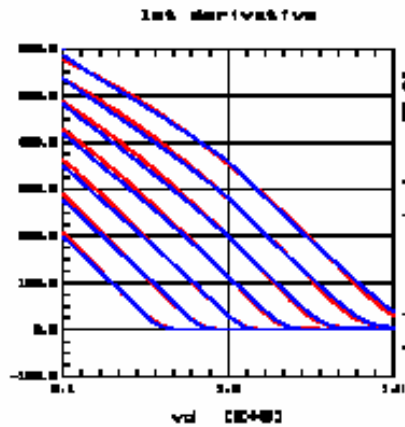
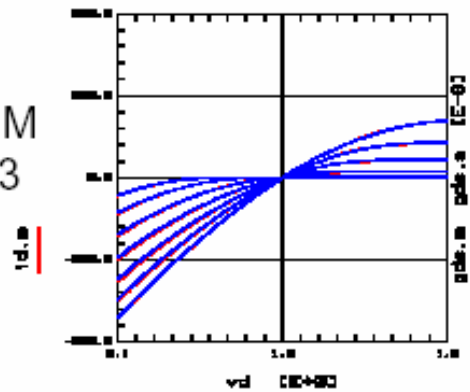
$i_d - v_d$

1<sup>st</sup> deriv  $\frac{\partial i_d}{\partial v_{ds}} - v_d$

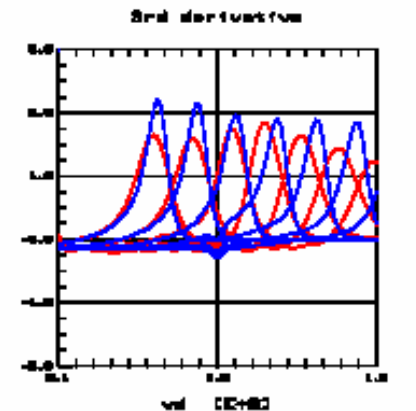
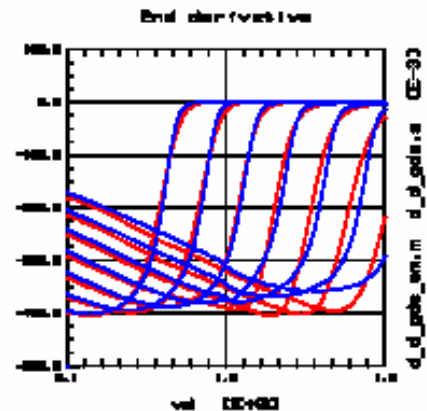
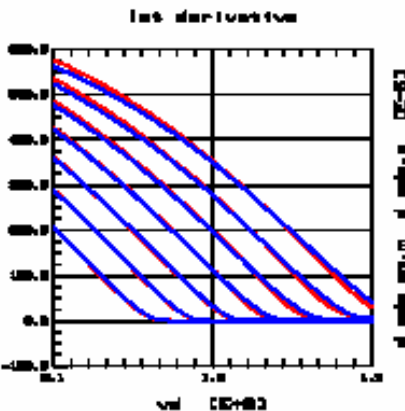
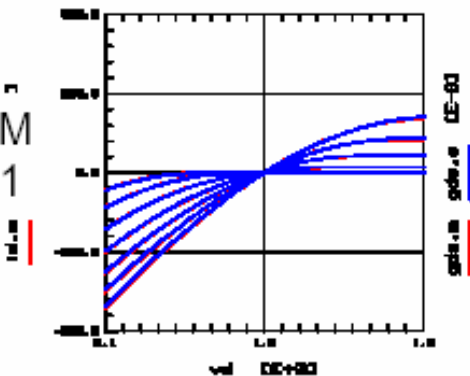
2<sup>nd</sup> deriv  $\frac{\partial^2 i_d}{\partial v_{ds}^2} - v_d$

3<sup>rd</sup> deriv  $\frac{\partial^3 i_d}{\partial v_{ds}^3} - v_d$

BSIM  
3v3

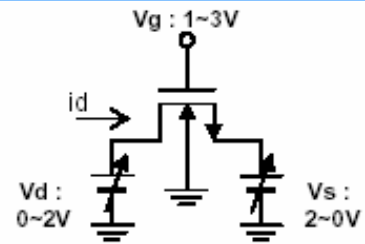


HiSIM  
2.3.1



HiSIM2.3.1 is in excellent agreement with measurement

# Derivatives for Source-Drain Interchange at 0V



— Measure  
— Model

Source: Sony (HiSIM231)

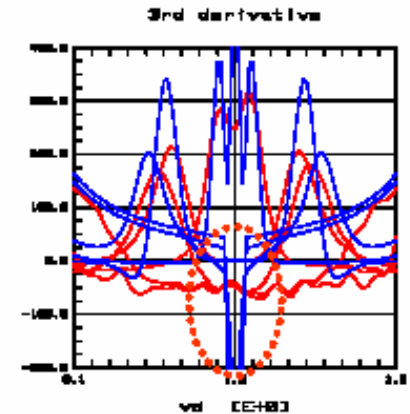
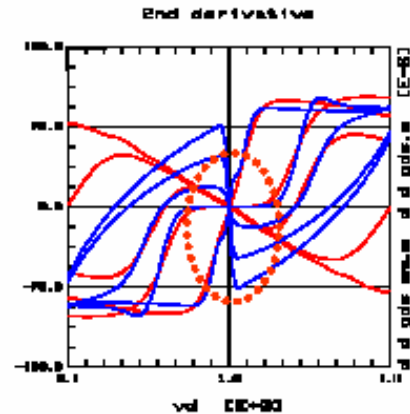
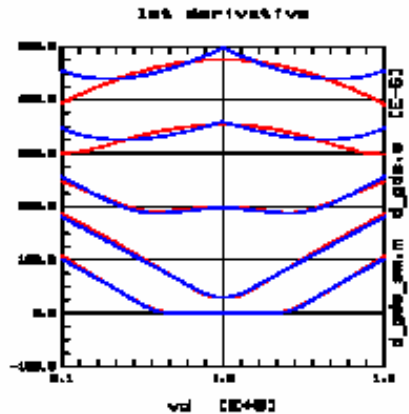
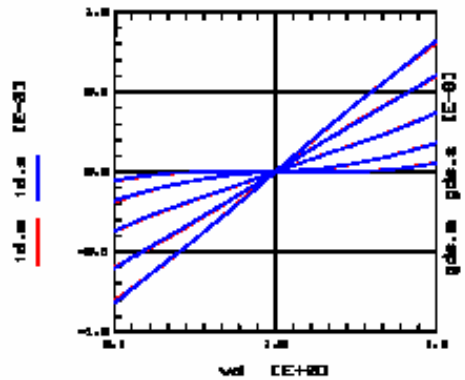
$$i_d - v_d$$

$$1^{st} \text{ deriv } \frac{\partial i_d}{\partial v_{ds}} - v_d$$

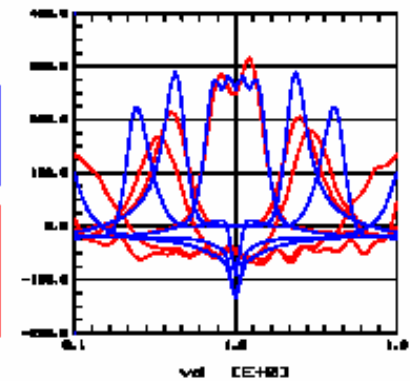
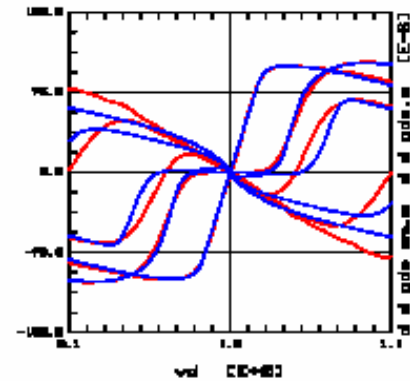
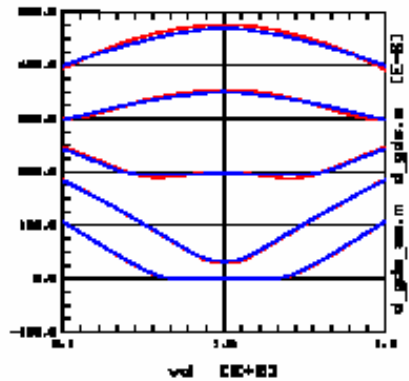
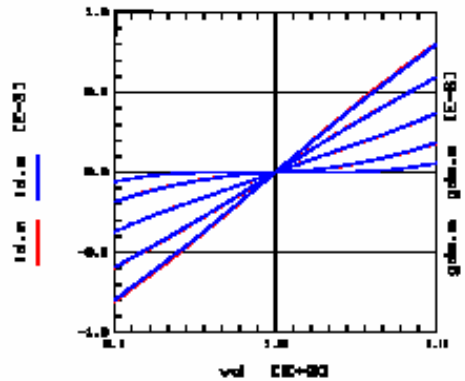
$$2^{nd} \text{ deriv } \frac{\partial^2 i_d}{\partial v_{ds}^2} - v_d$$

$$3^{rd} \text{ deriv } \frac{\partial^3 i_d}{\partial v_{ds}^3} - v_d$$

BSIM  
3v3



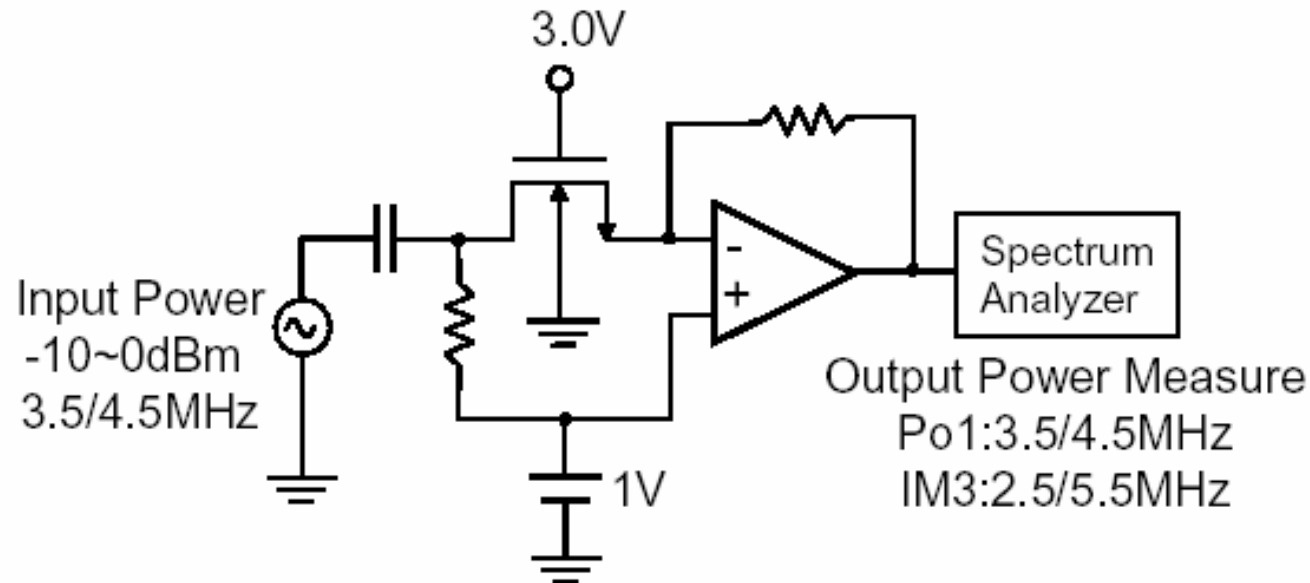
HiSIM  
2.3.1



HiSIM2.3.1 is in excellent agreement with measurement

# Evaluation of IM3 Characteristics (250nm CMOS)

- Model : BSIM3v3, HiSIM2.3.1
- Device : 0.25um NMOS(Low Vth) W/L = 8um / 4um
- Conditions :
  - Input : 3.5/4.5MHz 2-tone, Output : Po1 3.5/4.5MHz, IM3 : 2.5/5.5MHz
  - Simulation : Spectre-RF PSS Analysis

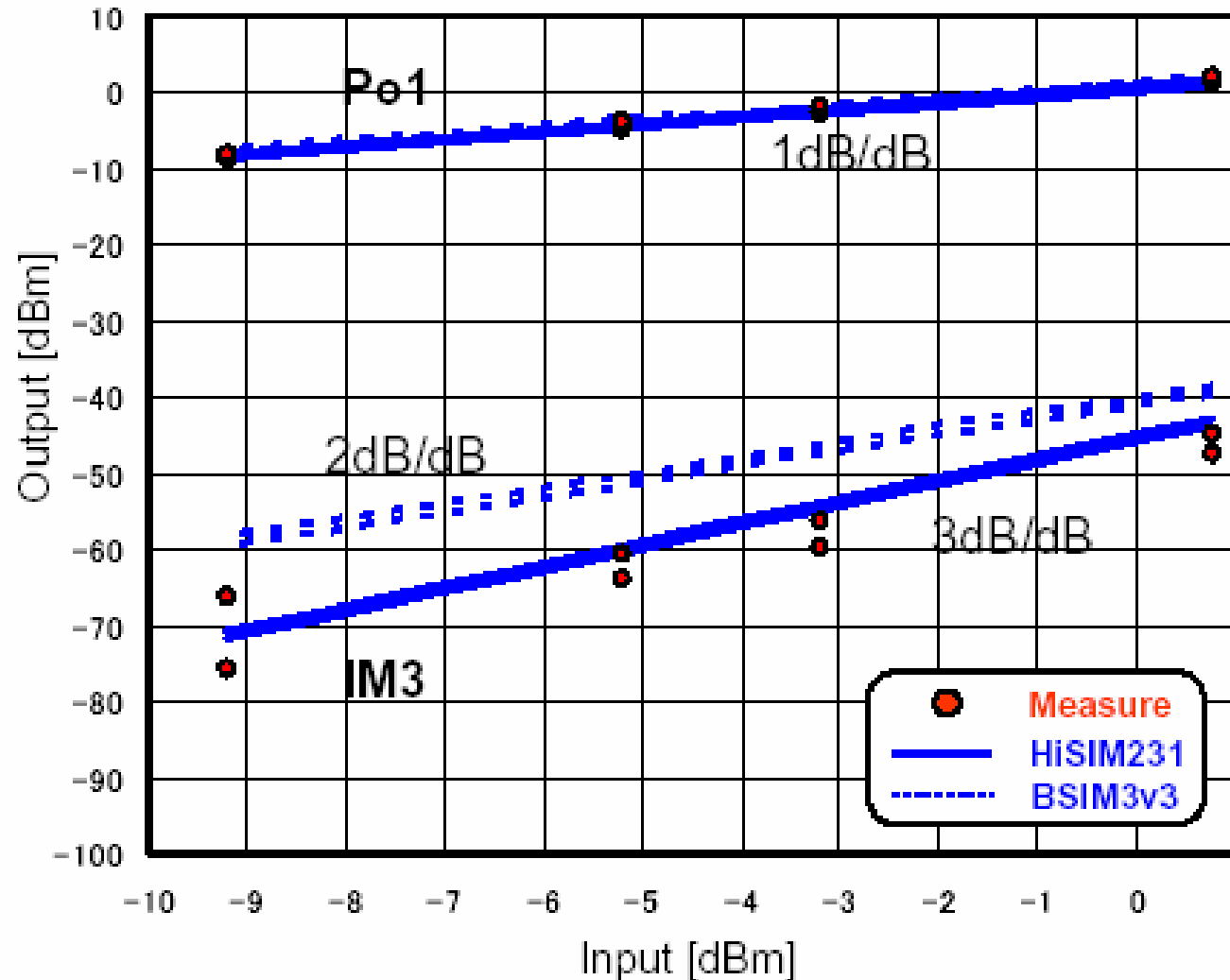


Source: Sony (HiSIM231)

# IM3 Simulation in Comparison to Measurement

$V_g=3.0V$

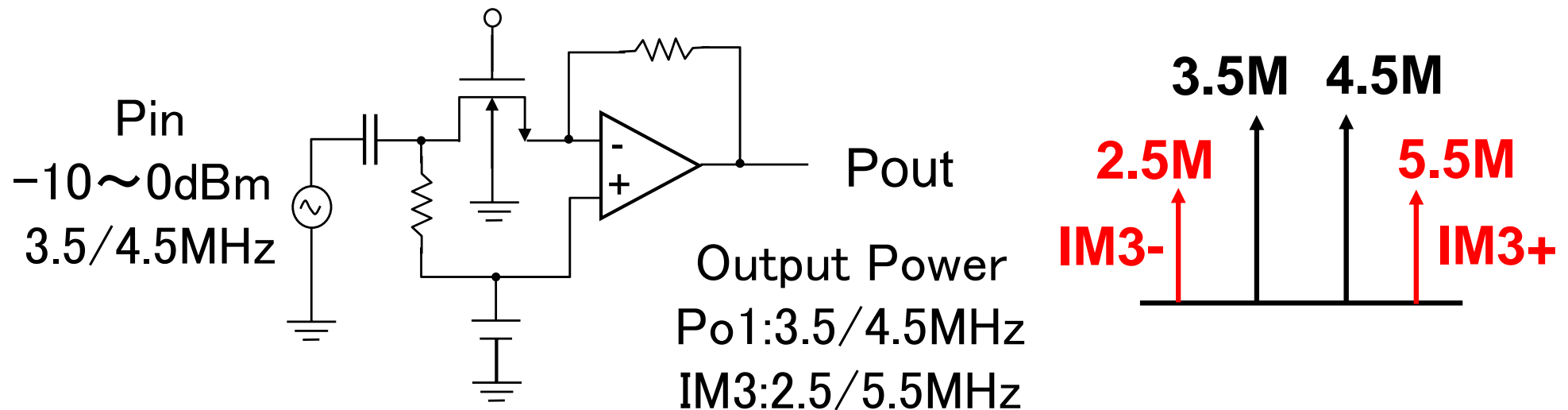
Source: Sony (HiSIM231)



Accurate reproduction of IM3 measurements with HiSIM

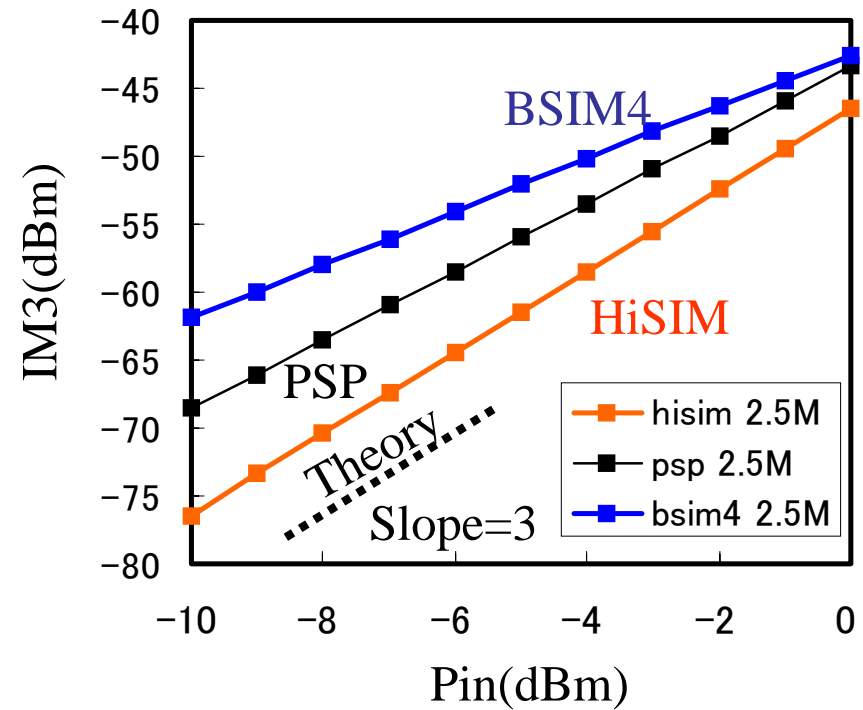
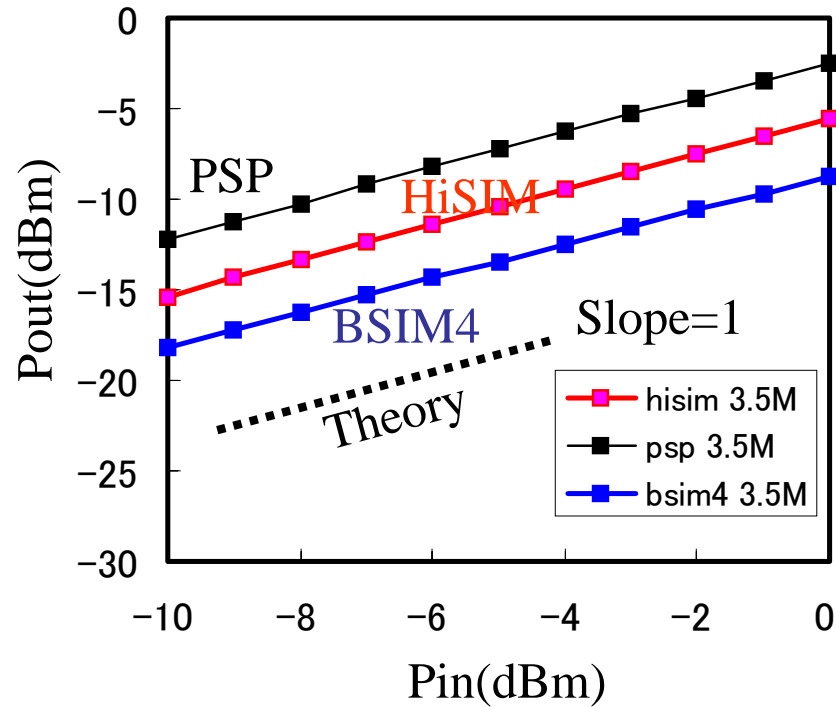
# Evaluation of IM3 Characteristics (90nm CMOS)

- Model: BSIM4, HiSIM2.3.1, PSP102
- Device: 90nm technology, NMOS transistor, W/L = 8um / 4um
- Simulation condition
  - Input: 3.5/4.5MHz 2-tone, Output: Po1 3.5/4.5MHz, IM3: 2.5/5.5MHz
  - Simulation: PSS analysis of Spectre-RF



Source: Toshiba

# IM3 Results for BSIM4, PSP102 and HiSIM2.3.1



## Slope in IM3 Analysis (90nm CMOS)

**BSIM4 : 2.0 (in large disagreement with theory)**

**PSP102 : 2.7 (in improved agreement with the theory)**

**HiSIM2.3 : 3 (in perfect agreement with the theory)**

Source: Toshiba

# 1/f-Noise Evaluation

## 1/f noise model of BSIM model

$$\begin{aligned}
 FN = & \frac{q^2 V_{tm} I_{ds}}{C_{ox} L_{eff}^2 J_{EF}} \times 10^8 \left\{ \text{Noia} \times \log \left( \frac{N_0 + 2 \times 10^{14}}{N_l + 2 \times 10^{14}} \right) - \text{Noib} (N_0 - N_l) + \frac{\text{Noic}}{2} (N_0^2 - N_l^2) \right\} \\
 & + \frac{V_{tm} I_{ds} \Delta L_{clm}}{W_{eff} L_{eff}^2 J_{EF}} \times 10^8 \times \frac{\text{Noia} + \text{Noib} \times N_l - \text{Noic} \times N_l^2}{(N_l + 2 \times 10^{14})^2}
 \end{aligned}$$

## 1/f noise model of HiSIM model

Very simple equation and high accuracy

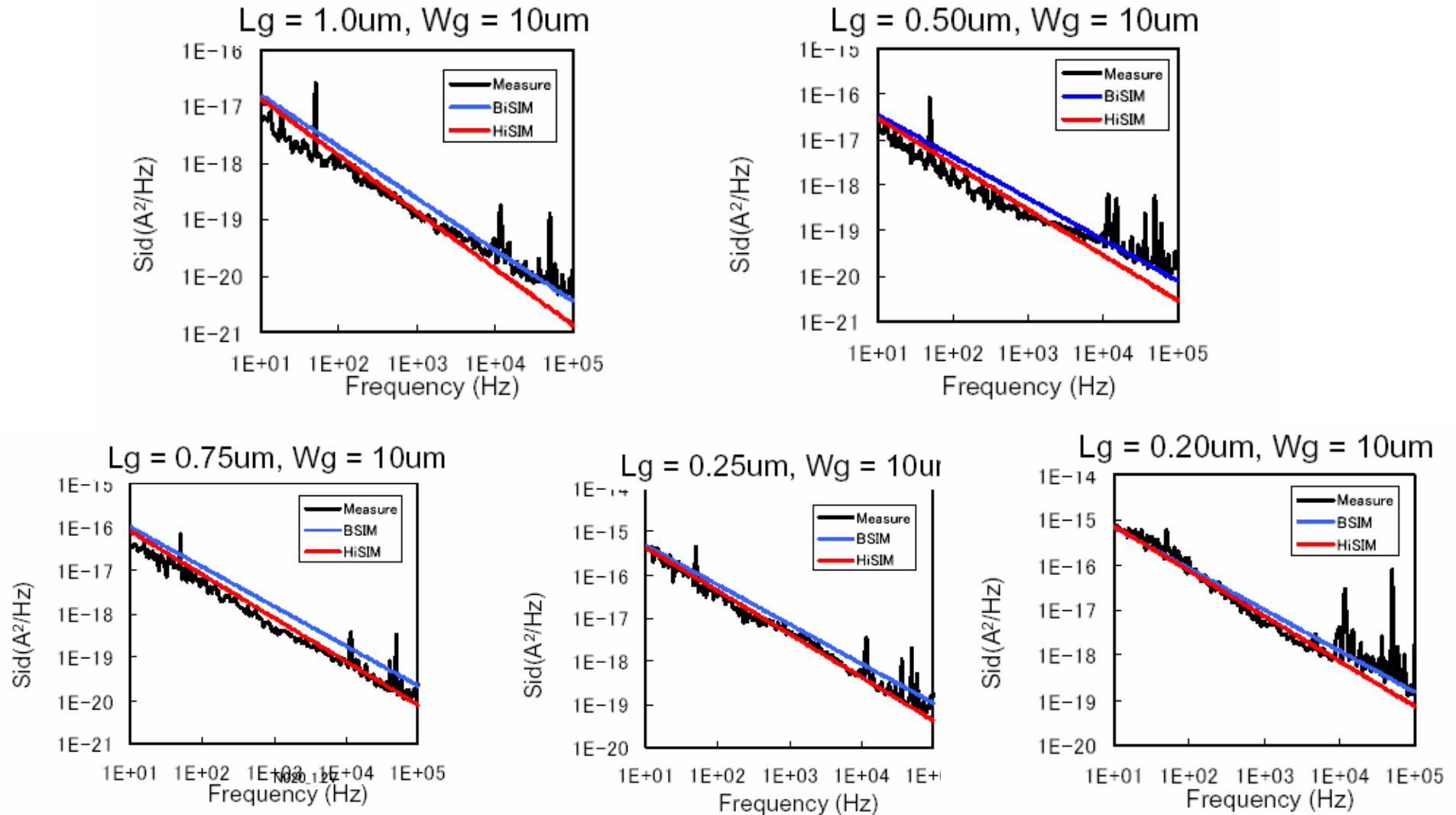
Mobility fluctuation

Trap density

$$S_{I_{ds}} = \frac{I_{ds}^2 \text{NFTRP}}{\beta f (L_{eff} - \Delta L) W_{eff}} \left[ \frac{1}{(N_0 + N^*)(N_L + N^*)} + \frac{2\mu E_0 \text{NFALP}}{N_L - N_0} \ln \left( \frac{N_L + N^*}{N_0 + N^*} \right) + (\mu E_0 \text{NFALP})^2 \right]$$

Source: Toshiba

# Simulation Results Compared with Measurements



Source: Toshiba (HiSIM2.3.1)

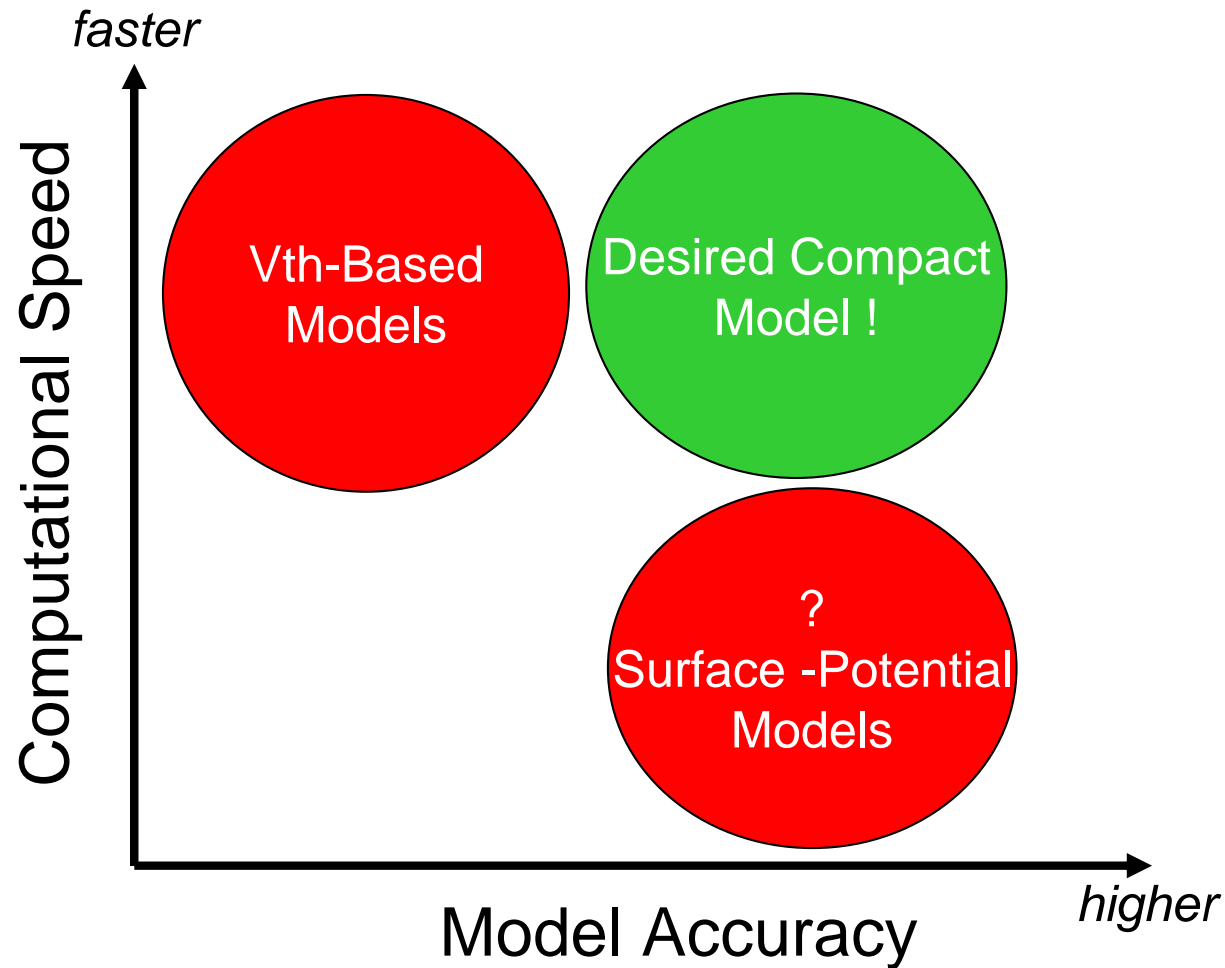
HiSIM2.3.1 accurately reproduces 1/f measurements

# Outline

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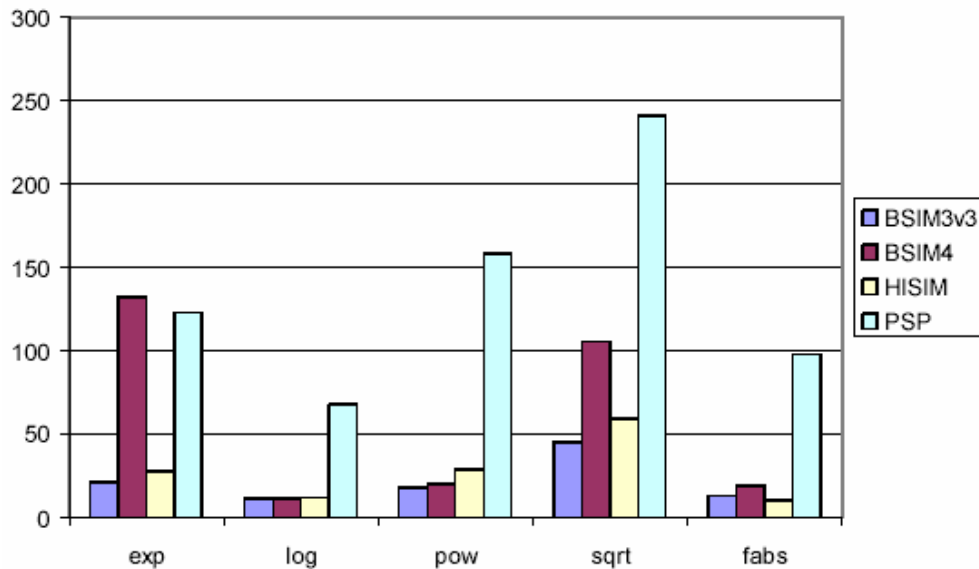
- Overview of Compact-Modeling Approaches
- Accuracy Aspects of HiSIM2.3.1 and 2.4.0
- **Speed Versus Accuracy Trade-Off and Position of Leading Compact Models**
- **Conclusion**

# Speed versus Accuracy Trade-Off

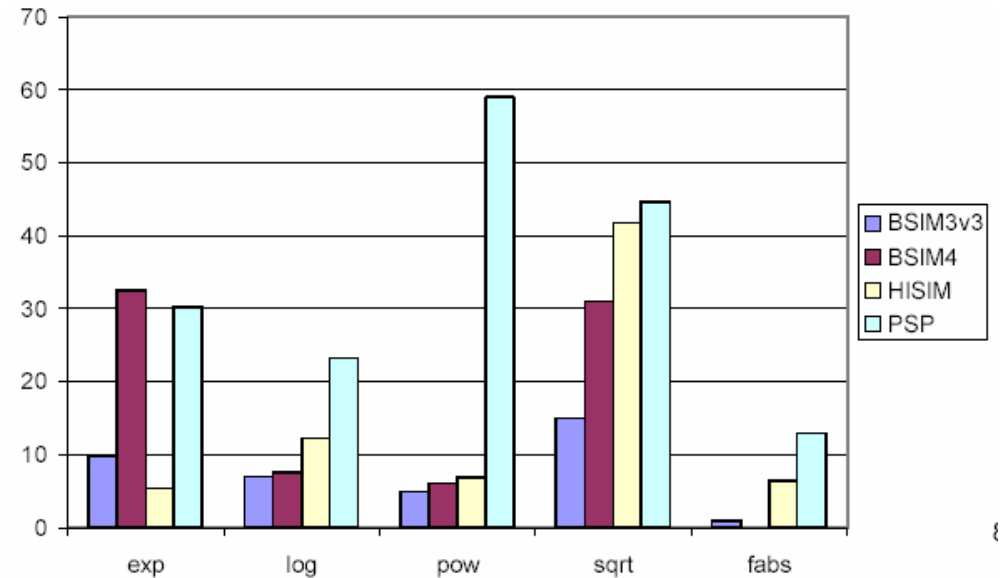


Is it possible to combine high speed and high accuracy to obtain an “ideal” MOSFET model ?

# High Cost Functions in the Source Code



Static Count of High Cost Functions  
(Complete Source Code)

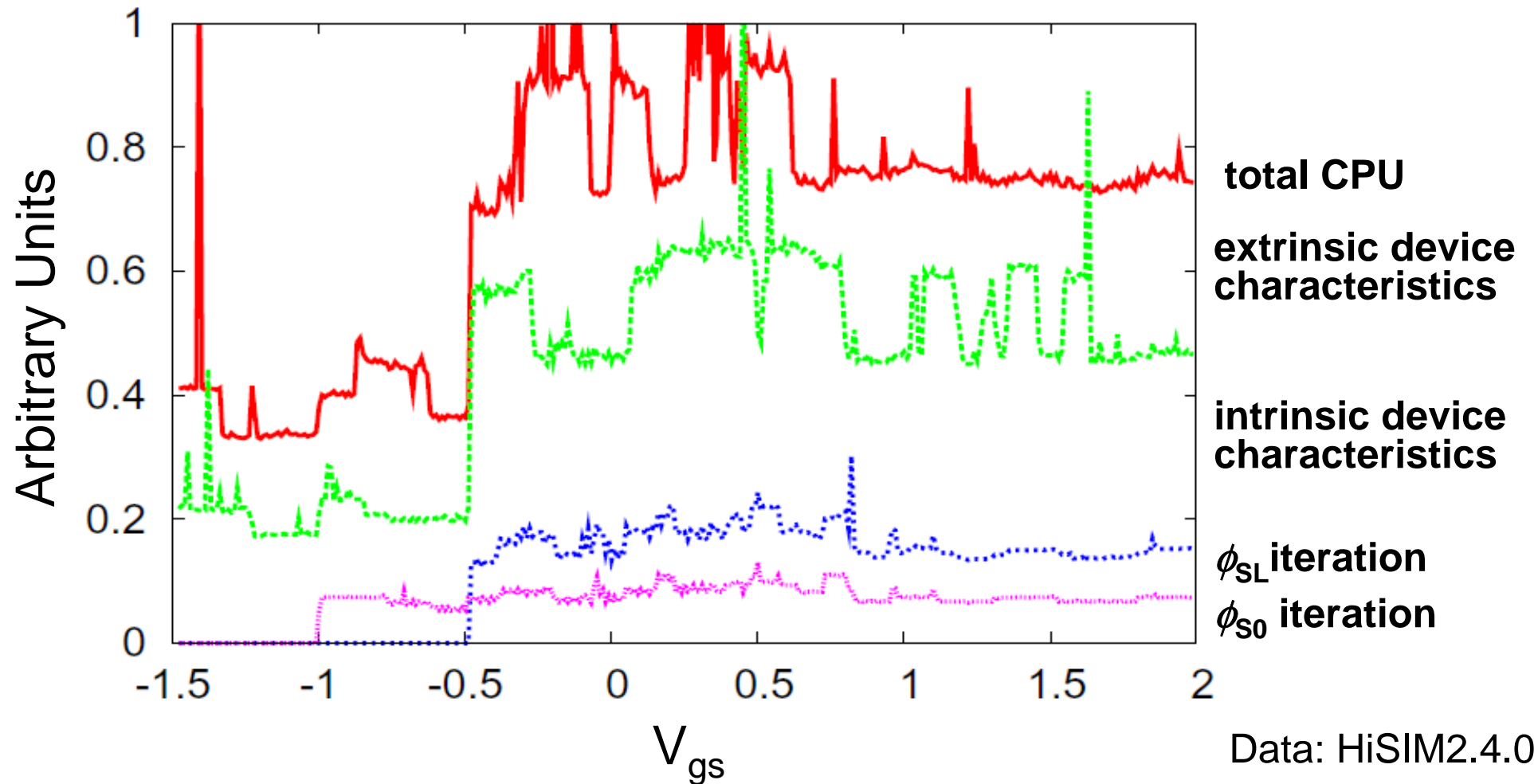


Dynamic Count of High Cost Functions  
(average of 9 different bias conditions)

Data Source: Silvaco, Oct. 2005

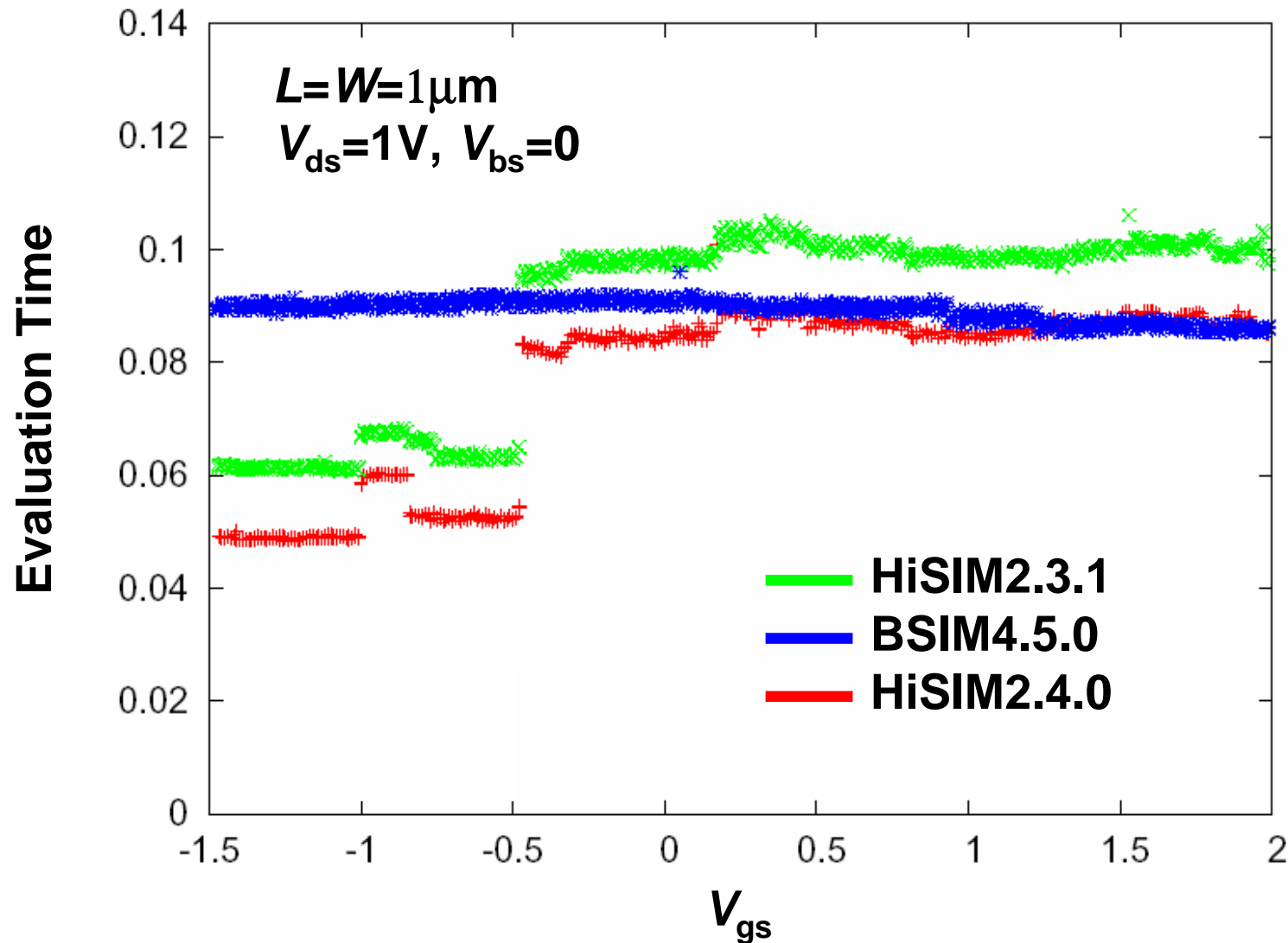
The number of high-cost functions in the HiSIM2 source code is not larger than for advanced Vth-based models.

# Breakdown of HiSIM's Model Evaluation Time



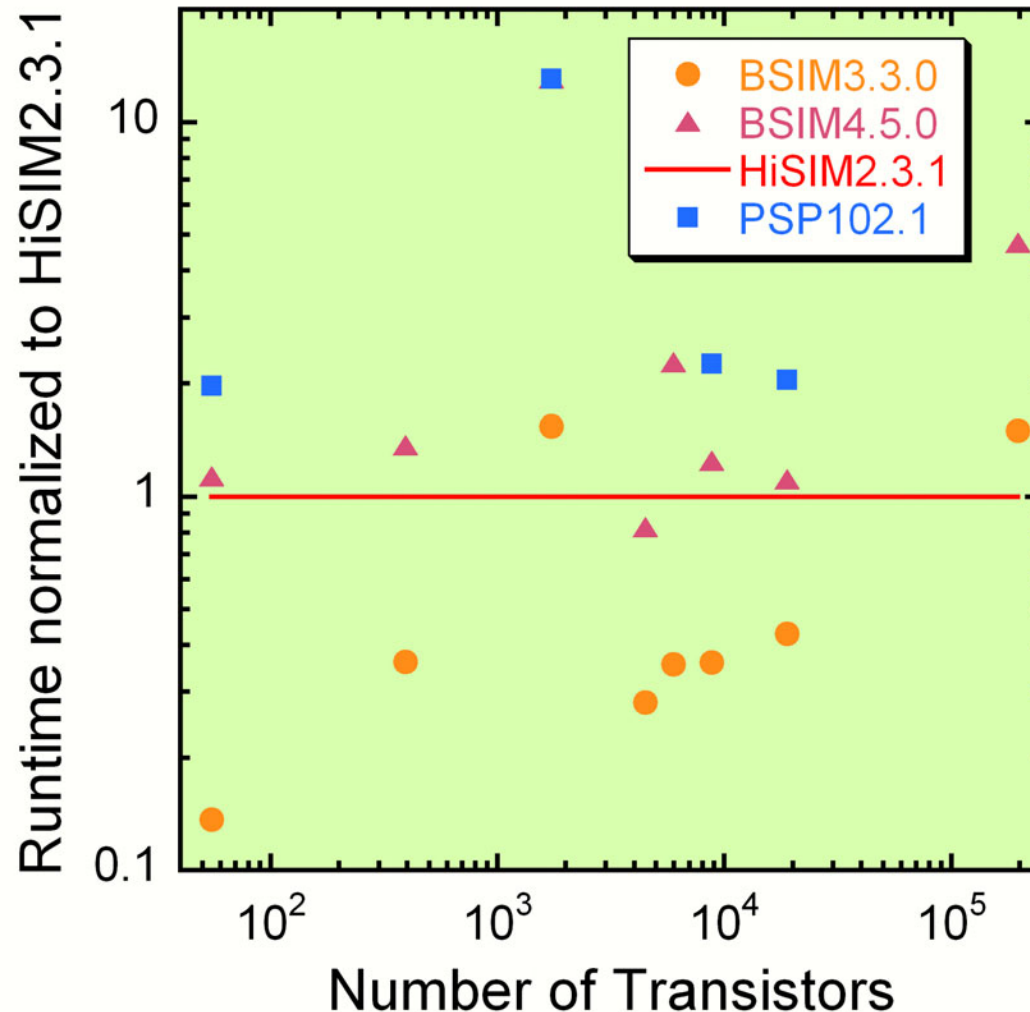
Iteration for surface-potential determination requires only a small fraction of the total model evaluation time.

# Model Evaluation Time Comparison



Model evaluation time of HiSIM2.4.0 is 20% improved and shorter than BSIM4.5.0.

# Runtime Comparison of Compact Models



## Simulated Circuit Types:

(90nm CMOS, productively used circuits)

ADC, Active Driver, PLL, I/O Module, VCO, DLL, Parity Checker, MUX Buffer

## Simulator:

SmartSpice 64bit, Version 3.3.0B

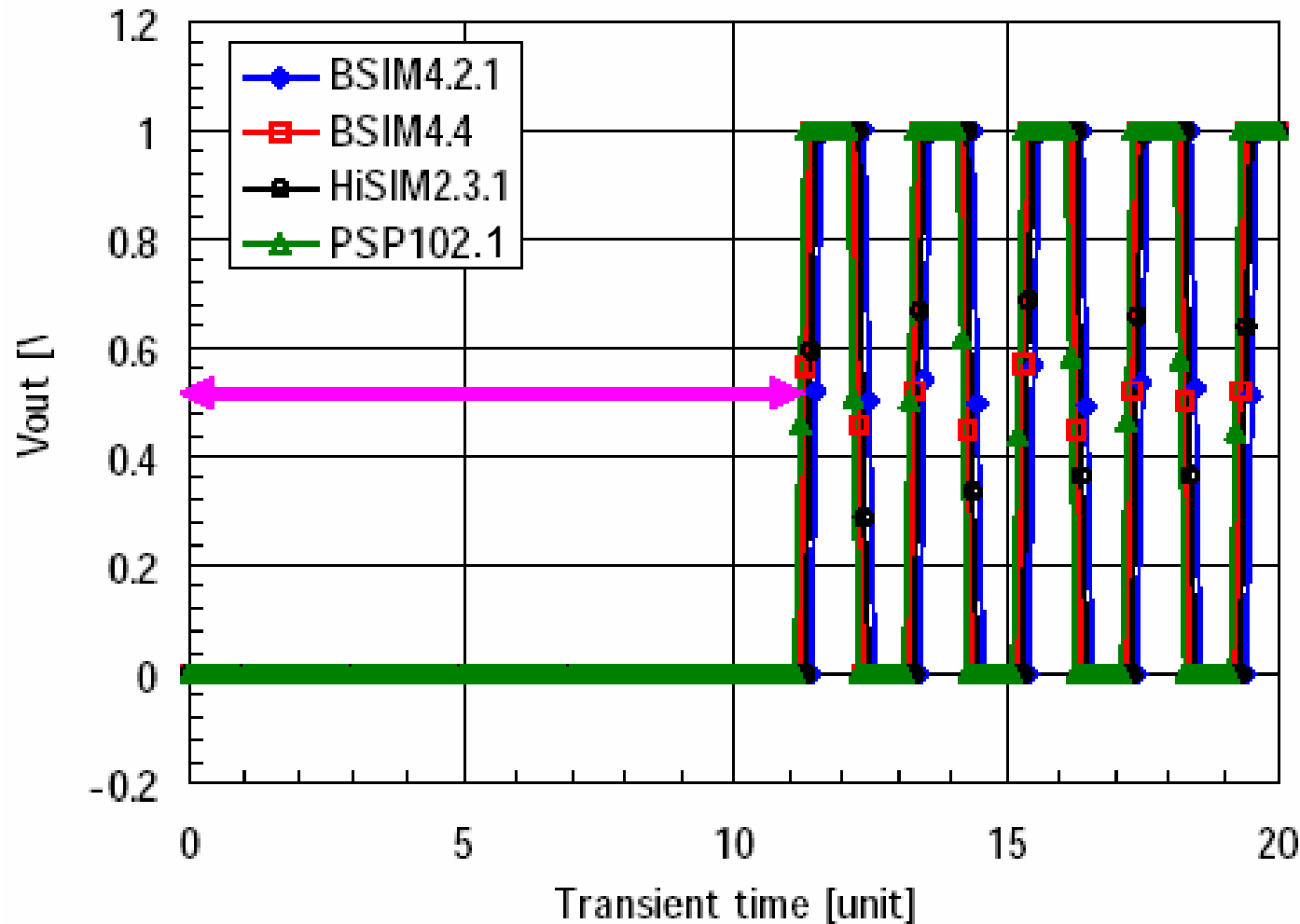
## Data Source:

Simucad, Dec. 2006

HiSIM2 executes faster than non-iterative surface-potential models as well as the latest Vth-based models.

# Runtime of Inverter Chains with Different Length

Vout of 512/512 inverter chain

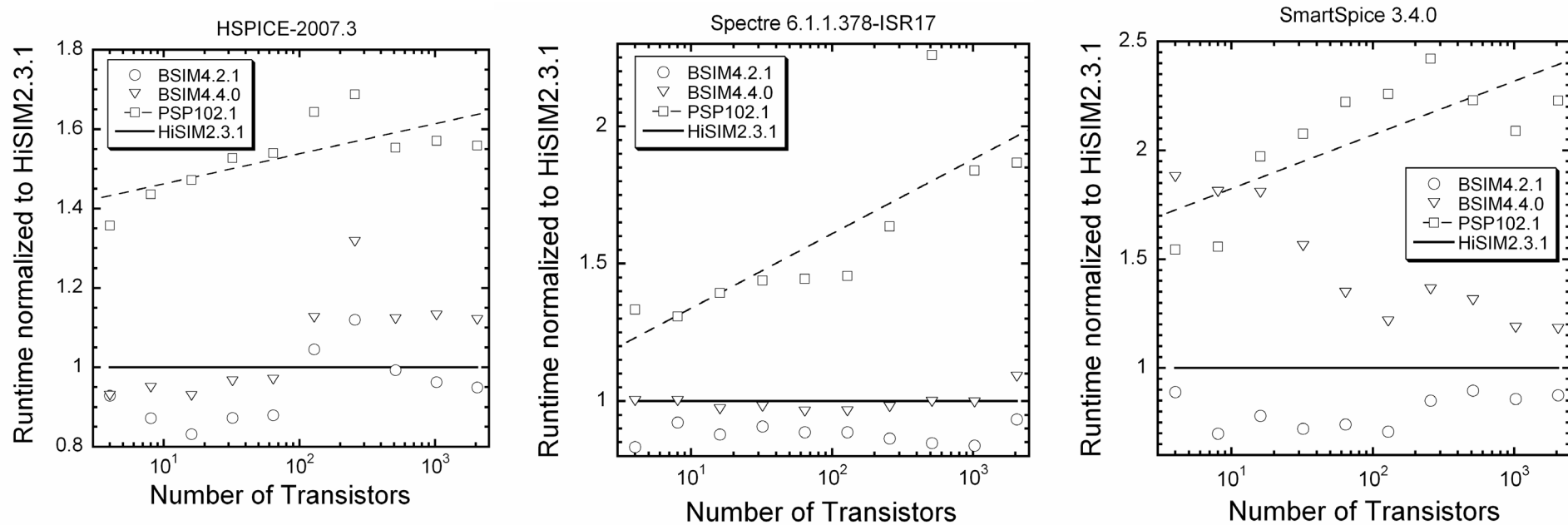


Source: NEC

Propagation delay times are equalized for all models.

# Runtime Comparison in 3 Different Simulators

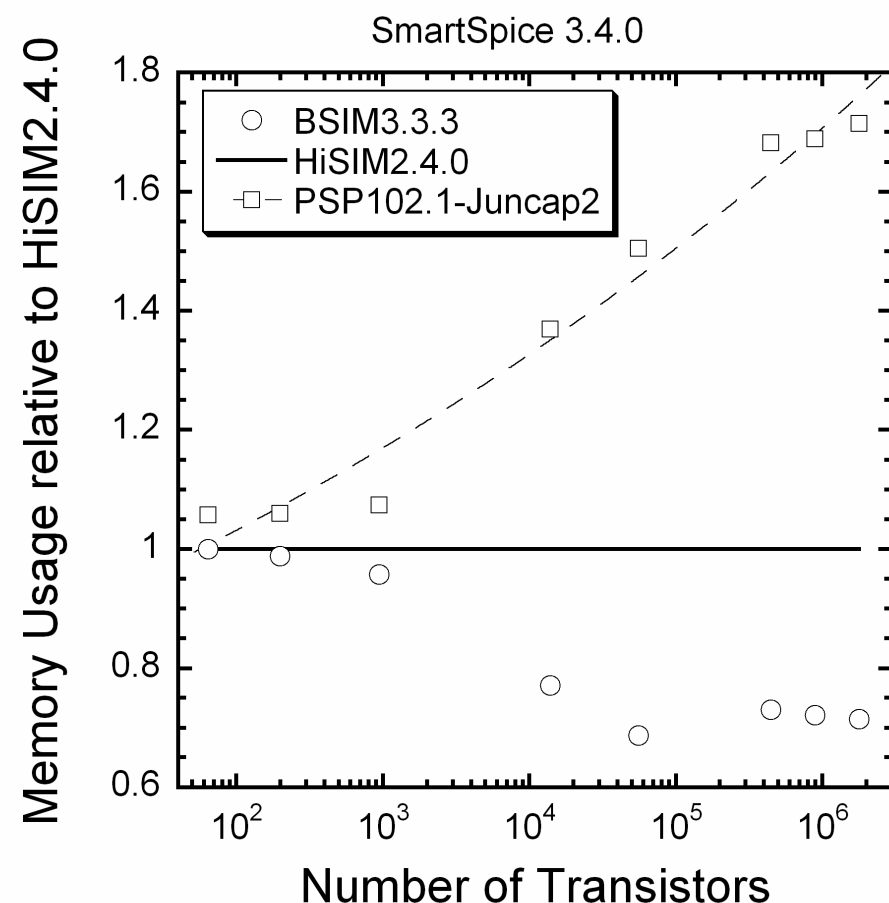
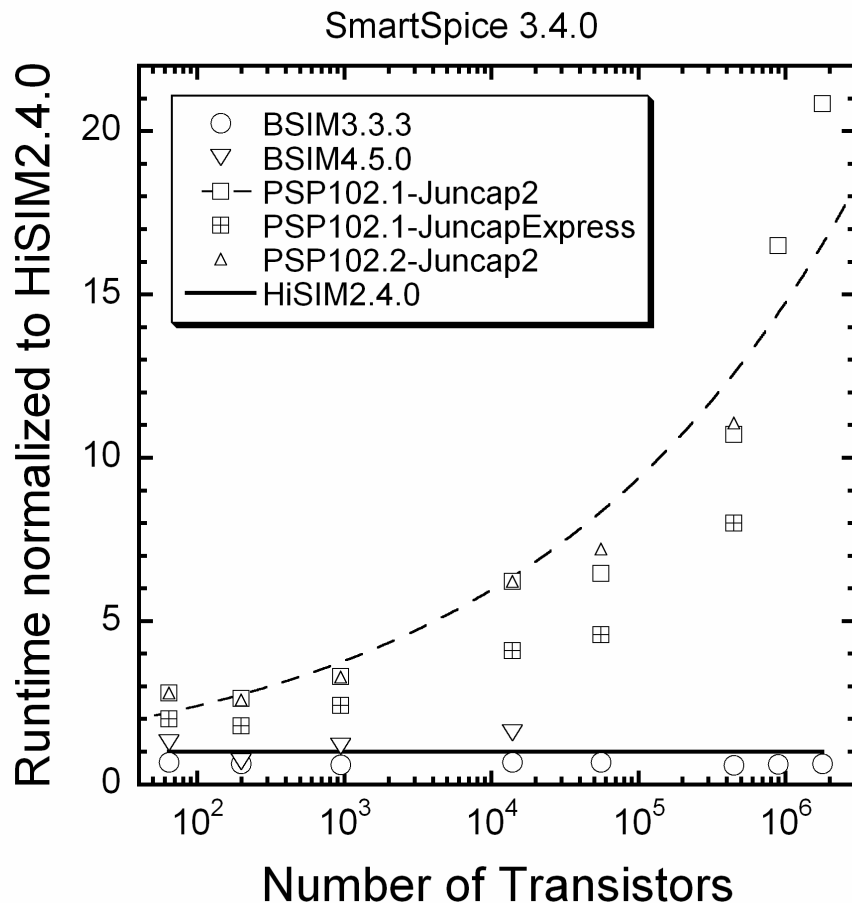
Inverter chains with up to 2024 transistors



Source: NEC

HiSIM2.3.1 computational runtimes are comparable to BSIM4. The relative runtimes of PSP102.1 consistently increase as a function of the transistor number.

# Computational Performance for Large Circuits



Source: Simucad

HiSIM2.4.0 is faster than BSIM4.5.0 and has comparable memory consumption. PSP runtimes increase strongly above 50K transistors.

# Large RF Circuit Simulation Performance

- Ran on Opteron with 8 2.8GHz CPU and RH.4 OS
- FineSim Spice v2007.03.01

## GHz PLL Pre-Layout

MOSFET – 3k  
Resistor – 0.05k  
Capacitor – 0.7k  
Vsource - 0.02k  
Fvco=M/N X Fref=GHz

Tran: 100us,  
TYP 1.0v, 25C

MOS Model	Relative Runtime Pre-Layout
<b>BSIM 4.21</b>	<b>1.28</b>
<b>HiSIM 231</b>	<b>1</b>

## GHz PLL Post-Layout

MOSFET - 4k  
Resistor - 150k  
Capacitor – 60k  
Vsource - 0.02k  
Fvco=M/N X Fref=GHz

Tran: 100us,  
TYP 1.0v, 25C

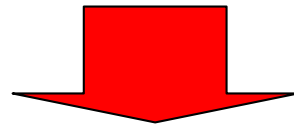
MOS Model	Relative Runtime Post-Layout
<b>BSIM 4.21</b>	<b>1.66</b>
<b>HiSIM 231</b>	<b>1</b>

Source: Magma

# Conclusion

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- HiSIM2.3.1 and 2.4.0 are a highly accurate MOSFET model based on the full iterative surface-potential concept.
- HiSIM2.3.1 and 2.4.0 have no runtime disadvantage in comparison to surface-potential models using a non-iterative approximation, but rather an advantage.
- HiSIM2.3.1 and 2.4.0 have even shorter computer runtime than the most advanced  $V_{th}$ -based models.



HiSIM2 (Versions 231 and 240) is a compact MOSFET model concept with optimized accuracy/speed trade-off