

IHP OpenPDK Roadmap



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Outline

- IHP in a nutshell
- Open source ASIC Development
- Motivation for IHP open PDK initiative
- Digital open source design flow
- Analog/RF open source design flow
- MPW Runs
- Interposer ADK
- Education: Certificate Courses @ IHP
- Contact us
- Acknowledgement

IHP in a nutshell

- IHP is the European research and innovation centre for silicon-based systems, ultrahigh-frequency circuits and technologies,
- Unique selling point of a 200mm pilot line for state-of-the-art BiCMOS technologies, operated under industry-like conditions, 24/7, for the provision of prototypes and low-volume production runs.
- Qualified technological platform with direct access for science and industry
- Vertical structure from material research to system architecture
- 350+ employees, 40+ nationalities



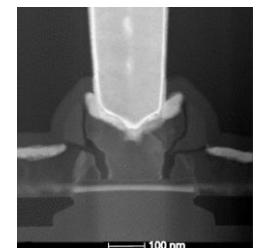
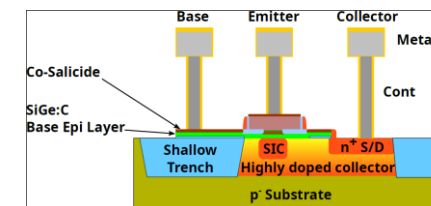
Vision

"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalized and networked world as well as for the sustainable preservation of our natural living conditions."

130nm SiGe BiCMOS Technologies

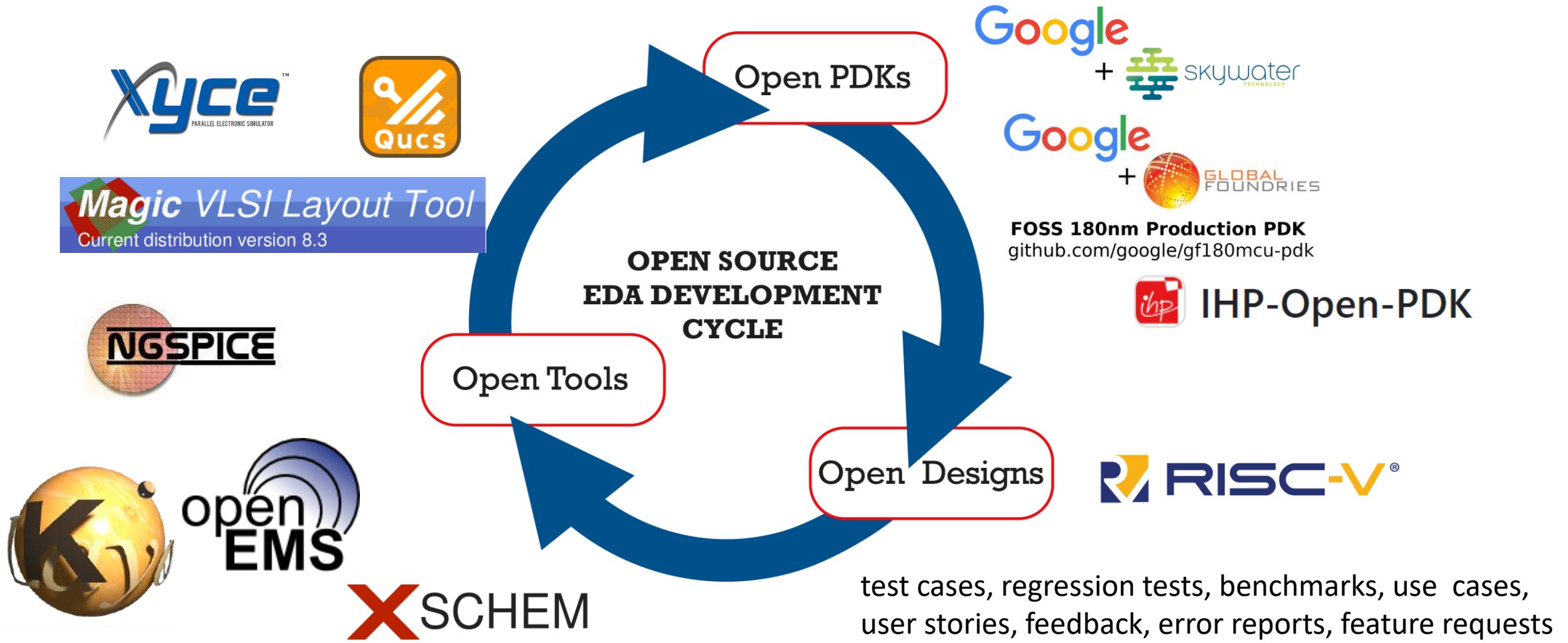
	SG13S	SG13G2	SG13G3Cu
HBT f_t/f_{max}	250 / 340 GHz	350 / 450 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CEO}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	2.1 fF / μm^2
Metallization	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	*Cu: 4 + 2 (3 μm) Al: 2 (3 μm)

- Target are high-end technology developments, low volume market introduction, technology transfer for potential mass production in commercial fabs
- SG13S & SG13G2 are qualified and ready for Low Volume of high end products
- SG13G3Cu is early access - qualification scheduled 2025



- SG13G2 technology was selected for the development of an open source PDK

Open source ASIC Development



Open Source in a Nutshell

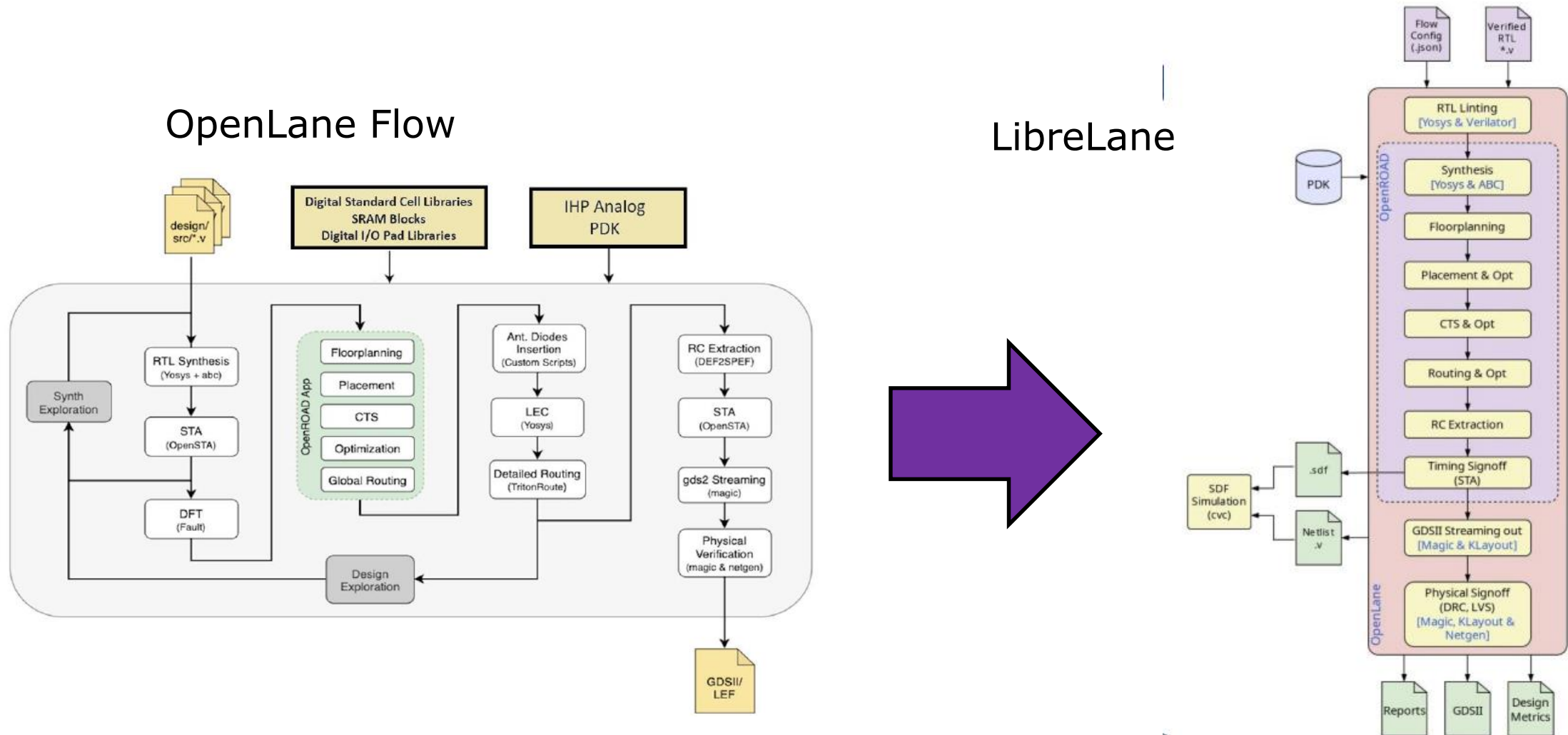
- Open-source - Open-access, exchange, collaboration, transparency on source code
- Benefits
 - No legal issues related to the NDA, ...
 - Collaboration, sharing efforts, enables re-use
 - Improves productivity, managing complexity
 - There is a lot of space for research
 - Lowers entry barriers
 - Promotes educations
- Open source does not mean for “free”
 - You can make money with open-source (Google Android, RedHat, ChatGPT)
 - Proprietary vs. open-source (NOT: commercial vs. open-source)



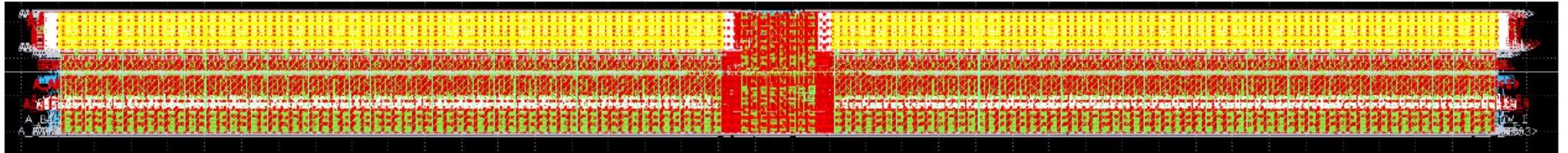
Motivation for IHP's open PDK initiative

- ❑ **Simplify access to education** materials for chip designers and to attract young people to get into chip design process
- ❑ Provide **low threshold (cost/technological) access to technology & PDK** for chip designer, academic projects
- ❑ Initiate cooperation's and joint projects with open source community
- ❑ **Be a pioneer** in demonstrating the possibilities of open source EDA
- ❑ software
- ❑ To **convince commercial fabs** to support the open source approach
- ❑ Support chip design possibilities for **advance IC design projects** by **StartUp, SMEs and companies**

Digital Open Source Design Flow

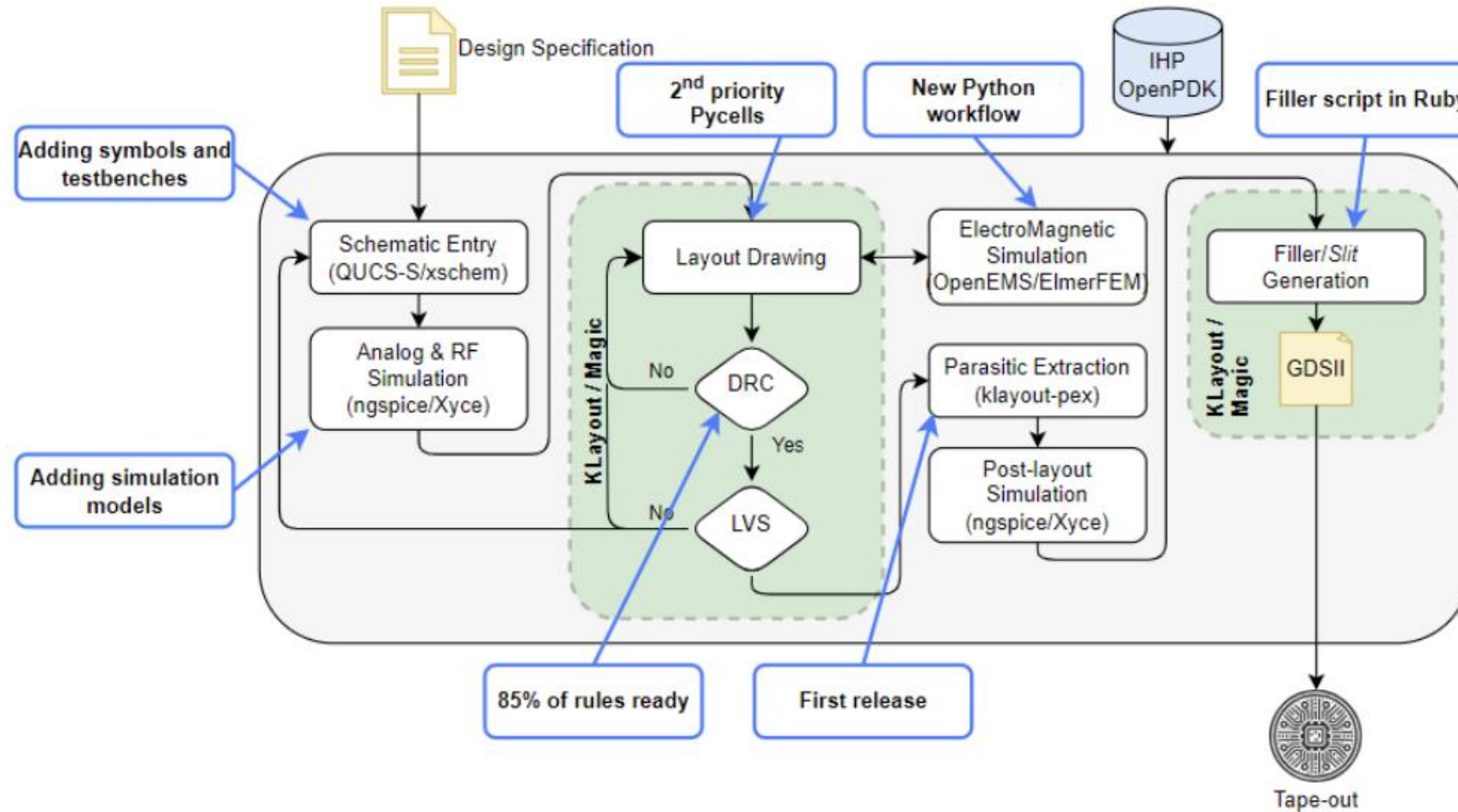


OpenPDK Digital cellsets



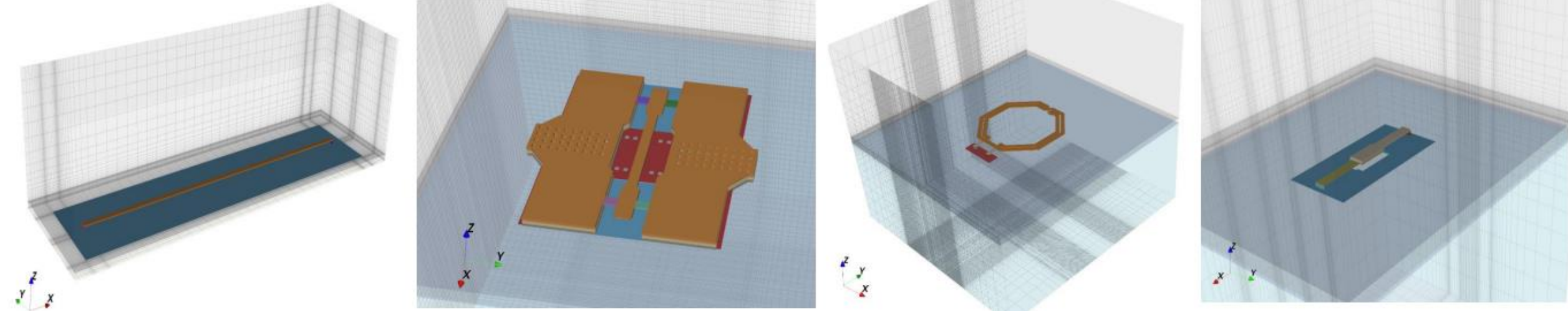
- Standard Cells
 - 84 cells
 - Sequential elements
 - Gated cells
- IO cells
 - In,Out, InOut, Analog
 - Different Drive strengths (4mA, 16mA, 30mA)
- SRAM
 - Hard macros of single port SRAM
 - Different sizes (1024x16, 1024x64, 1024x8, 2048x64, 256x48, 256x64, 4096x16, 4096x8, 512x64, 64x64)
 - SRAM generator

Analog/RF Open Source Design Flow



Magic VLSI, KLayout-PEX, Elmer FEM

OpenEMS new Python flow

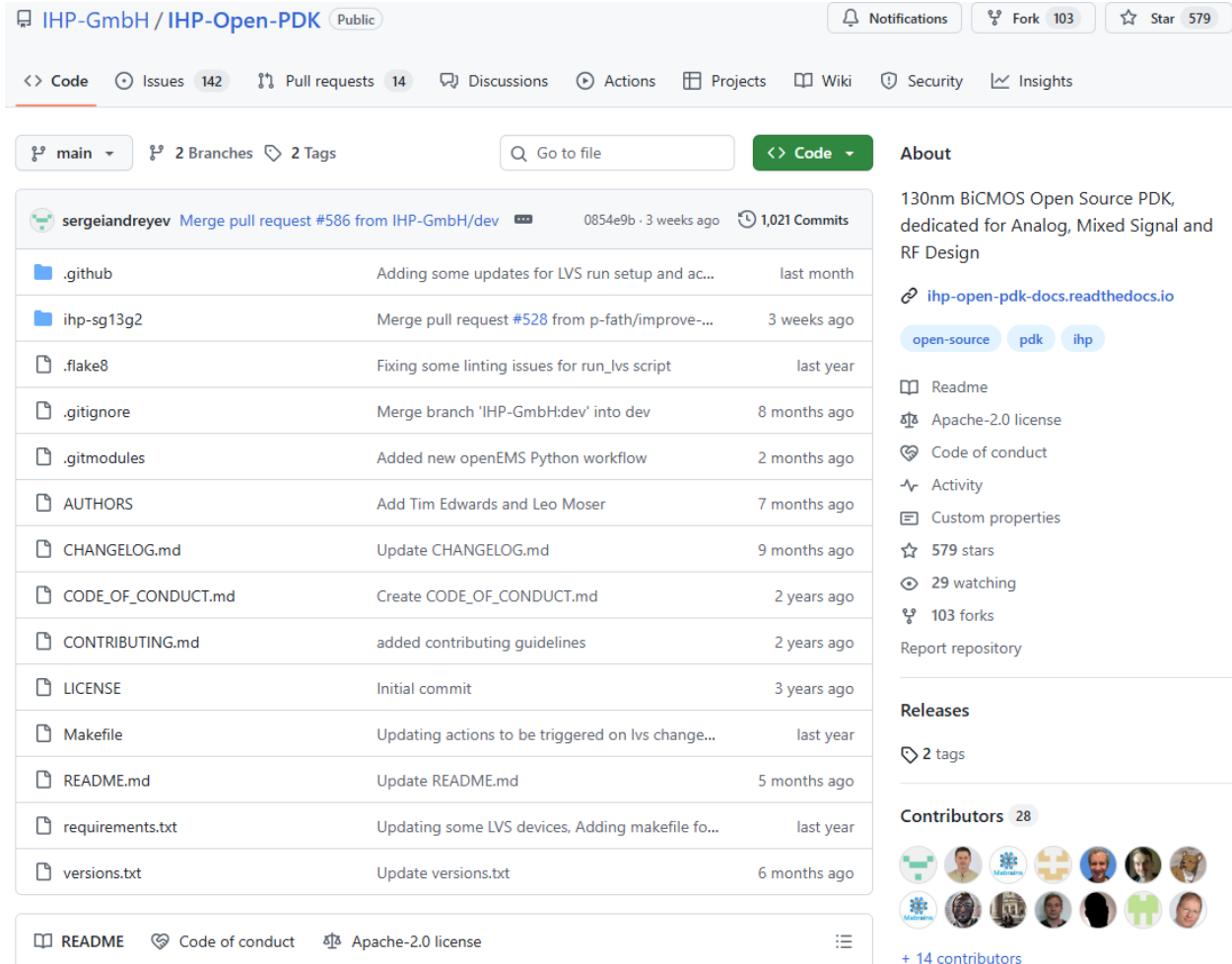


- ❑ Automatic mesh generation
- ❑ The model code can load files directly from GDSII
- ❑ Port (in plane or via port) are defined in GDSII file on special layers
- ❑ The technology stackup is read from an XML file
- ❑ Merging of via arrays is supported Touchstone SnP file output is supported

Work in progress analog mixed RF flow

- ❑ Parasitics Extraction PEX – first release
<https://github.com/martinjankoehler/klayout-pex>
- ❑ Qucs-S support – ongoing (primitive device symbols in XML format)
- ❑ DRC – 85% subset of rules available, new high performance implementation
- ❑ Klayout Pycells – ongoing (callbacks, devices, API, ...)
- ❑ OpenEMS integration for EM field solving
- ❑ Issues found, reported and fixed by community members!

OpenPDK Project on GitHub



The screenshot shows the GitHub repository page for IHP-Open-PDK. At the top, it indicates the repository is public and has 103 forks and 579 stars. The navigation bar includes links for Code, Issues (142), Pull requests (14), Discussions, Actions, Projects, Wiki, Security, and Insights. The repository is currently on the 'main' branch with 2 other branches and 2 tags. A search bar is available to go to a specific file. The file list on the left shows recent updates, such as 'Merge pull request #586 from IHP-GmbH/dev' and 'Adding some updates for LVS run setup and ac...'. The 'About' section on the right describes the project as a 130nm BiCMOS Open Source PDK, dedicated for Analog, Mixed Signal and RF Design. It provides a link to the documentation and lists tags like 'open-source', 'pdk', and 'ihp'. Other details include 579 stars, 29 watchers, 103 forks, and 2 tags. A 'Contributors' section shows 28 contributors.

Community involvement

Contributors 28



+ 14 contributors

Quite nice numbers

Issues 142 Pull requests 14

One year ago

Issues 20 Pull requests 1

IHP-Open-PDK GitHub repository, <https://github.com/IHP-GmbH/IHP-Open-PDK>, accessed: 2025-07-28.

IHP open source roadmap

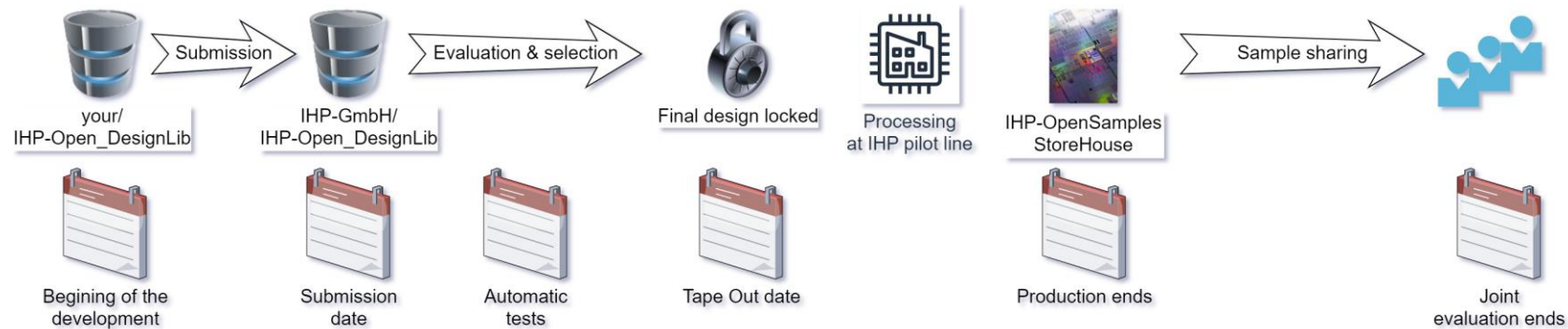
- DE:Sign – Design tools for sovereign chip development with open source:
 - DI-Flowspace (16ME0986k) – Radiation Hard Open Source PDK
 - DI-DEMICO (16ME0944) – Advanced Open Source RF Designs, improvement of openEMS EM simulator
 - DI-SIGN-HEP (16KIS2067K) – SRAM generator, OTP, RRAM
 - DI-OCDCpro (16ME0940) – Design challenge on secure designs
- New European projects:
 - APECS pilot line – Development of an open source interposer ADK
 - DECIDE – Development of EU design platform – Integration of open source offerings (PDKs, EDA tools, Design IP, design trainings)

Free MPW Runs

- The table provides schedule of MPW Runs for FMD-QNC project in 2024 and 2025

Tape out date	22/05/24	11/11/24	22/11/24	07/04/25	09/05/25	18/07/25	15/09/25
Technology	SG13G2	SG13CMOS	SG13G2	SG13G2	SG13G2	SG13G2	SG13CMOS
Area [mm ²]	10	220	20	140	30	30	220

For more details check: <https://ihp-open-ip.readthedocs.io/en/latest/>



****Project funds can be used exclusively to produce chip designs for non-economic activities, such as university education, research projects, and others**

Free MPW Runs – Free Samples from IHP Depot

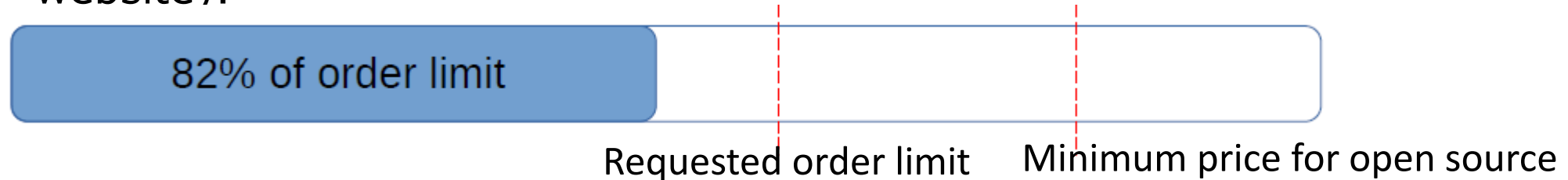
- ❑ Sample from free Runs stay IHP proprietary
- ❑ See latest documentation <https://ihp-open-ip.readthedocs.io/en/latest/>
- ❑ To hire samples you need to sign an agreement (AGREEMENT FOR HIRE OPEN IP SAMPLES) https://ihp-open-ip.readthedocs.io/en/latest/_downloads/c82c58426246cc84f3bbce282975b255/samples.rtf
- ❑ Hiring period can be several years, if you loose or break samples we need a written declaration, no penalty will occur
- ❑ Export and custom need to be considered outside of EU

Criteria for design IP selection from open community

- Mandatory criteria for IP selection
 - Completeness of IP data (all data need to be open source)
 - DRC error free designs
 - Area below 2 mm² preferred (larger designs only if area is available)
 - Potential export restrictions
- Additional criteria for IP selection
 - First time submission (preferred)
 - Design should use open source tools supported by IHP open PDK
 - For SG13G2 runs designs using SiGe (preferred)
 - Documentation quality
 - Uniqueness, not yet seen designs (i.e. if there were no ADCs before, an ADC design would get a higher point)

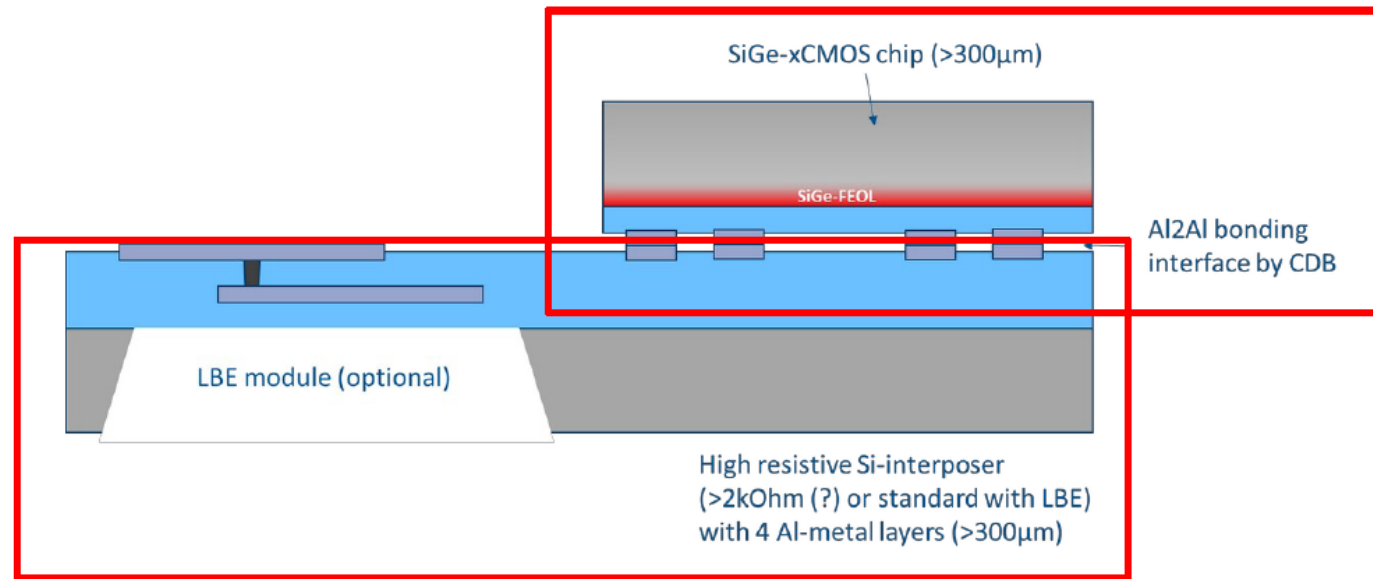
Concept open source MPW runs – 2026 and later

- 2 open source runs per year but only if enough requests (visualization on website):



- One SG13C run (Order limit appr. 100 mm²)
 - Proprietary - academic user 1500 €, industry user 2400 € (income to achieve order limit earlier and to reduce costs for open source)
 - IHP funding from internal projects
 - Order limit reduction via funding from IHP internal projects, may be **additional reduction via Europractice and/or sponsoring**
- One SG13G2 run
 - Proprietary - academic user open source user 3500 €, industry user 5800 €
 - Open source, Tiny Tapeout 3500 € down to 2400 €

Development of an open source interposer ADK



- SG13 based four metal interposer Based on 130nm Al BEOL (2 thin & 2thick) + MIM + TFR
- First test run 11th August 2025 (with Cu Pillar option)
- SiGe-BiCMOS – on – Interposer PDK for Dec. MPW 2025 (Al-Al bonding)

Education: Certificate Courses @ IHP



□ **Digital Design Course**

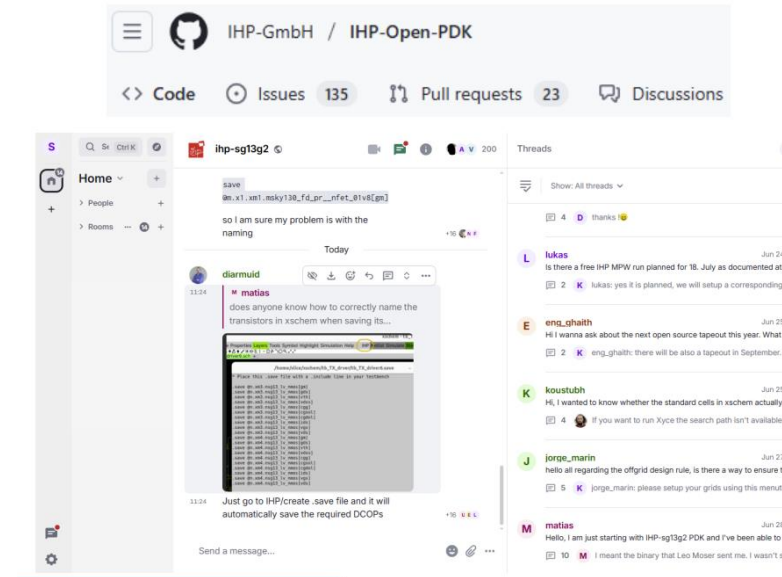
- Full RTL-to-GDSII workflow using OpenROAD and SG13G2 PDK
- Git-based, fully open-source: <https://github.com/OS-EDA/Course>
- Trial run Feb 2025: 15 on-site participants selected from 85+ applicants
- Feedback integrated via GitHub & live sessions

□ **Analog Design Course**

- Git-based, fully open-source: <https://github.com/IHP-GmbH/IHP-AnalogAcademy>
- Hands-on design with SG13G2 PDK
- Examined Designs: Bandgap, 50 GHz PA, SAR ADC
- Tools: Ngspice, Xyce, Xschem, Qucs, Klayout
- Strong emphasis on analog/RF practice – not an intro course
- Focus on layout, verification, and process variation analysis
- 16 on-site participants selected from 80+ applicants

How to reach us

- Email
 - openpdk@ihp-microelectronics.com
- GitHub
 - issues – for reporting issues, questions, requesting features
 - pull requests – for adding features ;)
 - discussions
- FOSSi Chat: Room ihp-sg13g2
 - area specific + general discussions
 - Announcements
- ChatGPT Chatbot
 - Information on technology, layout and process specifications



Acknowledgement

- Thanks to my colleagues at IHP and all the people involved in the development of the PDK
- Thanks to open source community SemiMod, ETH Zurich, Uni Linz, ChipFlow, Staf Verhaegen (PDKMaster), M. Koefflerlein (klayout), D.Warning, H. Vogt (ngspice), M. Brinson (Qucs-S), and many more ...
- And special thanks to the following public founded German projects:
 - VE-HEP (16KIS1339K) <https://elektronikforschung.de/projekte/ve-hep-1>
 - IHP Open130-G2 (16ME0852) <https://www.elektronikforschung.de/projekte/ihpopen130-g2>
 - FMD-QNC (16ME0831) <https://www.elektronikforschung.de/projekte/fmd-qnc>