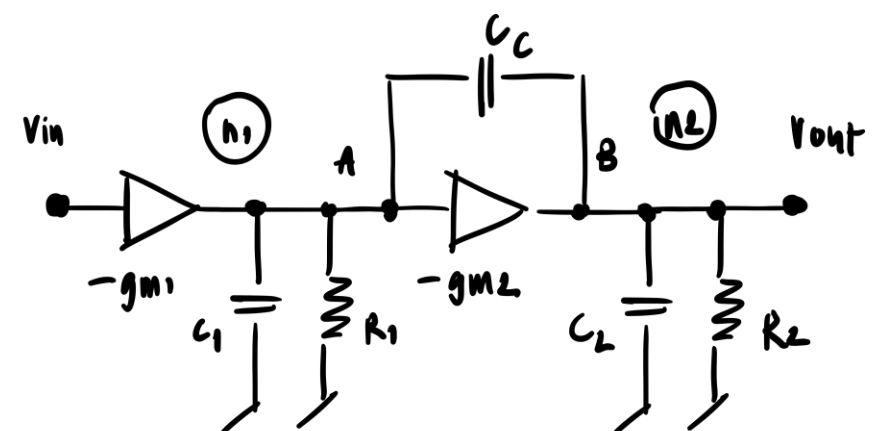
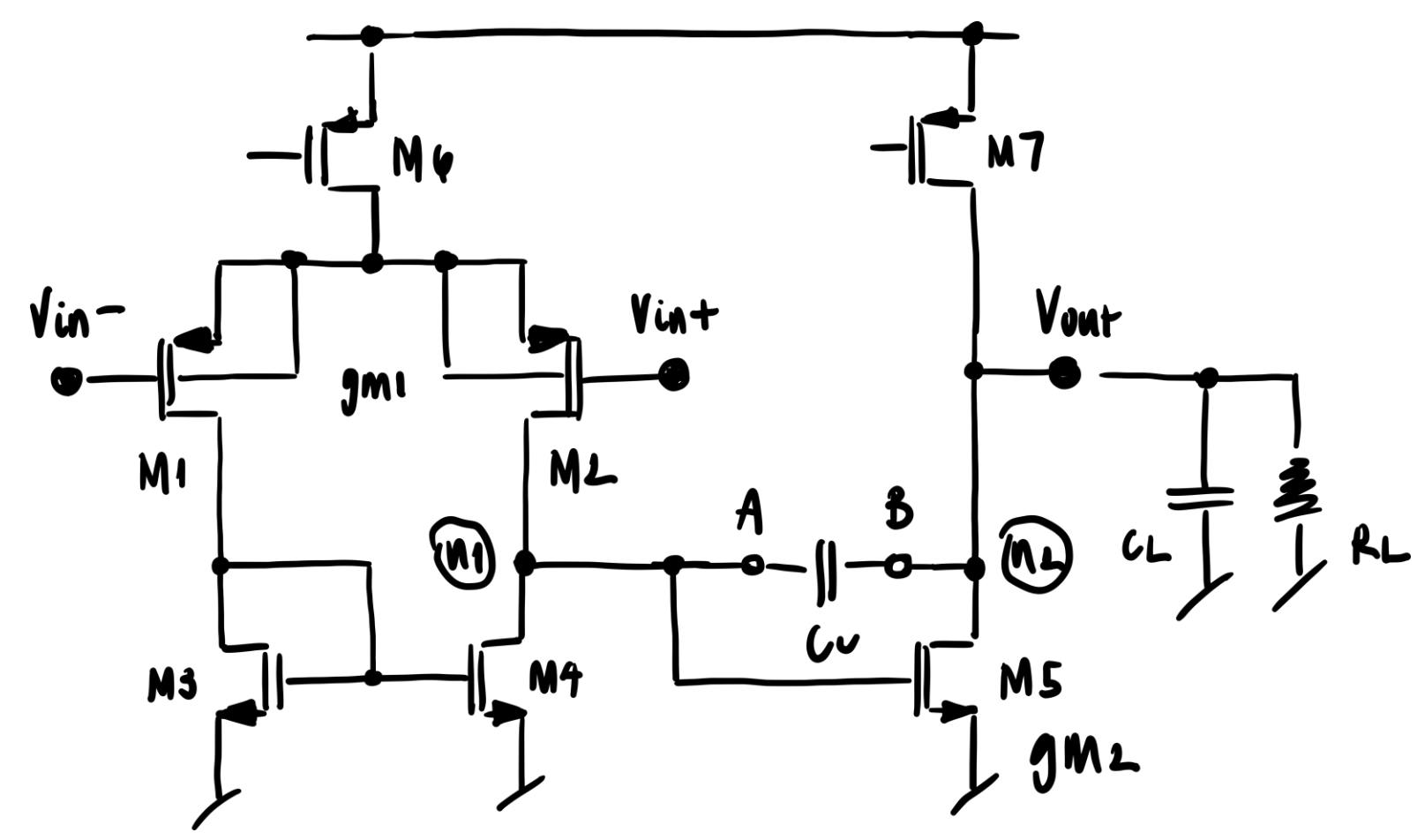


# MOS Sizing Tool

Single Transistor Simulator

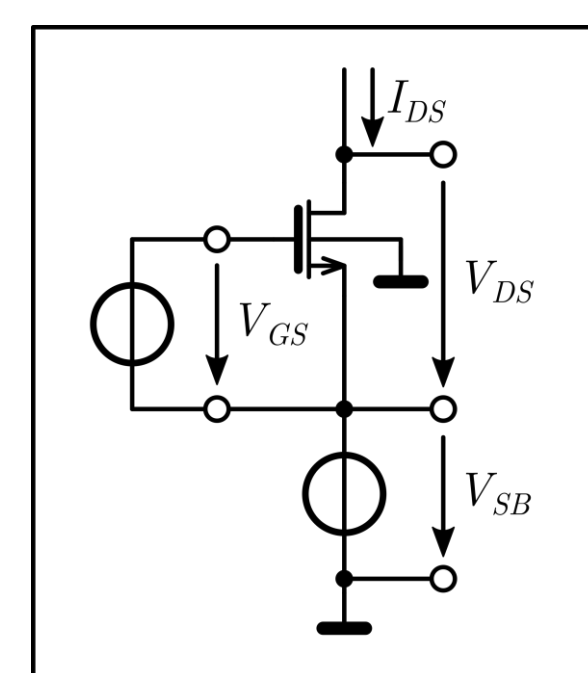
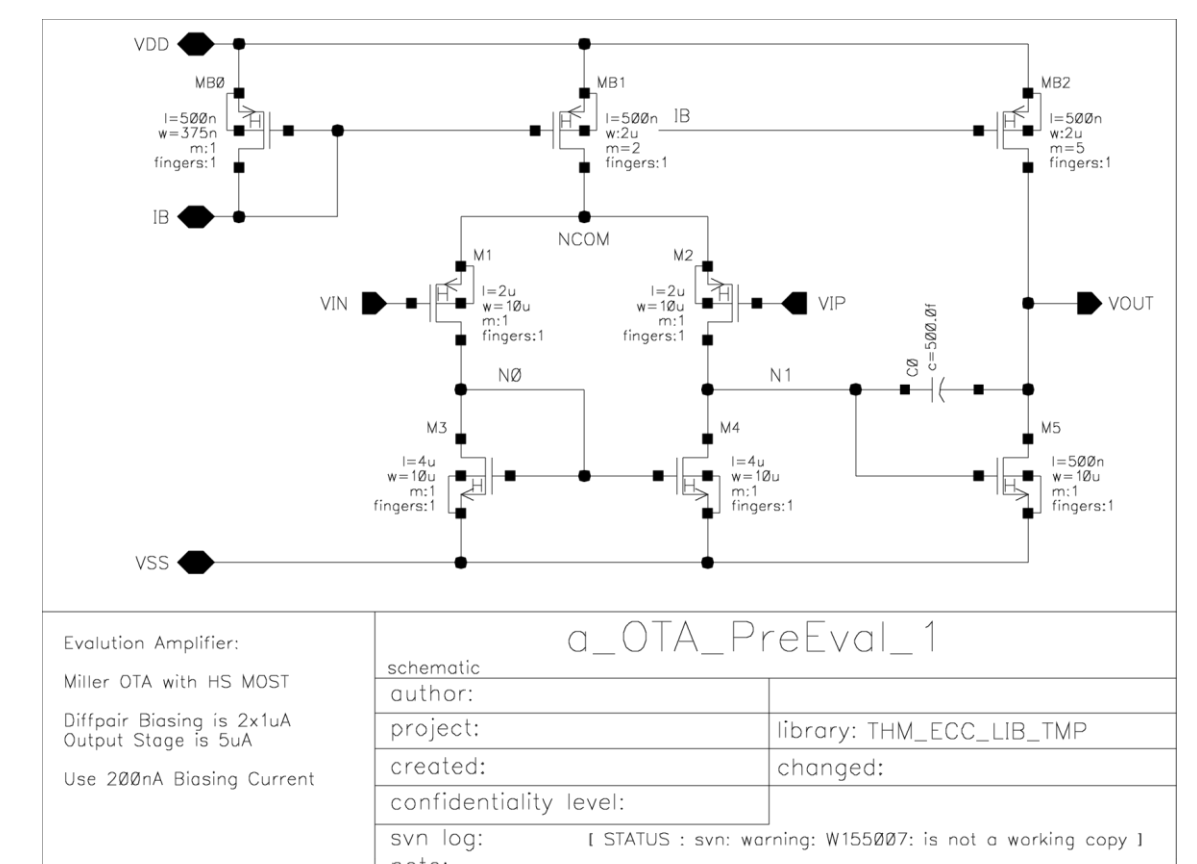
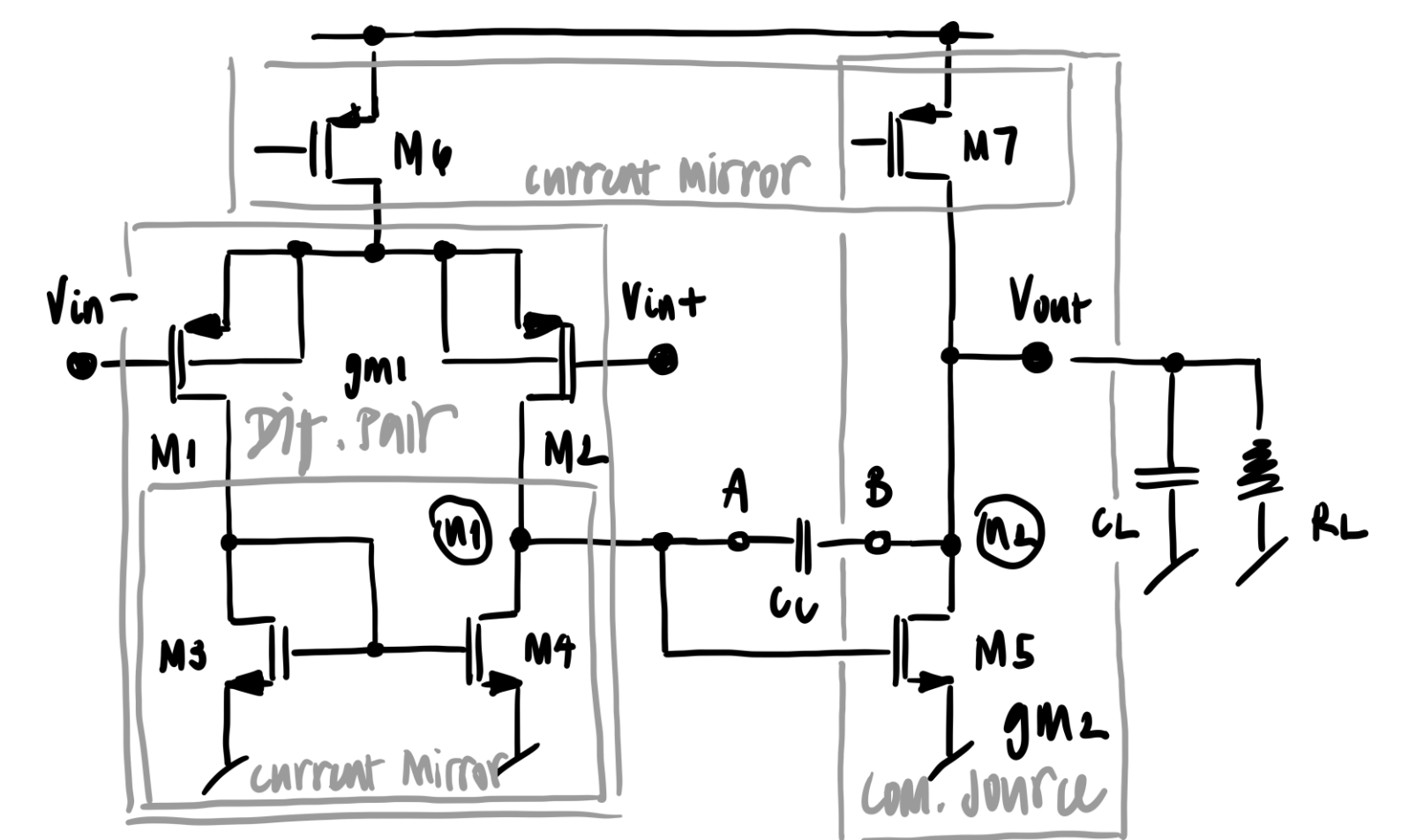


## Support of Natural Design Flow



$$AV(s) = \frac{A_0 (1 - \frac{sC_L}{g_{mL}})}{(1 + j \frac{sC_L}{g_{m1}}) (1 + s \frac{C_L C_L + C_L (C_1 + C_2)}{g_{mL} C_C})}; A_0 = R_L R_L g_{m1} g_{mL}$$

- Topology selection
- Circuit analysis
- Specifications (application) to secondary specifications ( $A_0, f_{UG}, f_p, g_m, g_{ds}, \dots$ )
- Macro block sizing
- Estimation of  $V_{dsat}$  and  $V_{DS}$
- Adjustment of  $V_{dsat}$  and  $g_m$ 's according specifications
- Schematic verification



Solution for DC, AC, and NZ

**Results**

DC-Solution: (saturation region)

vgs = 1.500000 V	vds = 1.500000 V	vgd = 0.000000 V
vgb = 1.500000 V	vdb = 1.500000 V	vsb = 0.000000 V
ids = 40.012618 uA	vth = 667.360742 mV	vdsat = 506.702830 mV
ibs = -1.006037 nA	ibd = -1.716521 nA	ig = 0.000000 A
ron = 37.488174 kohm	A0 = 24.470500	

AC-Solution:

gm = 75.031838 uS	gds = 3.066216 uS	rds = 326.134891 kohm
gmb = 14.803253 uS	gbs = 9.208814 aS	gbd = 1.000000 aS
gs = 366.935813 mS	gd = 366.935813 mS	gm/id = 1.875204 1/V
cgs = 724.385080 aF	cgd = 129.427643 aF	
cgb = 116.808242 aF	cbs = 412.882777 aF	cbd = 205.122087 aF
fp = 571.557947 MHz	ft = 13.986309 GHz	fz = 92.265364 GHz

NZ-Solution:

Frequency	1 Hz	1 kHz	1 MHz	(fkn = 222.989 MHz)
Vn(thermal)	14.848 n	14.848 n	14.848 n	[V/sqrt(Hz)]
Vn(1/f)	91.314 u	3.972 u	172.758 n	[V/sqrt(Hz)]
Vn(shot)	0.000	0.000	0.000	[V/sqrt(Hz)]
Vn(tot)	91.314 u	3.972 u	173.395 n	[V/sqrt(Hz)]
A(f)	24.471	24.471	24.470	[-]

Technology Settings & Tools

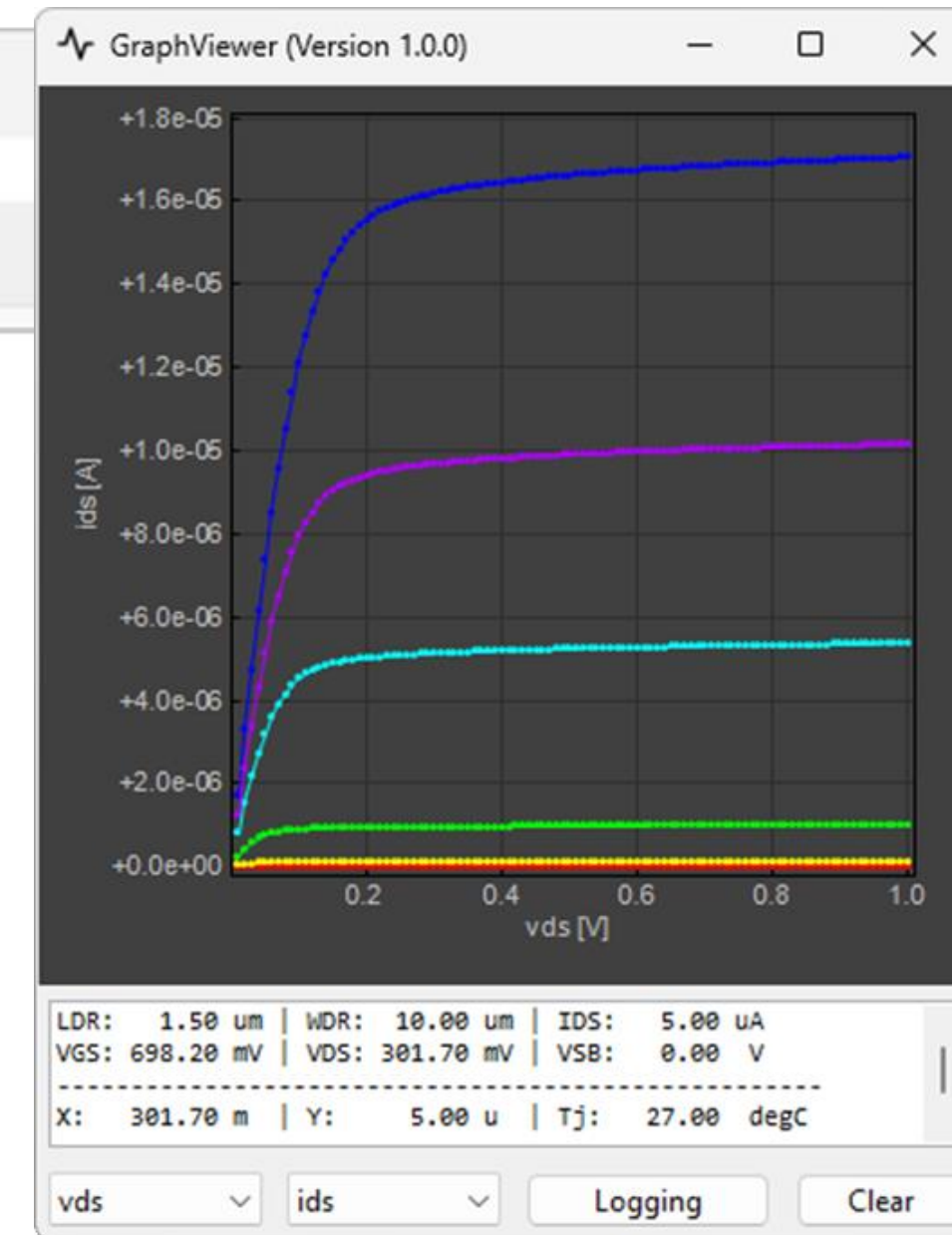
Process Technology Settings: AnalogMOS mos33, nmos

VCC min/max [V]: 0.0000, 3.6300

Corners and Temperatures [°C]: FAST(FAST), FAST(FAST), FAST(FAST); FAST(SLOW), FAST(SLOW), FAST(SLOW); TYP, TYP, TYP; SLOW(FAST), SLOW(FAST), SLOW(FAST); SLOW(SLOW), SLOW(SLOW), SLOW(SLOW); -45.0, 27.0, 125.0

MOS Transistor Biasing: Voltage VGS [V]: 1.5000; Voltage VDS [V]: 1.5000; Voltage VSB [V]: -0.0000; Current IDS [uA]: 40.0126; VSB to GND: checked; VDS to VGS: unchecked

MOS Transistor Sizing: Width WDR [um]: 0.5000; Length LDR [um]: 0.5000; Lock Aspect Rat.: unchecked; Lock IDS/W [A/m]: unchecked; Multiplier: 1



Biasing Condition

$$V_{GS} = f(V_{DS}, I_{DS}, V_{SB})$$

$$V_{DS} = f(V_{GS}, I_{DS}, V_{SB})$$

$$I_{DS} = f(V_{DS}, V_{GS}, V_{SB})$$

Diode Connection ( $V_{DS} = V_{GS}$ )

Transistor Dimensions

Process Technology

Available Process Corners

Corner Temperature

## General Remark on Transistor Sizing

Current density  $I_{DS}/W$  design procedure

The (main) purpose of a MOST is to make gain, hence, large  $g_m$  and small  $g_{ds}$ .

$$I_{DS} \approx K \frac{W}{L} V_{dsat}^2, \text{ hence, } V_{dsat} \approx \sqrt{\frac{I_{DS}}{W}} \frac{1}{\sqrt{K}} \sqrt{L}$$

- choose "reasonable" current density  $I_{DS}/W$
- adjust  $V_{dsat}$  with  $L \rightarrow V_{dsat}$  and  $V_{ds}$  sets  $g_{ds}$
- adjust  $g_m$  with  $I_{DS}/W$

(with  $V_{dsat}$  fixed, also  $\omega_T = \mu V_{dsat}/L^2$  is fixed, and  $I_{DS}/g_m = V_{dsat}/2$  fixed)

