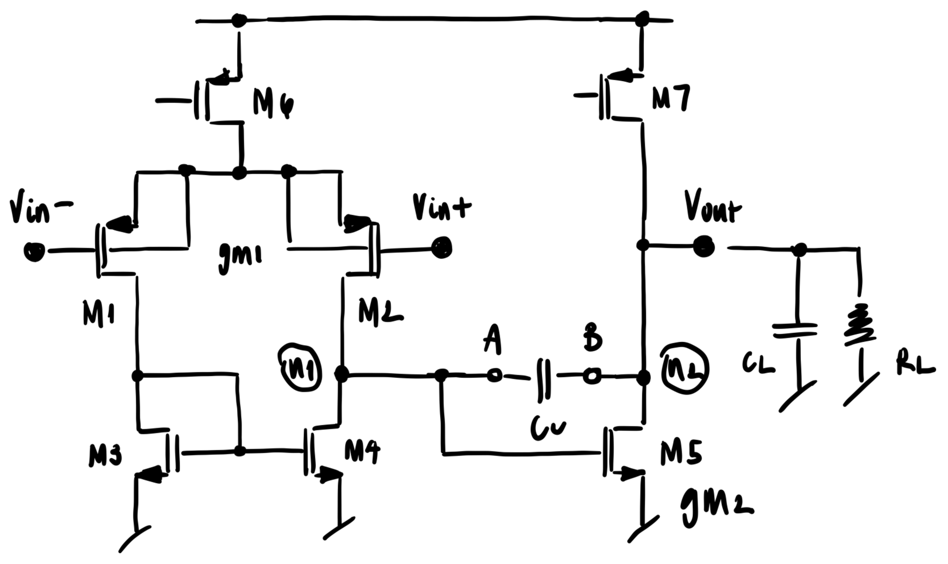
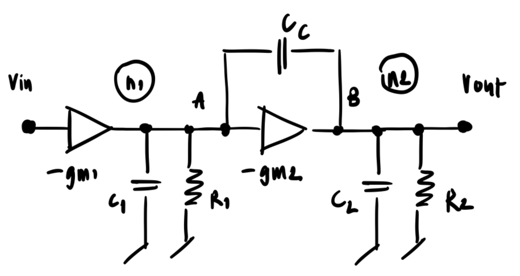
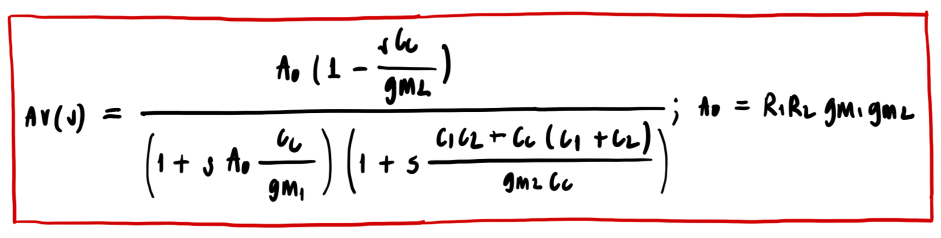
MOS SizingTool *Single Transistor Simulator*

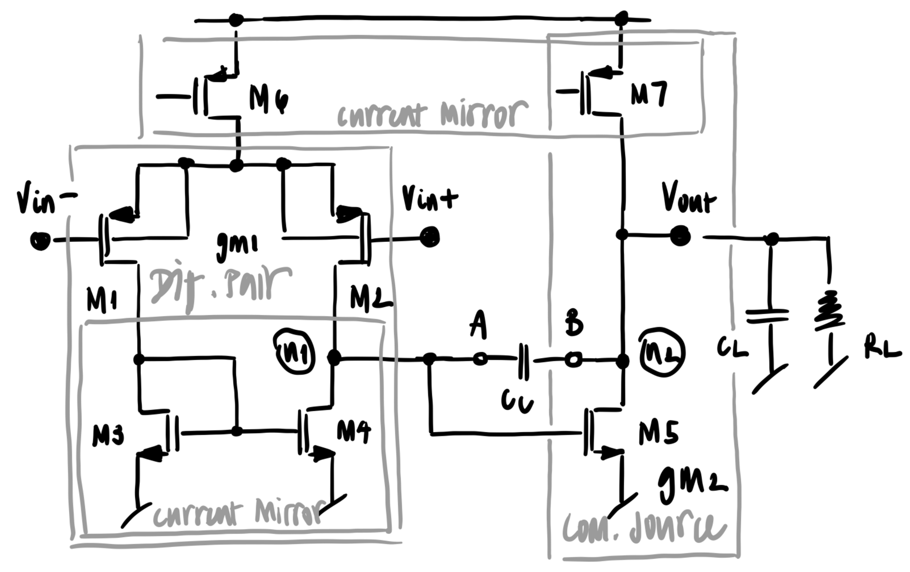
Support of Natural Design Flow

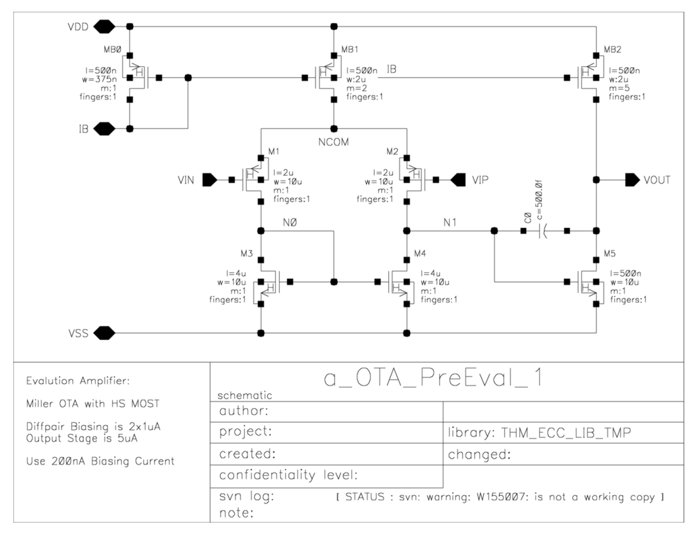


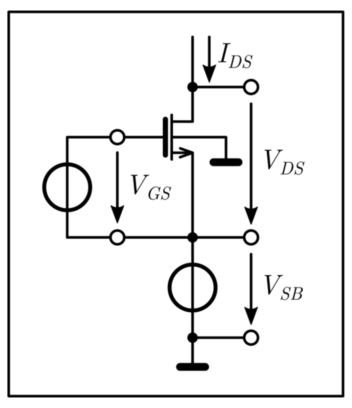




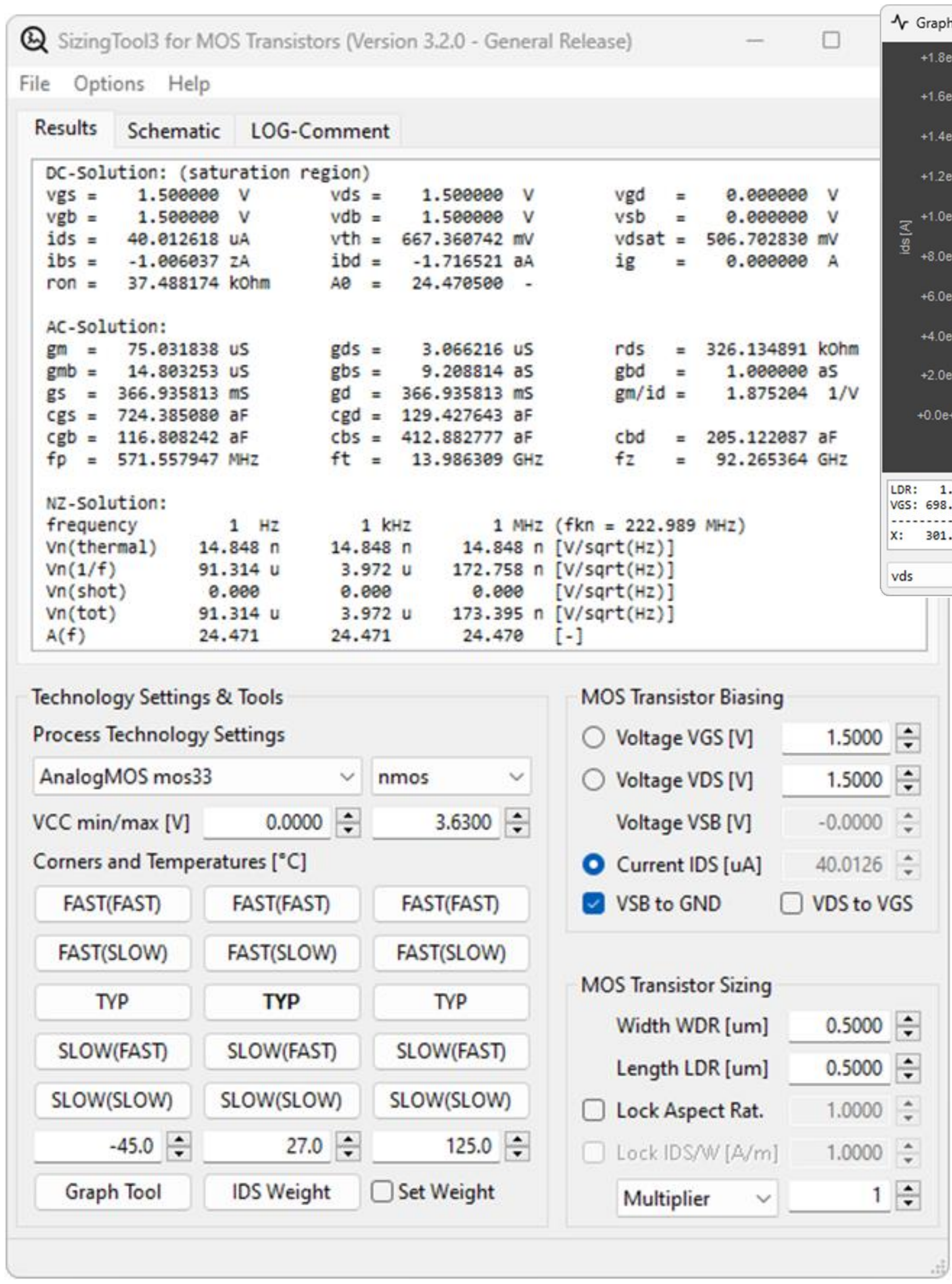
- Topology selection
- Circuit analysis
- Specifications (application) to secondary specifications (A_0, f_{UG}, f_p, g_m, g_{ds}, …)
- Macro block sizing
- Estimation of V_{dsat} and V_{DS}
- Adjustment of V_{dsat} and g_m's according specifications
- Schematic verification

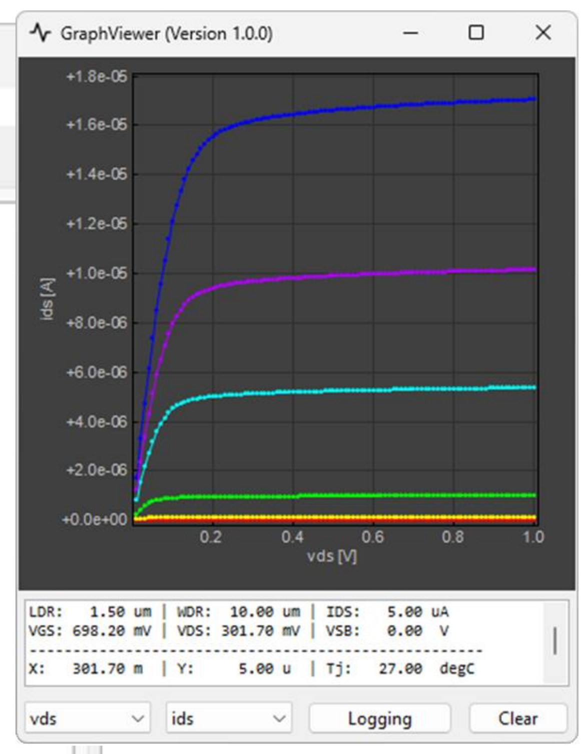






Solution for DC, AC, and NZ





Process Technology

Available Process Corners

Corner Temperature

Biasing Condition
$V_{GS} = f(V_{DS}, I_{DS}, V_{SB})$
$V_{DS} = f(V_{GS}, I_{DS}, V_{SB})$
$I_{DS} = f(V_{DS}, V_{GS}, V_{SB})$
Diode Connection ($V_{DS} = V_{GS}$)

Transistor Dimensions

General Remark on Transistor Sizing *Current density I_{DS}/W design procedure*

The (main) purpose of a MOST is to make gain, hence, large g_m and small g_{ds}.

$$I_{DS} \approx K\frac{W}{L}V_{dsat}^2, \text{ hence, } V_{dsat} \approx \sqrt{\frac{I_{DS}}{W}\frac{1}{\sqrt{K}}}\sqrt{L}$$

- choose "reasonable" current density I_{DS}/W
- adjust V_{dsat} with $L \rightarrow V_{dsat}$ and V_{ds} sets g_{ds}
- adjust g_m with I_{DS}/W

(with V_{dsat} fixed, also $\omega_T = \mu V_{dsat}/L^2$ is fixed , and $I_{DS}/g_m = V_{dsat}/2$ fixed)

rsvNumerics