

ODE4EC-AMS OpenPDK

Status and Roadmap

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the European Union**

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Outline:

- Motivation
 - Talent Gap by Microelectronic Job Profile in EU
- eSim FOSSEE Tool for IC Design
- Open PDK Initiatives
 - SkyWater (US), GF (US), AIST ACPS (J), ICSprout (CN) and IHP (D)
- IHP Open PDK and FOSS Tools Flow Development
 - Technology - Devices - Applications
- What's next?
 - Roadmap for Open-Source EDA in Europe
 - ODE4EC-AMS: open source EDA tools for IC designs
- Acknowledgment

Motivation: A call for Building Talent and Skills

To conclude



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EU Chips Act Drives pan-European full-stack innovation partnerships

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A call for

System Technology Co-Optimization

Pilot Lines and design platforms for
advanced and mature nodes innovation

Focus on Sustainable innovation

Building Talents and Skills

Full-stack innovation
partnerships



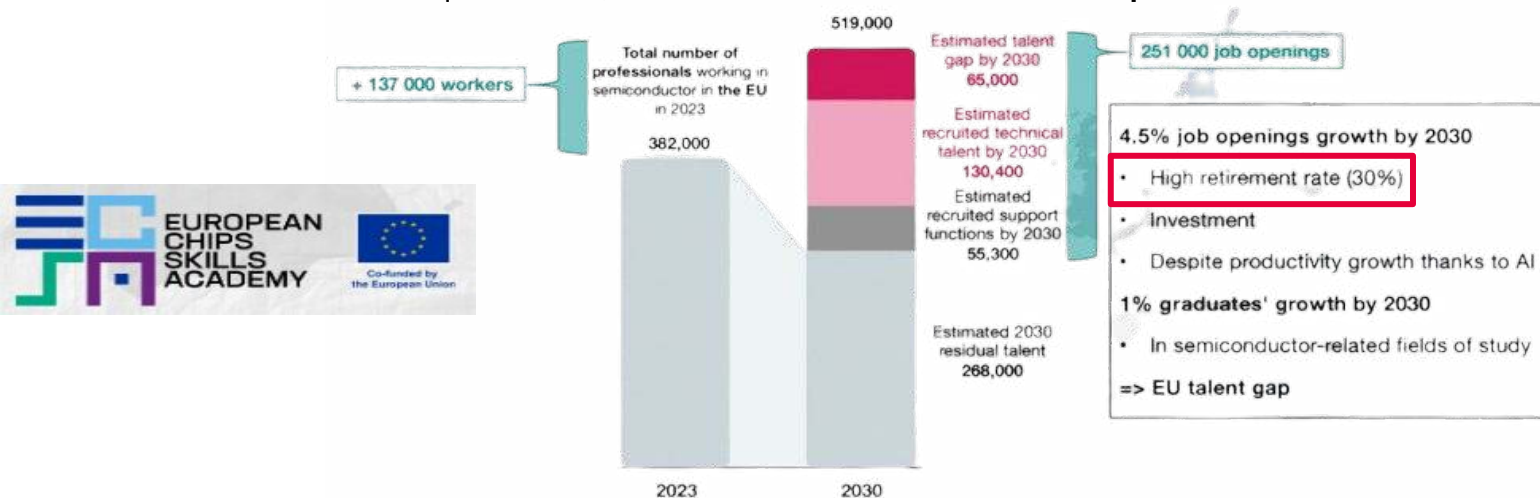
[REF] EU Chips Act Drives Pan-European Full-Stack Innovation Partnerships
Plenary Session at ISSCC, FEB.20, 2023

Jo De Boeck, Executive VP and CSO, imec and KU Leuven, Belgium



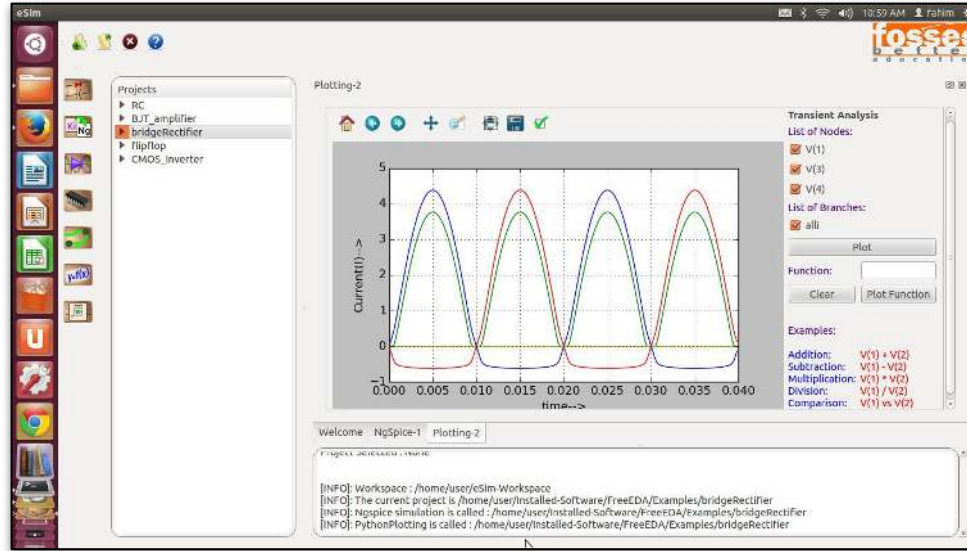
Talent Shortage: 65000 Jobs in Europe by 2030

- **Ageing workforce:** 30% of employees expected to retire by 2030
- Gaps in training: **limited training pipelines** for electrical engineering in some countries (eg: France, Italy)
- **EU-wide shortfalls in training** for system designers, analog designers, and cybersecurity experts
- In the second quarter 2026, **ASML sold no new machines in Europe**



- **One in three imec researchers** now comes from outside the EU <https://lnkd.in/ekNf-DkY>
- "Klicken und wischen" statt digitaler Kompetenz <https://www.tagesschau.de/>
- In 2025, only 14.7k students passed the high-school physics exam (a drop of 25% in six years).
At the same time, Poland wants to develop the nuclear energy, automotive industry, and microelectronics.
A PARP report warns that 24% of companies already lack engineers, and by 2040 Poland may be short of 44k specialists.

eSim FOSSEE Tool for IC Design



- eSIM FOSSEE Collaborative Effort <<https://esim.fossee.in/home>>
 - A global advisory committee for eSim to connect industry and academia.
 - [eSim Team participated in the WOSET conference](#), showcasing advancements.
 - [eSim Research Migration Initiative](#) started to shift research papers published using the **Open Source** eSim
 - Collaboration with **Open Source Fabs** to enhance hardware accessibility.
 - [Mixed Signal Circuit Design Competition](#) conducted earlier with Google SkyWater and adapting **IHP OpenPDK**
 - [eSim Marathon https://esim-hackathon-2025.fossee.in/](https://esim-hackathon-2025.fossee.in/)
 - eSim EDA Tool with IHP OpenPDK integration:
 - <https://github.com/FOSSEE/eSim/blob/master/ihp/ihp-install-script.sh>

Google Silicon



Automated RTL to GDSII flow that performs full ASIC implementation steps from RTL all the way down to GDSII offers a set of free and open-source tools enabling fast prototyping for FPGA chips and automated EDA support, through open standard collaboration <https://osfpga.org/about-us/>

- **Semiconductor R&D:** Tapeout of a design is one of the most important aspects of academic semiconductor research and development.
- **Prohibitive cost:** The prohibitive cost of tapeout and complications therein has prevented the majority of R&D folks and startups from participating.
- **Open-Source:** Open PDK Initiative plans to promote and facilitate the usage of open source FPGA technologies.
- **Free tapeouts:** Open PDK Initiative plans to offer a very simple flow for tapeout, and several of those will be free or at minimal costs.

Available Resources (see chipfoundry, now):

- SkyWater Open 130nm CMOS PDK: <https://github.com/google/skywater-pdk>
- OpenLane RTL2GDS Compiler: <https://github.com/efabless/openlane>
- Caravel Harness: <https://github.com/efabless/caravel>
- Caravel User Project: https://github.com/efabless/caravel_user_project
- Open MPW Precheck: https://github.com/efabless/open_mpw_precheck

[REF] <https://developers.google.com/silicon>

一生一芯 Initiative



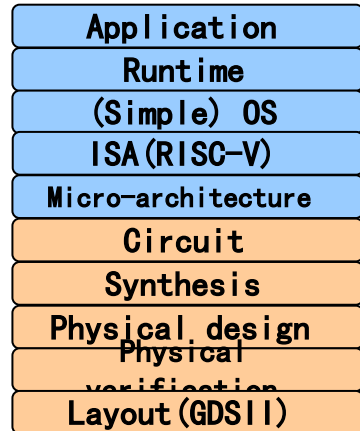
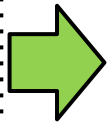
Start From Scratch
Create Your Own
RISC-V® Processor

Everyone is
welcome, with
no limitations

- University
- Major
- Grade level
- Background



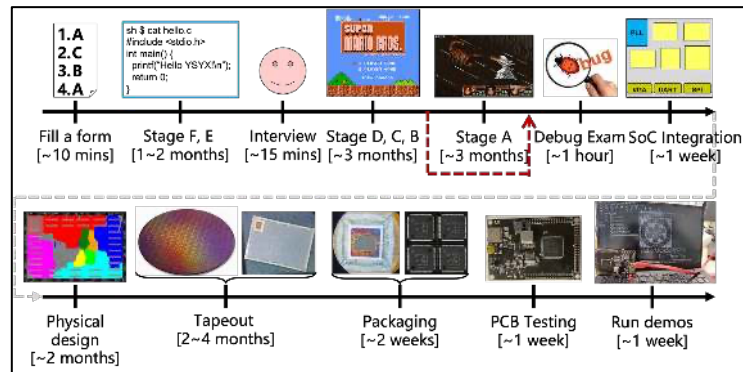
Education
equality



Full-stack
training

Visit <https://ysyx.org/en/>
Enroll Anytime, Open Year-Round

- 4 years since inception
- 800 schools have been involved
- 10,000 students have participated
- 100 ICs have successfully taped-out



Students learn to design their own RISC-V processors
(RTL→GDSII) using OpenPDK (SkyWater, ICSprout55 or IHP
OpenDPK)

A Massive Open Learning-by-doing Initiative
<https://github.com/Jasonyanyusong/OneStudentOneChip>

New Chinese ICSprout 55nm OpenPDK

- ICSprout Semicond. is a **Chinese** foundry (**founded in 2021**)

- jointly established by Zhejiang Provincial Government and ZJU
- have **advanced** 12-inch CMOS 180/55nm process lines
 - 55nm-CMOS, 55nm-eFlash, 180nm-BCD
 - collaborate with universities, academia and industry in China

- open its 55nm-CMOS PDK in **July, 2025**

- MPW tape-out cost (**55nm CMOS Open PDK**)

- **Independent:** 30~40K yuan/mm² (\$4,182~\$5,576/mm²)
- **Full Mask (600mm²):** 10K yuan/mm² (\$1,395/mm²)

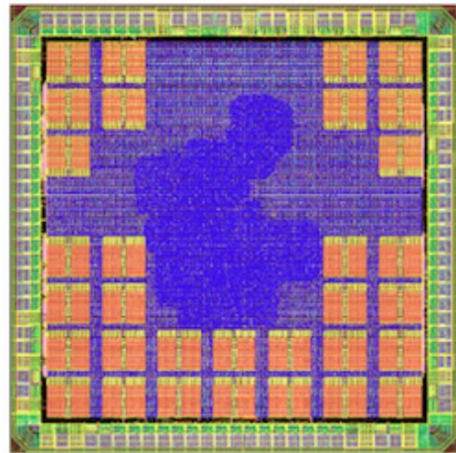
<https://github.com/openecos-projects/icsprout55-pdk>

- Bring ICSprout 55nm Open PDK into **ECOS Studio**

- establish strong cooperation with ICSprout (**What've we done**):

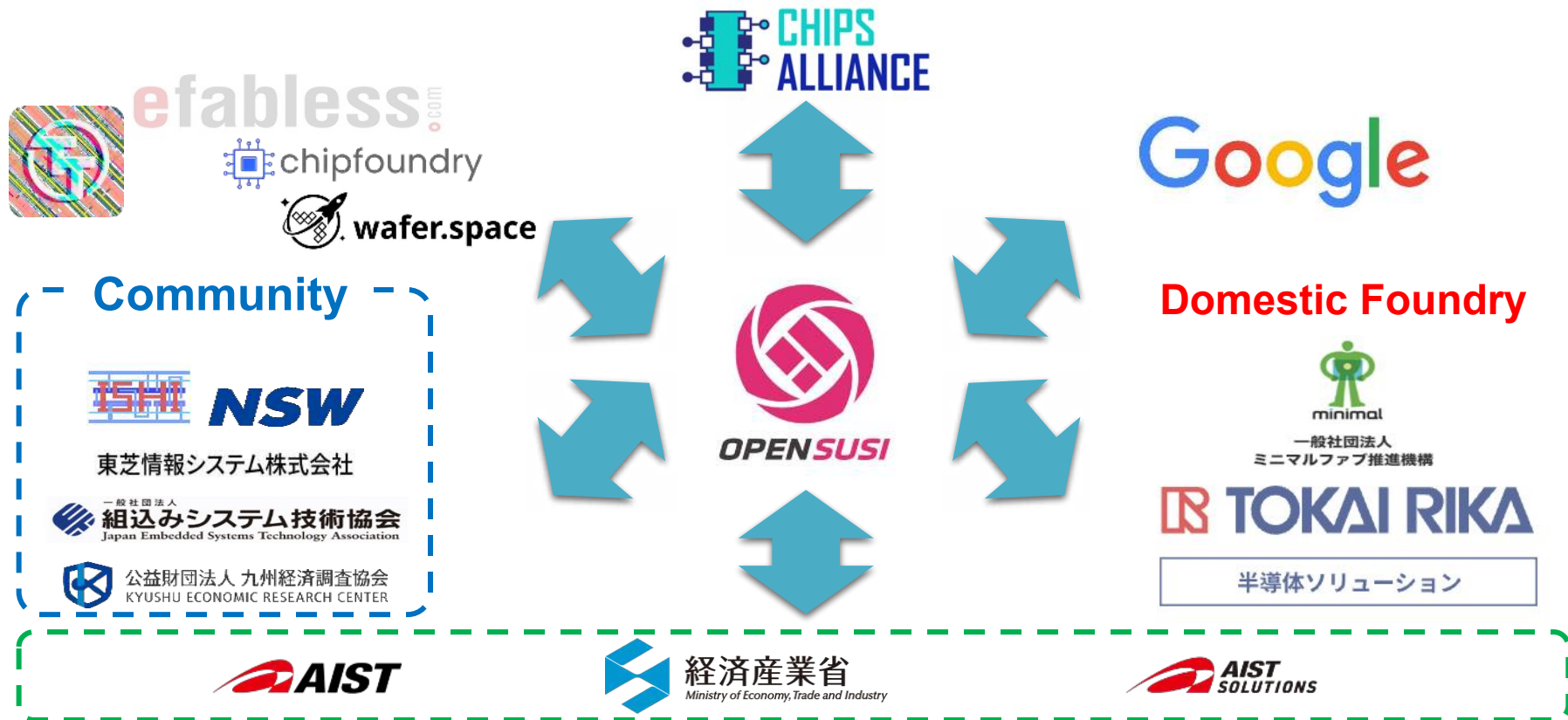
- port our designs and backend flows into ICSprout 55nm Open PDK
- tape-out **FIRST** test chip on ICSprout 55nm Open PDK in **June 15, 2025**
- help to try PD flow and give feedbacks to ICSprout for bugs fixing

develop **OPEN-SOURCE PLL** and **DDR3 PHY** based on ICSprout 55nm Open PDK(**ongoing**)



Design: A RV32IMAC SoC(PSRAM, QSPI, UART, I2C, PWM, TIMER, RNG). Impl. by Innvovs
Size: 4mm²(128KB OCM, no PLL)
Freq: 100MHz(external clock bypass)
Gates: 1.517M(73,009 cells)
Power: 115.4mW(dynamic) 0.42mW(static)

OpenSUSI Initiative



[REF] <https://www.opensusi.org/>
<https://ishikai.connpass.com/event/374444/>

OpenPDK Brazil: The CI Aberto Project



OpenPDK Brasil

Disseminating Open-Source Efforts for the
Lusophone Microelectronics Community

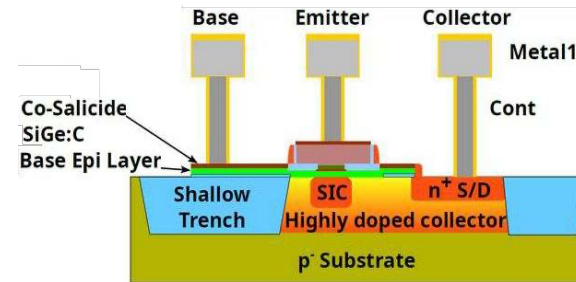
São objetivos específicos:

- Guiar novos estudantes sobre a existência de ferramentas e PDKs abertos;
- Fazer a curadoria de links para conteúdo em língua estrangeira;
- Incentivar a colaboração e a adoção de ferramentas abertas na comunidade acadêmica e industrial;
- Promover a formação de redes de apoio para o compartilhamento de experiências e conhecimentos em ferramentas EDA e PDKs abertos.

IHP SiGe-HBT SG13G2 OpenPDK

	SG13S	SG13G2	SG13G3Cu
SiGe-HBT	250 / 340 GHz	350 / 450 GHz	470 / 650 GHz
f_t / f_{max}			
$W_{emitter}$	170 nm	130 nm	110 nm
HBT BV_{CEO}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	2.1 fF / μm^2
Metallization	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	*Cu: 4 + 2 (3 μm) Al: 2 (3 μm)

- ❑ Targets are high-end applications for RF and THz frequencies, cryo, space
- ❑ SG13G2 is qualified and ready for Low Volume of high-end products it was selected for the OpenPDK development
- ❑ SG13G3Cu is early access / qualification scheduled 2025



[REF] IHP 130nm BiCMOS **OpenPDK**, dedicated for Analog/Digital, Mixed Signal and RF Design

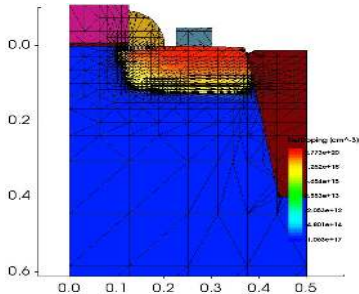
<https://github.com/IHP-GmbH/IHP-Open-PDK>

<https://github.com/IHP-GmbH/IHP-Open-PDK/wiki/Networking-Workshop-FMD-QNC>

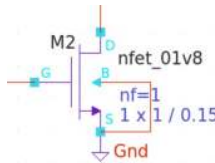
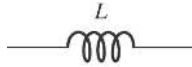
https://www.mos-ak.org/bruges_2024/publication/1_Scholz_ESSERC_2024_IHP_OpenPDK.pdf

<https://www.esserc2025.org/w2>

OpenPDK Device/Cell Abstract Views



Process/TCAD



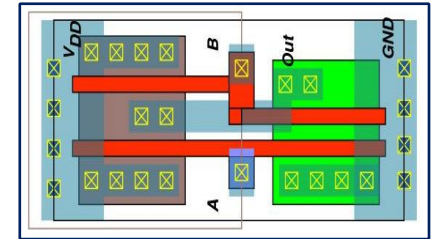
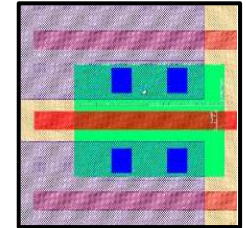
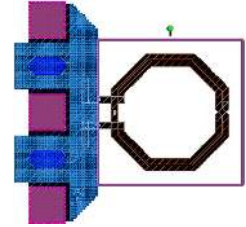
Schematic Symbols

```
# Inductor 3D Numerical Instance
gds_filename = "L_2n0.gds"
XML_filename = "SG13.xml"
script_path = utilities.get_script_path(__file__)
```

```
* SPICE instance NMOS Card
N1 (D G S B) nfet_01v8 <i_par=value>
* Model Card
.model nfet_01v8 psp <m_par=value>
```

```
// Verilog Instantiate: CMOS NAND gate
//
cmos_nand NAND1 (.a(A), .b(B), .out(Out));
```

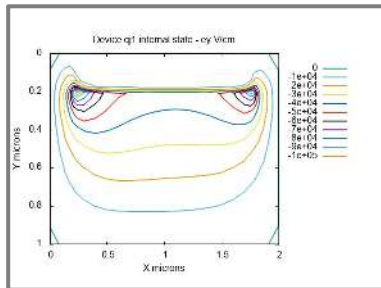
Numerical/SPICE/Verilog-A



GDSII Layout

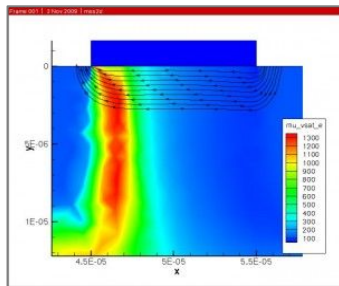
FOSS TCAD Process Simulations

Cider in ngspice



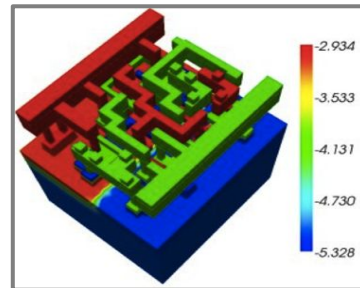
<https://sourceforge.net/projects/ngspice/>

DevSim TCAD



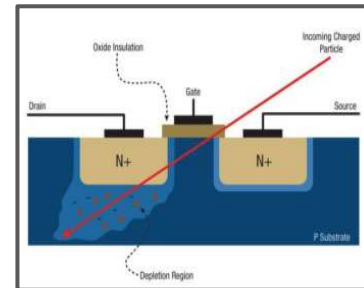
2D MOSFET simulation
<https://devsim.org/>

Cogenda TCAD



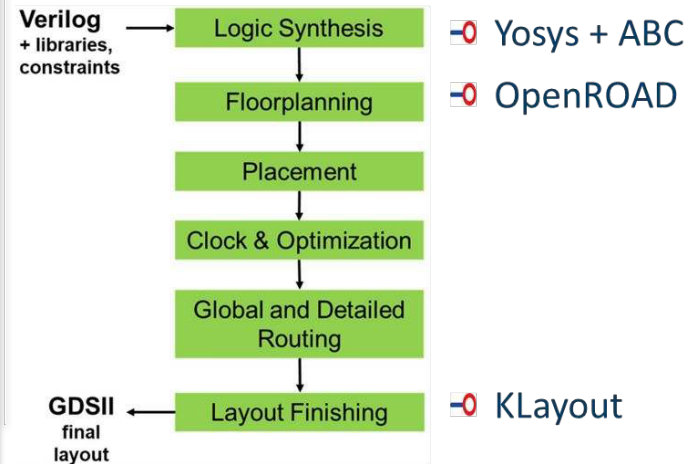
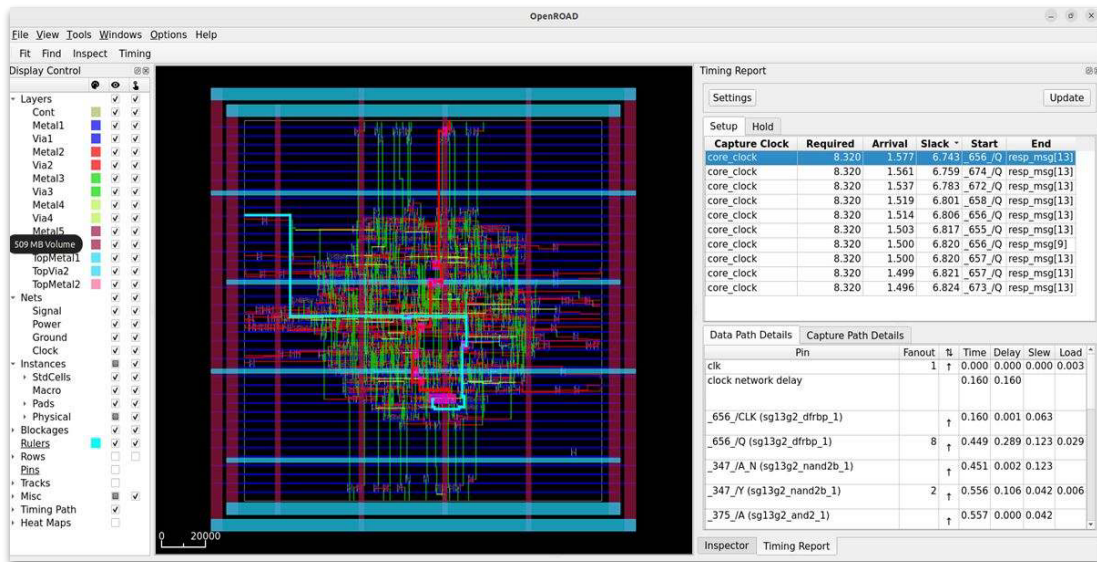
3D SRAM Cell
<https://cogenda.com/>

Charon TCAD



Single-Event Effects
<https://charon.sandia.gov/>

Open Source Digital Design Flow



OpenROAD is an open-source EDA tool that automates the entire digital circuit design process from RTL to GDSII, enabling no-human-in-the-loop chip fabrication. Developed under the DARPA IDEA initiative, it aims to democratize access to advanced semiconductor design by providing a free, end-to-end platform for researchers, startups and academia to innovate without proprietary tooling barriers.

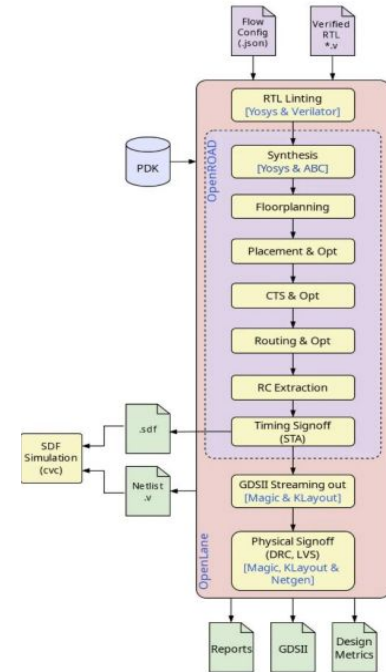
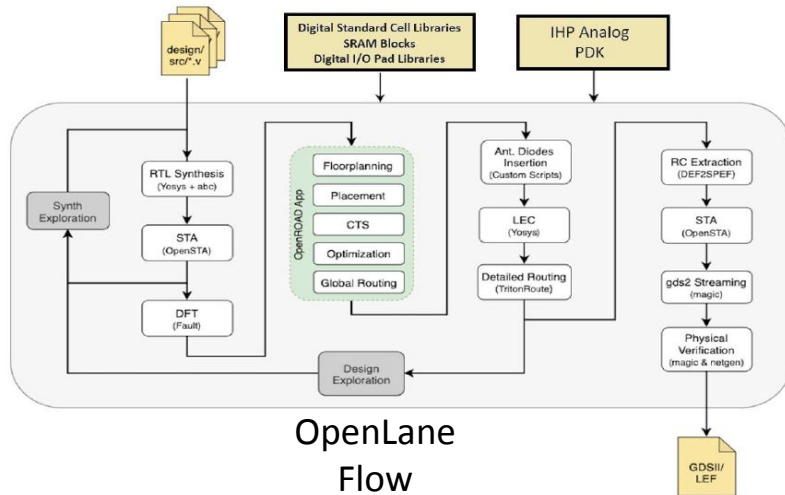
[REF] OpenROAD <<https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts>>

LibreLane <<https://colab.research.google.com/github/librelane/librelane/blob/main/notebook.ipyn>>

Alternative: LiP6 FOSS Logiciels: Alliance, Coriolis, Oceane, Standard Cell Libraries, Tas/Yagle <<https://largo.lip6.fr/equipe-cian/logiciels/>>

LibreLane Digital Design Flow

- Retain the simplicity of OpenLane and Flow/Apps supported
- Digital flow proven down to 16 nm
- Modularity and API Access
- Digital Libraries



[REF] LibreLane: Run a simple design through the OpenPDK flow: <http://github.com/librelane/librelane>
<https://colab.research.google.com/github/librelane/librelane/blob/main/notebook.ipyn>
<https://github.com/IHP-GmbH/ihp-sg13g2-librelane-template>

Alternative: LiP6 FOSS Logiciels: Alliance, Coriolis, Oceane, Standard Cell Libraries, Tas/Yagle
<https://largo.lip6.fr/equipe-cian/logiciels/>

LibreLane
Flow

LibreLane Digital Design Flow

Encapsulates the state of the design as an **immutable dictionary** of paths to various design formats.

Encapsulates a configurable **transformation** on the State object.

Encapsulates aggregations of steps for ease of configuration and ease-of-execution.

Performs validation of various **variables** used to configure flows and steps, incl. type checking.

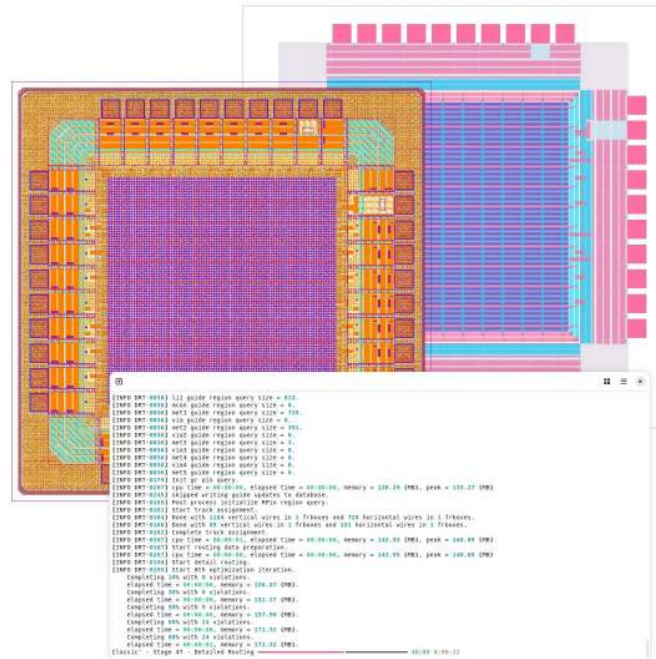
state
module

step
module

flow module

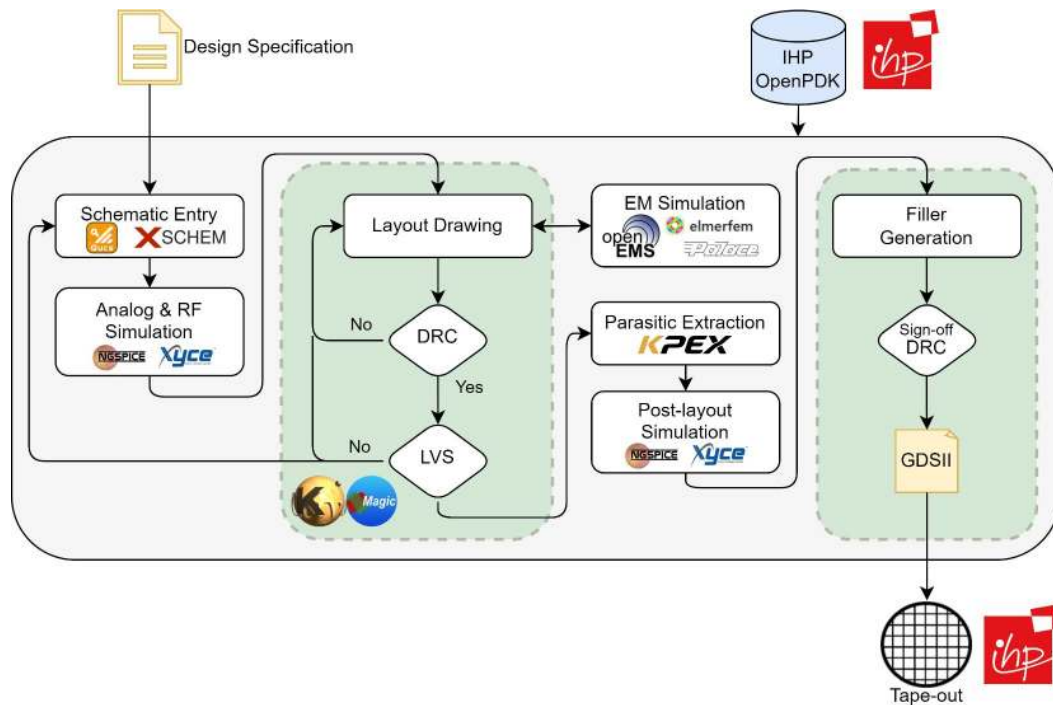
config module

The LibreLane Python API



[REF] LibreLane: <https://fossi-foundation.org/librelane/>
try online: <https://colab.research.google.com/github/librelane/librelane/blob/main/notebook.ipynb>
Alt: LiP6 FOSS Logiciels: Alliance, Coriolis, Oceane, Standard Cell Libraries, Tas/Yagle
<<https://largo.lip6.fr/equipe-cian/logiciels/>>

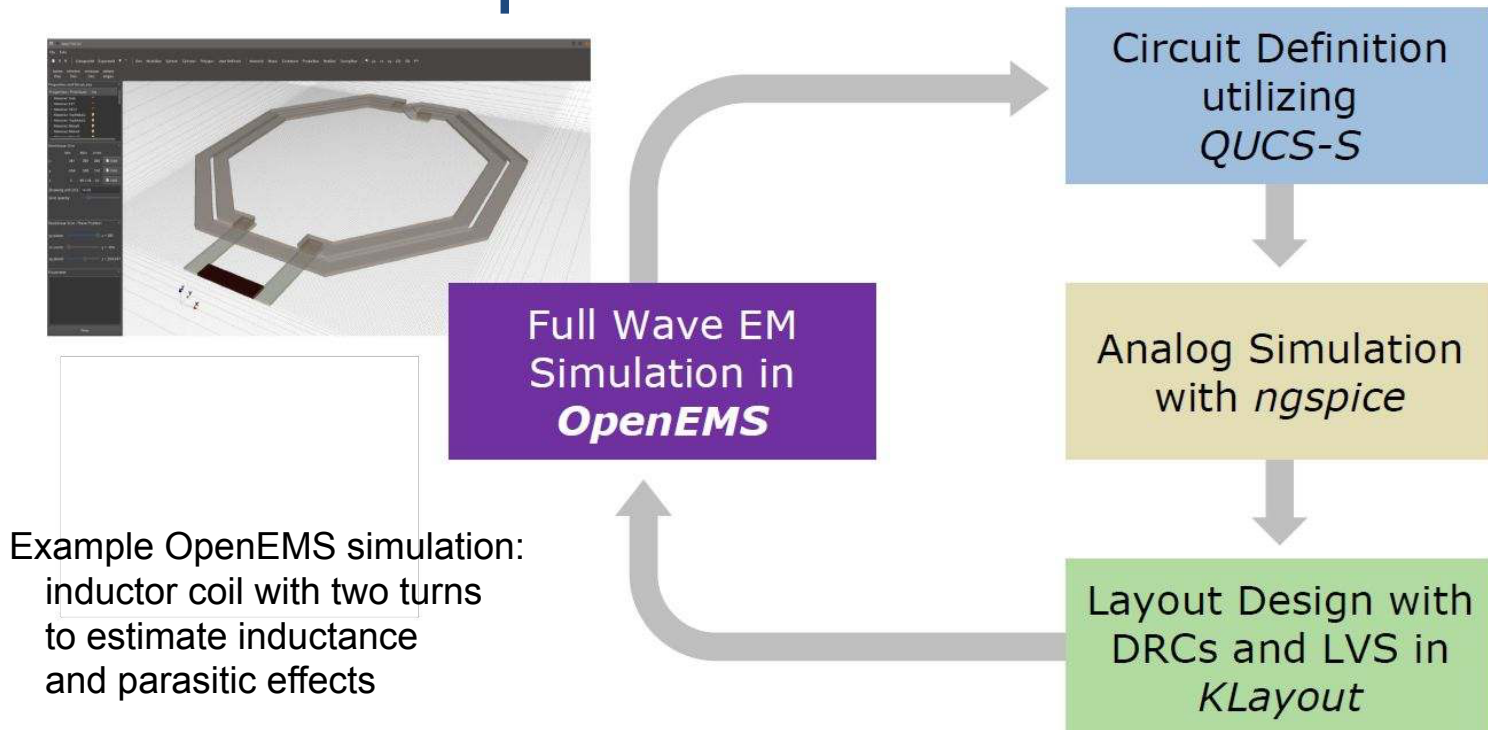
Analog/RF Open Source Design Flow



- QUCS-S, xschem
 - ngspice, Xyce, VACASK
- KLayout, Magic
 - Layout design
 - Parametric cells
 - Physical Verification
 - KPEX option
- OpenEMS
 - EMS ElmerFEM, Palace

[REF] IHP OpenPDK recommended FOSS EDA/CAD <<https://github.com/IHP-GmbH/IHP-Open-PDK-docs>>
IIC-OSIC-TOOLS is an all-in-one Dockers for analog and digital chip design <<https://github.com/iic-jku/iic-osic-tools>>
FOSS EDA Tools Wiki <<https://semiwiki.com/wikis/industry-wikis/eda-open-source-tools-wiki/>>

openEMS in OpenPDK



Example OpenEMS simulation:
inductor coil with two turns
to estimate inductance
and parasitic effects

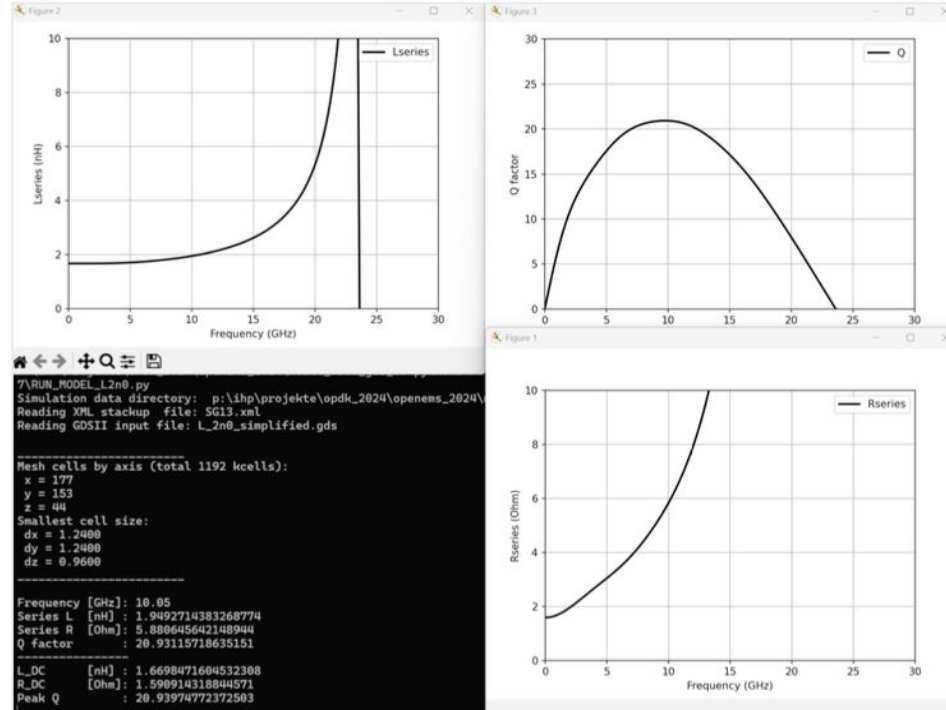
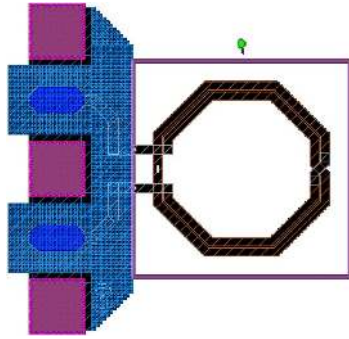
REF: Mustafa Alchalabi and Jan Taro Svejda

openEMS as a versatile tool in the framework of mm-wave openPDK-based RF chip design

https://www.mos-ak.org/bruges_2024/publication/5_Svejda_ESSERC_2024_openEMS.pdf

<https://www.esserc2025.org/w2>

Analog/RF modeling with openEMS



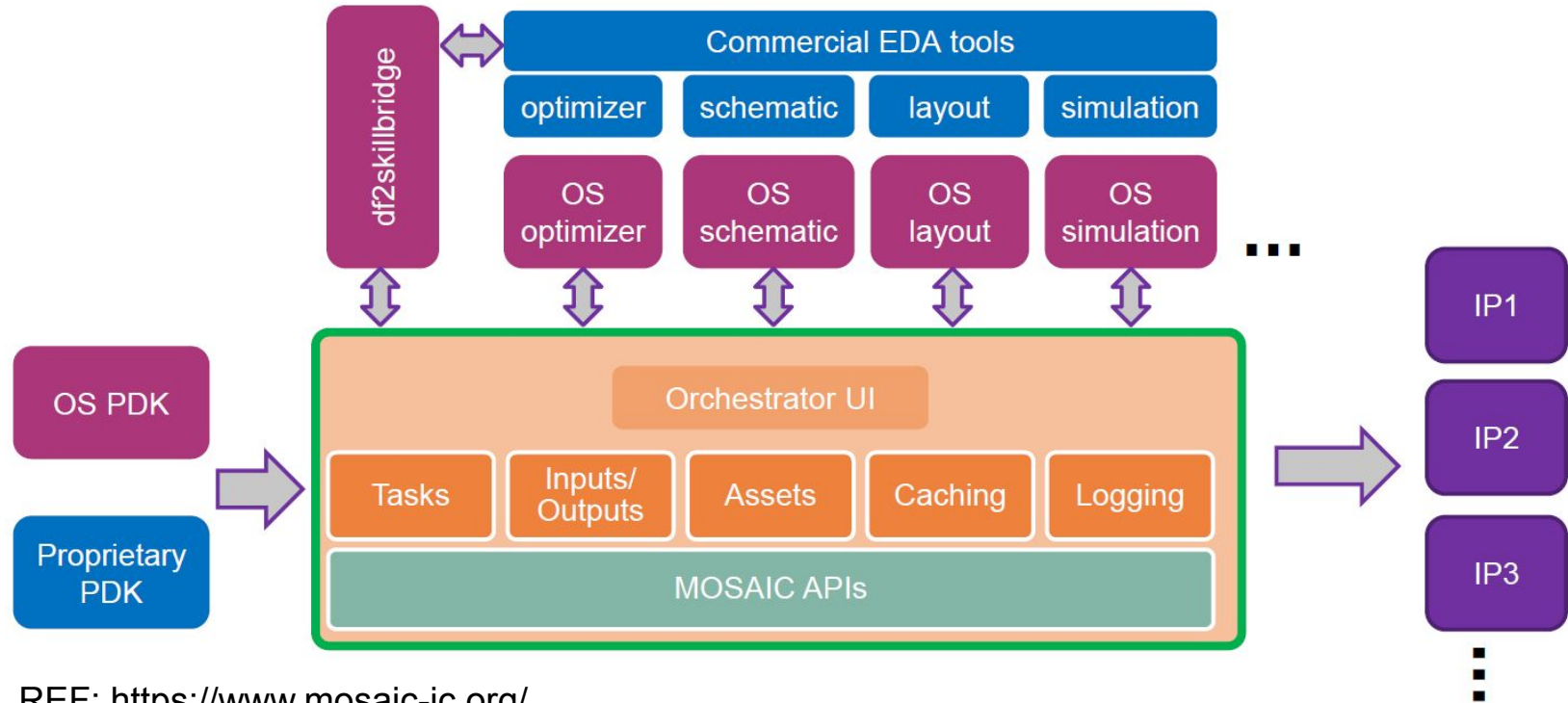
[REF] REF: Mustafa Alchalabi and Jan Taro Svejda “openEMS as a versatile tool in the framework of mm-wave openPDK-based RF chip design”

https://www.mos-ak.org/bruges_2024/publication/5_Svejda_ESSERC_2024_openEMS.pdf

Volker Mühlhaus; Using OpenEMS with IHP SG13 (Python Interface) ver.2.0 December 2024

<https://www.esserc2025.org/w2>

MOSAIC: Modular Framework



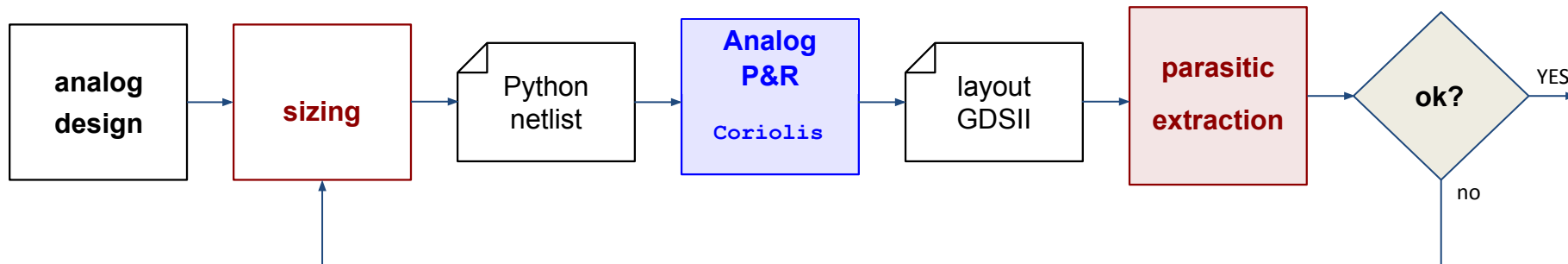
REF: <https://www.mosaic-ic.org/>

https://www.mos-ak.org/bruges_2024/publication/6_Sandner_ESSERC_2024_openIC.pdf

<https://www.esserc2025.org/w2>

Alternative: LiP6 FOSS Coriolis <<https://largo.lip6.fr/equipe-cian/logiciels/>>

CORIORIS – Analog Framework

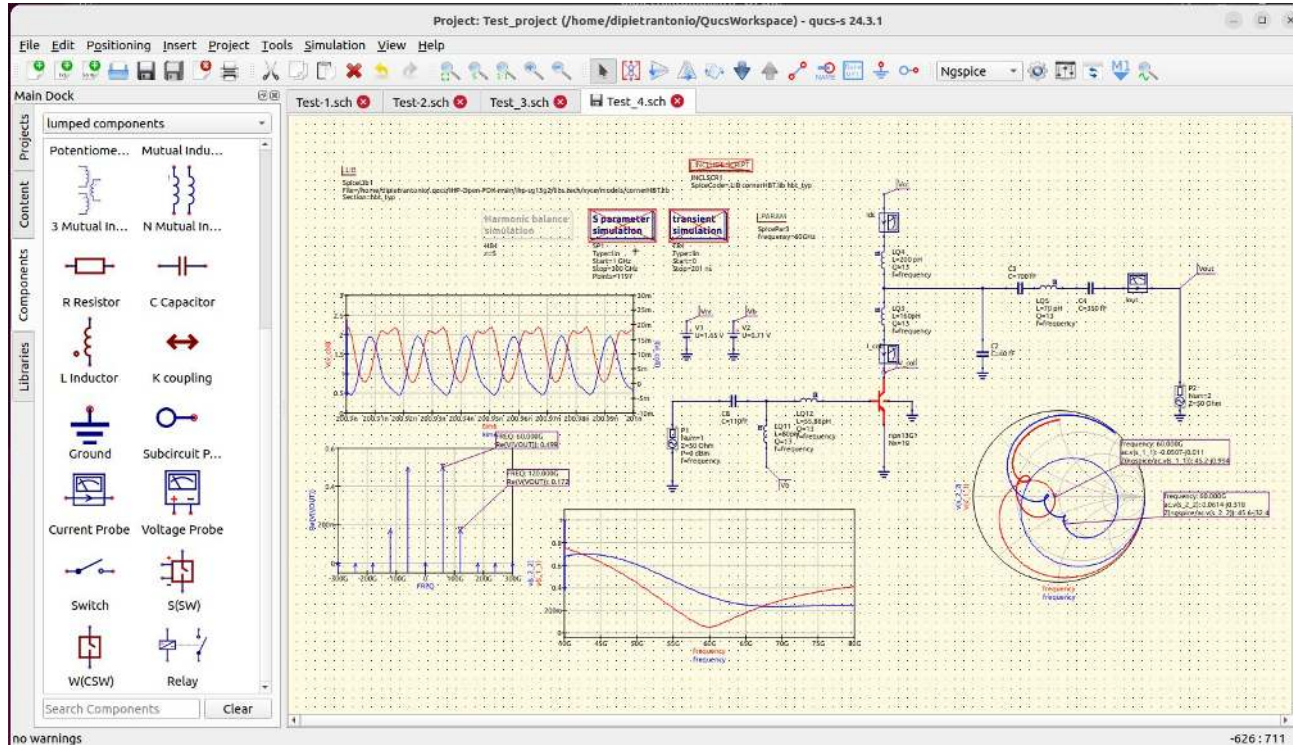


- CORIORIS focus on the P&R stage
- CORIORIS' assume the parasitics extraction do not fundamentally change the topological characteristics of the design
- That is only slight size adjustment of the components may be needed, so the overall topology remains valid

[REF] Jean-Paul CHAPUT, <Jean-Paul.Chaput@lip6.fr>
CIAN Team, LiP6 FOSS Logiciels:

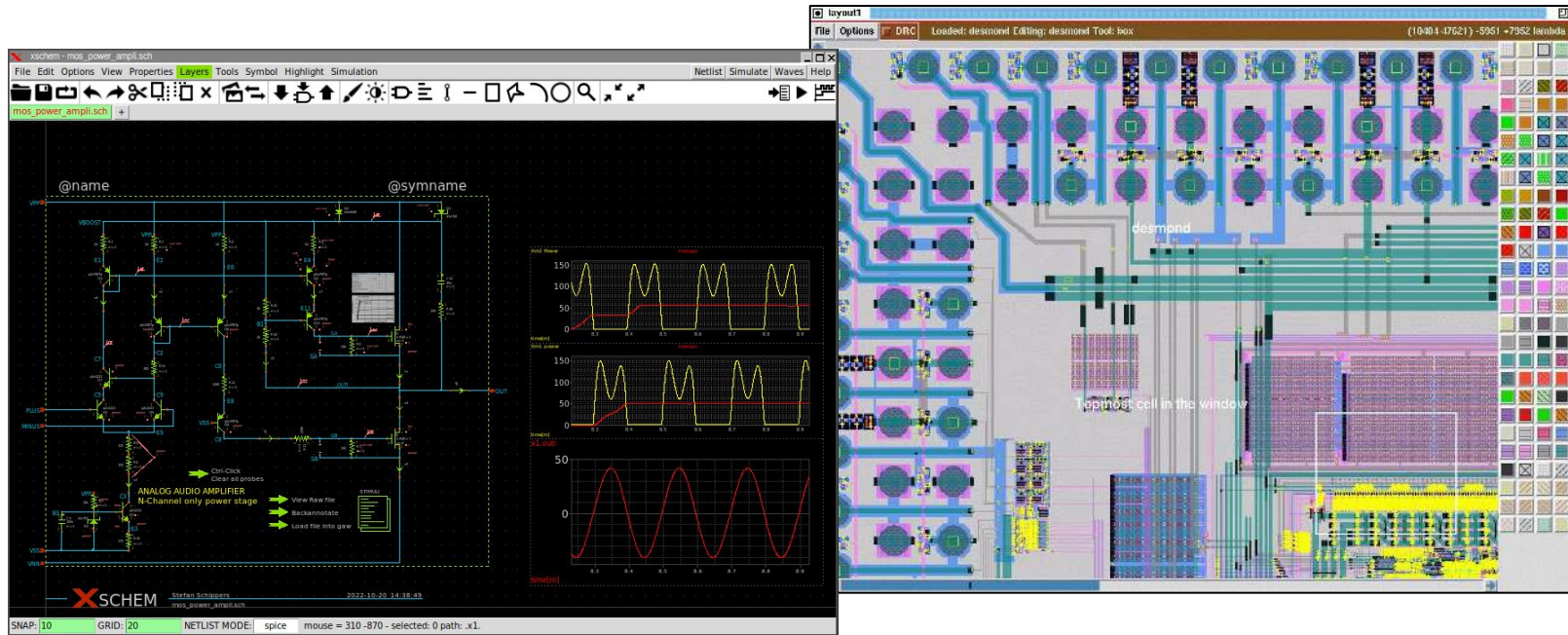


QUCS-S with ngspice for IHP Open PDK



REF: https://www.mos-ak.org/bruges_2024/publication/4_Brinson_ESSERC_2024_Qucs.pdf
<https://www.esserc2025.org/w2>

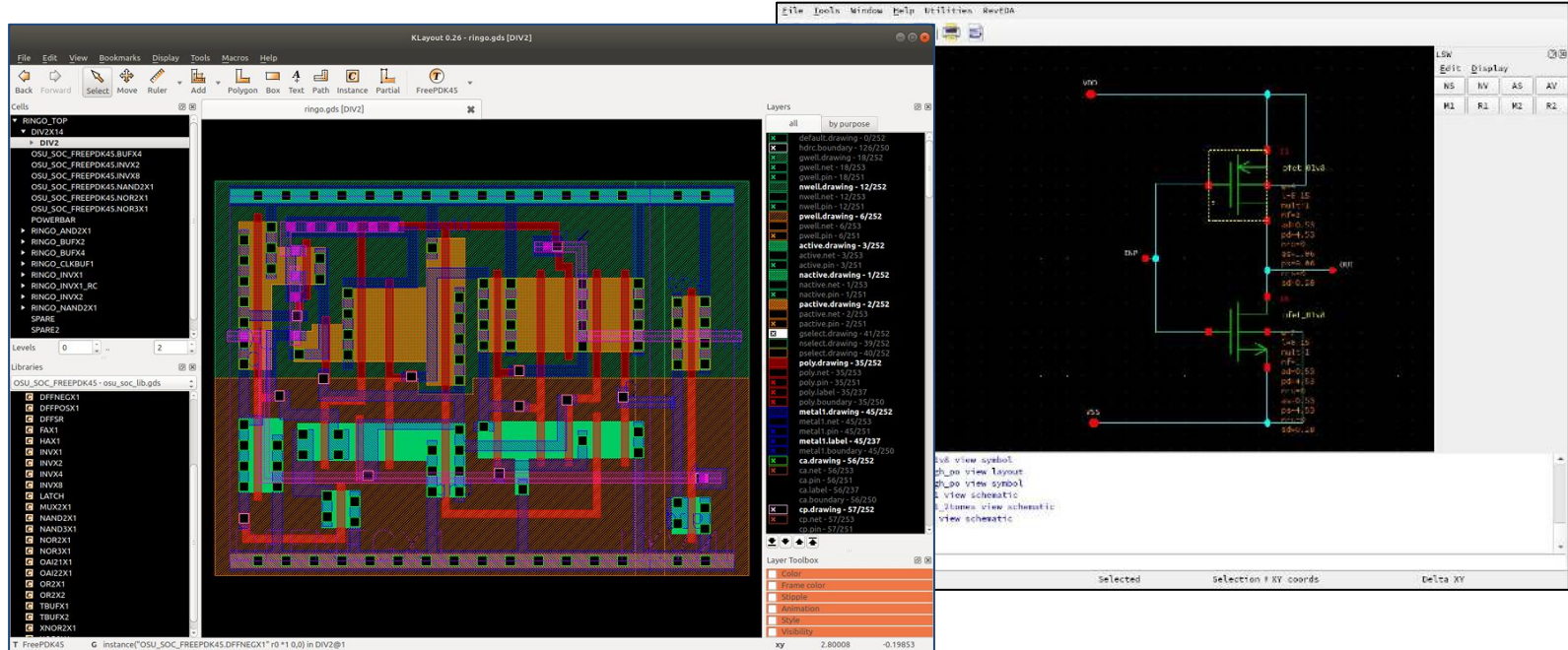
FOSS Schematic and Layout Editors



Xschem is a schematic capture program, it allows creation of hierarchical representation of circuits with a top down approach. By focusing on interfaces, hierarchy and instance properties, a complex system can be described in terms of simpler building blocks. A VHDL or Verilog or Spice netlist can be generated from the drawn schematic <<https://xschem.sourceforge.io/stefan/index.html>>

Magic version 8.3 is the official current released version of the program, a combined effort of the "Magic Development Team". The open-source license has allowed VLSI engineers with a bent toward programming to implement clever ideas and help magic stay abreast of fabrication technology. <<http://opencircuitdesign.com/magic/>>

FOSS Schematic and Layout Editors



KLayout has fast loading and accurate drawing, supports GDS and OASIS file formats with automatic uncompression of zlib compatible formats and is extensible and configurable to a large degree by custom Ruby or Python scripts

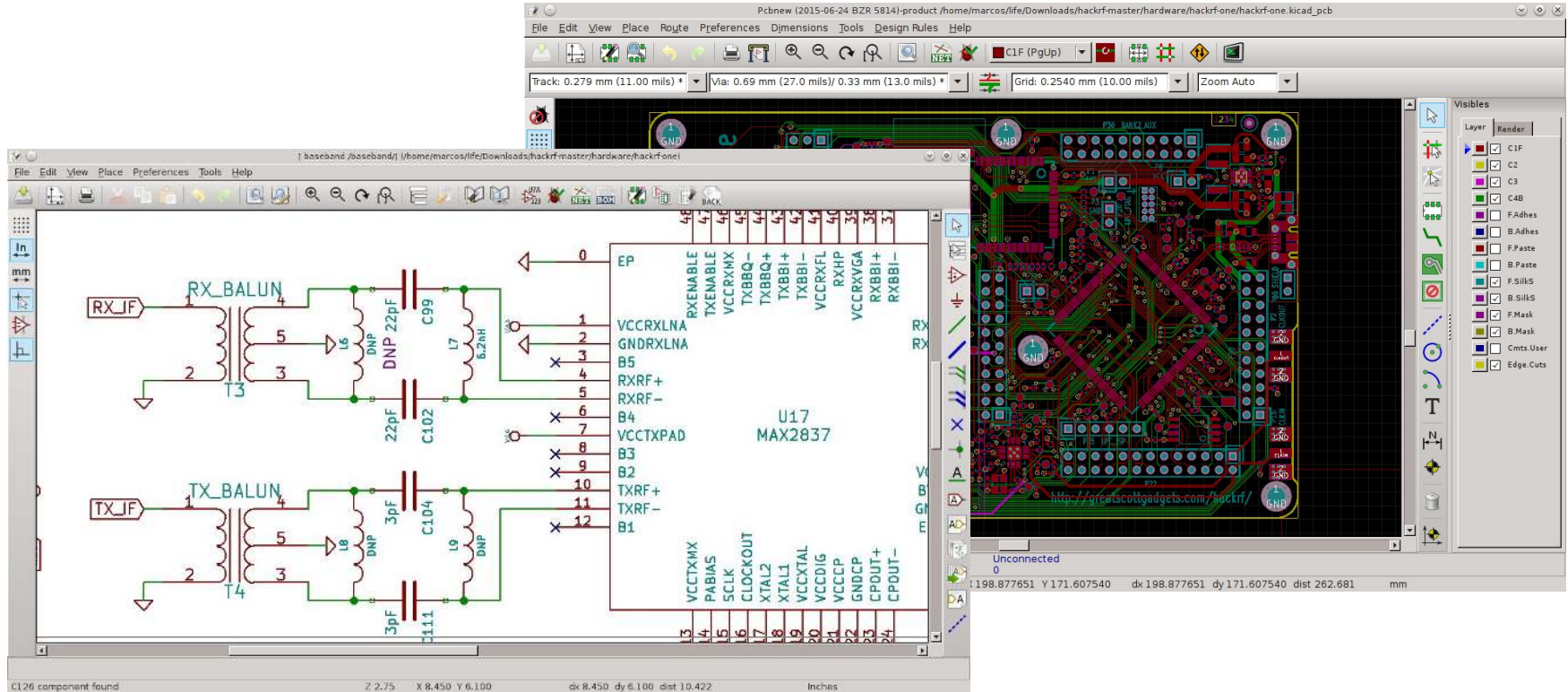
[REF] <https://klayout.de/>

<https://peertube.f-si.org/video-channels/fsic2022/videos?sort=-publishedAtand page=2>

Revolution EDA offers a complete setup starting from schematic or Verilog-A entry, to simulation, layout, DRC and LVS. Symbols have integrated callback functions allowing accurate simulations.

[REF] <https://reveda.eu/>

ngspice and KiCAD



[REF] <https://www.kicad.org/download/>
Holger Vogt; ngspice - XSPICE elemental devices made available in KiCad
<https://fosdem.org/2025/schedule/event/fosdem-2025-5619-ngspice-xspice-elemental-devices-made-available-in-kicad/>

Compact/SPICE Verilog-A Modeling

EKV Long Channel Verilog-A Code

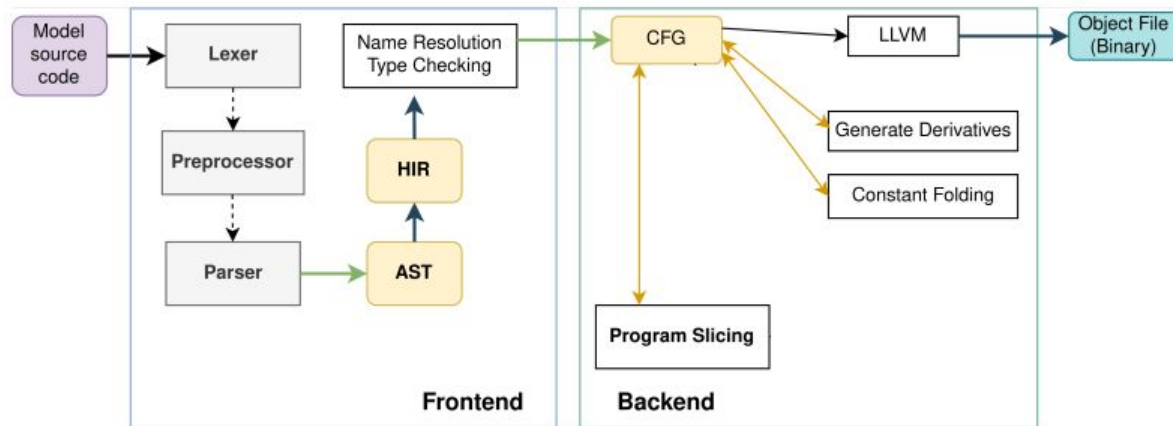
```
`include "std.va"
`include "const.va"
// *****
// * EKV MOS model (long channel)
// * https://ekv.epfl.ch/Verilog-A/
// *****
module ekv(d,g,s,b);
    //
    // Node definitions
    inout d,g,s,b ; // external nodes
    electrical d,g,s,b ; // external nodes
    //
    /*** Local variables
    real x, VG, VS, VD, VGprime, VP;
    real beta, n, iff, ir, Ispec, Id;
    //
    /*** model parameter definitions
    parameter real L = 10E-6 from[0.0:inf];
    parameter real W = 10E-6 from[0.0:inf];
    /*** Threshold voltage
    // substrate effect parameters (long-channel)
    parameter real VTO = 0.5 from[0.0:inf];
    parameter real GAMMA = 0.7 from[0.0:inf];
    parameter real PHI = 0.5 from[0.2:inf];
    /*** Mobility parameters (long-channel)
    parameter real KP = 20E-6 from[0.0:inf];
    parameter real THETA = 50.0E-3 from[0.0:inf];
```

```
analog begin // EKV v2.6 long-channel
    VG = V(g); VS = V(s); VD = V(d);
    // Effective gate voltage (33)
    VGprime = VG - VTO + PHI + GAMMA * sqrt(PHI);
    // Pinch-off voltage (34)
    VP = VGprime - PHI - GAMMA
    * (sqrt(VGprime+(GAMMA/2.0)*(GAMMA/2.0))-(GAMMA/2.0));
    // Slope factor (39)
    n = 1.0 + GAMMA / (2.0*sqrt(PHI + VP + 4.0*$vt));
    // Mobility equation (58), (64)
    beta = KP * (W/L) * (1.0/(1.0 + THETA * VP));
    // forward (44) and reverse (56) currents
    x=(VP-VS)/$vt;
    iff = (ln(1.0+exp(x/2.0)))*(ln(1.0+exp(x/2.0)));
    x=(VP-VD)/$vt;
    ir = (ln(1.0+exp(x/2.0)))*(ln(1.0+exp(x/2.0)));
    // Specific current (65)
    Ispec = 2 * n * beta * $vt * $vt;
    // Drain current (66)
    Id = Ispec * (iff - ir);
    //
    // Branch contributions to EKV v2.6 model (long-channel)
    //
    I(d,s) <+ Id;
end // analog

endmodule
```

[REF] EKV2.6 Compact MOSFET Model Standard for Analog/RF IC Design <<https://github.com/ekv26/model>>
EKV3 MOSFET model in Verilog-A <<https://github.com/MatBucher/ekv3model>>
Alternative: ACM2 (Advanced Compact MOSFET) charge-based physical model
https://github.com/ACMmodel/MOSFET_model/tree/main/Examples/IHP-SG13
Verilog-A Model Pythonic Rule Enforcer <<https://github.com/analogdevicesinc/vampyre>>

OpenVAF: Next-Generation Verilog-A Compiler



OpenVAF Roadmap

- Reaching full compliance with the Verilog-A standard on OpenPDK
- OSDI integration in ngspice and Xyce
- Noise analysis (released with ngspice-42*)
- Improved documentation

[REF] P. Kuthe, M. Muller; OpenVAF is a Next-Generation Verilog-A compiler
<<https://openvaf.semimod.de/>>

Árpád Bűrmen; VACASK and Verilog-A Distiller

<<https://fosdem.org/2025/schedule/event/fosdem-2025-4681-vacask-and-verilog-a-distiller-building-a-device-library-for-an-analog-circuit-simulator/>>

Alternative: Felix Salfelder and Al Davis; Verilog-AMS in GnuCap

<<https://fosdem.org/2025/schedule/event/fosdem-2025-5880-verilog-ams-in-gnucap/>>

EKV Verilog-A Long Channel SPICE Netlist

```
* EKV long channel MOSFET
* Verilog-A Model in SPICE

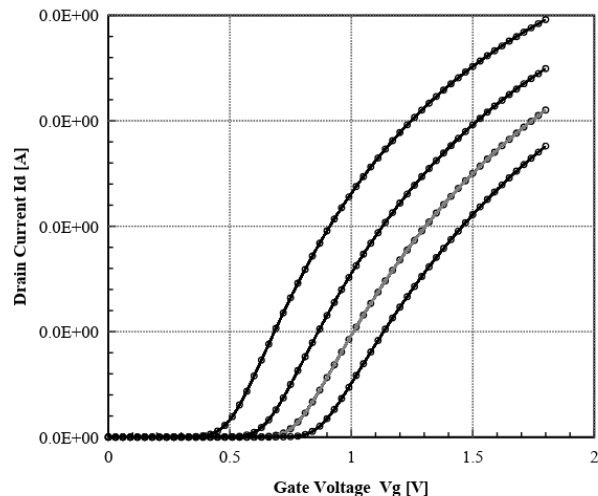
.osdi  ekv.va

vd  1  0 0.05
vg  2  0 2
vs  3  0 0
vb  4  0 0

xekv  1 2 3 4 ekv L=1E-6 W=1E-6

.dc  vg  0 2 0.1

.end
```

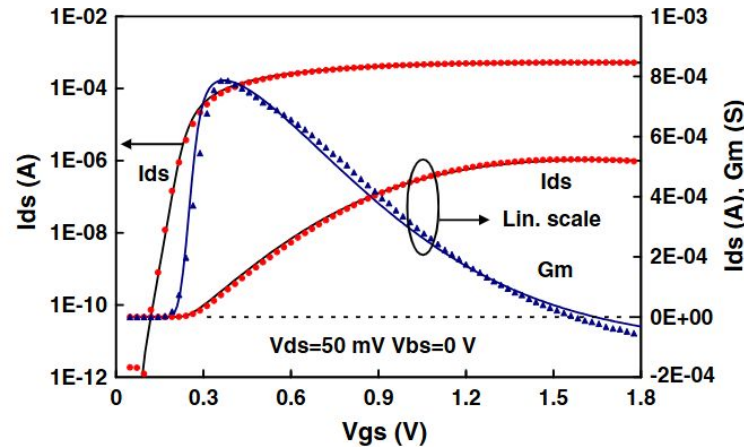


NLnet - "Test Procedures for MOSFET Open Source SPICE Model Validation"

The aims to establish such tests for the compact models in open PDKs, which are intended to be generic enough for model quality assurance testing with FOSS circuit simulators such as GnuCAP, ngspice, xyce, Qucs-S, among others.

<https://nlnet.nl/project/MOSFET-testprocedures/>

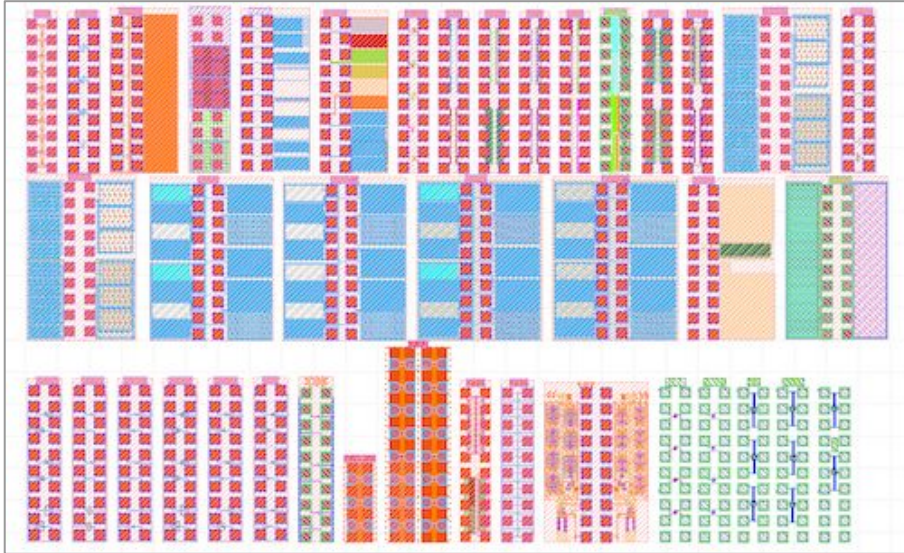
EKV Modeling at Cryo Temperatures



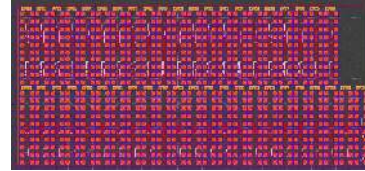
Measurements and EKV3 I_{ds} and G_m simulation: 1.8 V LVT W/L=20/2.5 NMOSFET at 77 K

- ❑ Saramad, Shahyar, Giovanni Anelli, Matthias Bucher, Matthieu Despeisse, Pierre Jarron, Nicolas Pelloux, and Angelo Rivetti. "Modeling of an integrated active feedback preamplifier in a 0.25 μ m CMOS technology at cryogenic temperatures." IEEE Transactions on Nuclear Science 50, no. 5 (2003): 1290-1296.
- ❑ Martin, P., M. Cavelier, R. Fascio, G. Ghibaudo, and M. Bucher. "EKV3 compact modeling of MOS transistors from a 0.18 μ m CMOS technology for mixed analog–digital circuit design at low temperature." Cryogenics 49, no. 11 (2009): 595-598.
- ❑ Beckers, Arnout, Farzan Jazaeri, Andrea Ruffino, Claudio Bruschini, Andrea Baschiroto, and Christian Enz. "Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing." In 2017 47th European Solid-State Device Research Conference (ESSDERC), pp. 62-65. IEEE, 2017.
- ❑ Beckers, Arnout, Farzan Jazaeri, and Christian Enz. "Characterization and modeling of 28-nm bulk CMOS technology down to 4.2 K." IEEE Journal of the Electron Devices Society 6 (2018): 1007-1018.
- ❑ Han, Hung-Chi, Antonio D'Amico, and Christian Enz. "sEKV Parameter Extractor of Simplified EKV I-V Model for Low-Power Analog Circuits." IEEE Open Journal of Circuits and Systems 3 (2022): 162-167.

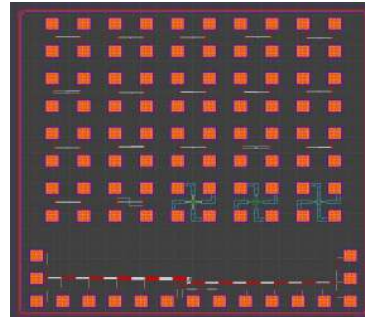
OpenPDK Test Chips



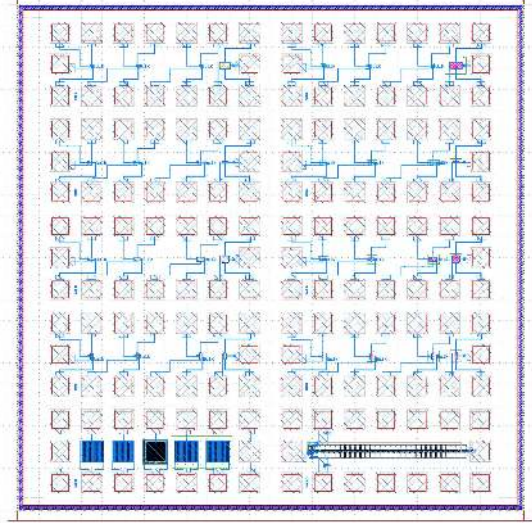
OpenTestChip Size: $6716.53\mu\text{m} \times 4183.42\mu\text{m}$
with 37 test structures/segments for DC, CV RF



SRAM Test Cells



CryoOpenTestChip



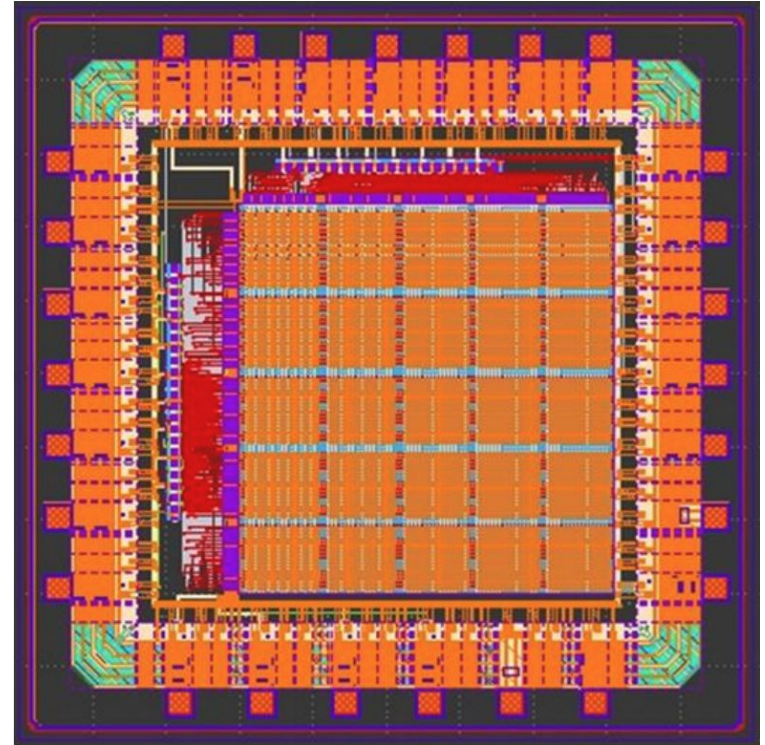
OpenTestChip for TR-1 μm OpenPDK

- REF: [1] https://github.com/wladek60/TO_Sep2025/tree/main/OpenTestChip
[2] https://github.com/IHP-GmbH/TO_May2025
[3] <https://github.com/wladek60/TR-1um-OpenTC>

OpenPDK MOSFET Matching Matrix IC

Complete 5×5 Matrix (25 subarrays)

- Each subarray contains $16 \times 16 = 256$ identical transistors
- Total devices per matrix: $25 \times 256 = 6,400$ devices
- W varies horizontally, L varies vertically
- Enables systematic mismatch analysis versus W, L, and W/L
- Scripts for automatic matrix test generation



[REF] Juan Brito, et al. "Statistical Analysis of MOSFET Extracted Parameters for n-MOS Mismatch Modeling"
<https://mos-ak.org/silicon_valley_2020/presentations/Brito_MOS-AK_SV_2020.pdf>
<https://github.com/IHP-GmbH/TO_Sep2025/tree/main/MissMatch>
F. Krummenacher "Matching Analysis of Analog Circuits" <https://www.mos-ak.org/lausanne/slides/fk_mos_ak.pdf>

Microelectronic Circuits and Smartphones

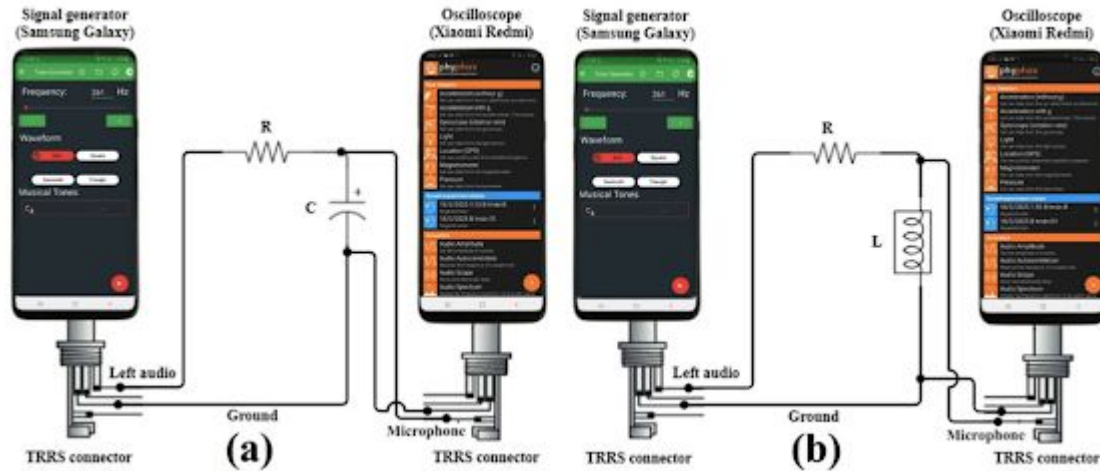
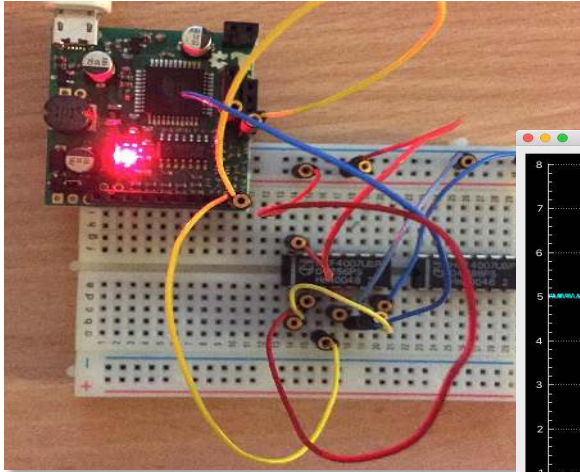


FIG: The connection diagram of (a) RC and (b) RL circuits shows smartphones working as signal generators and oscilloscopes

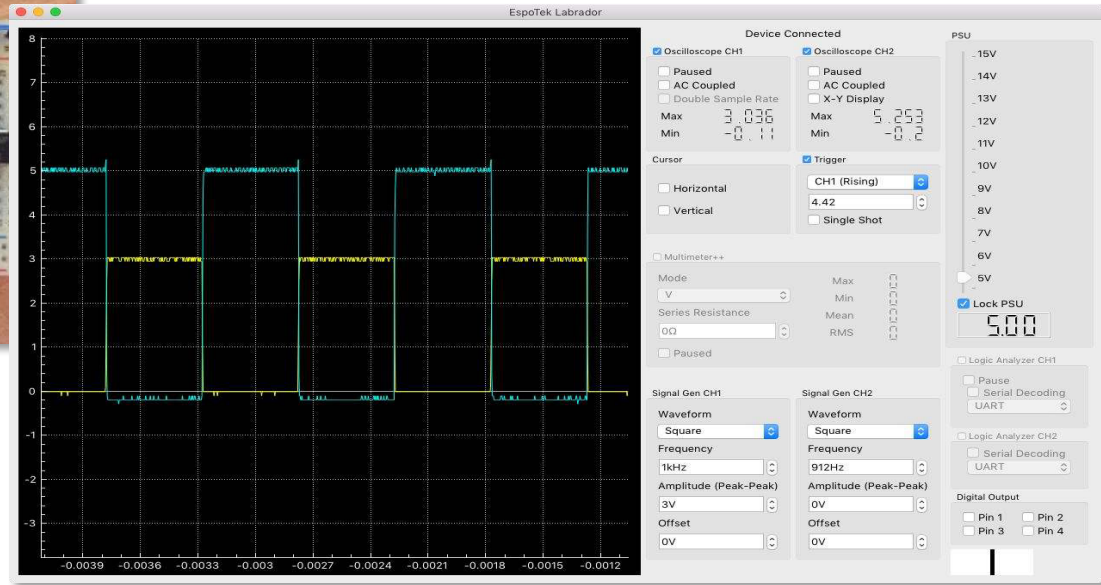
[REF] Lezcano, Marciano Santamaría, E. S. Cruz de Gracia, Lucio Strazzabosco Dorneles, and Noriel Correa. "Frequency effect on reactance in RC and RL circuits—a smartphone approach." *Physics Education* 60, no. 3 (2025): 035033

- Your smartphone is a mobile lab by RWTH Aachen University <<https://phyphox.org/>>
- Physics Toolbox by Vieyra Software <<https://www.vieyrasoftware.net/>>

EspoTek Labrador Circuit Lab



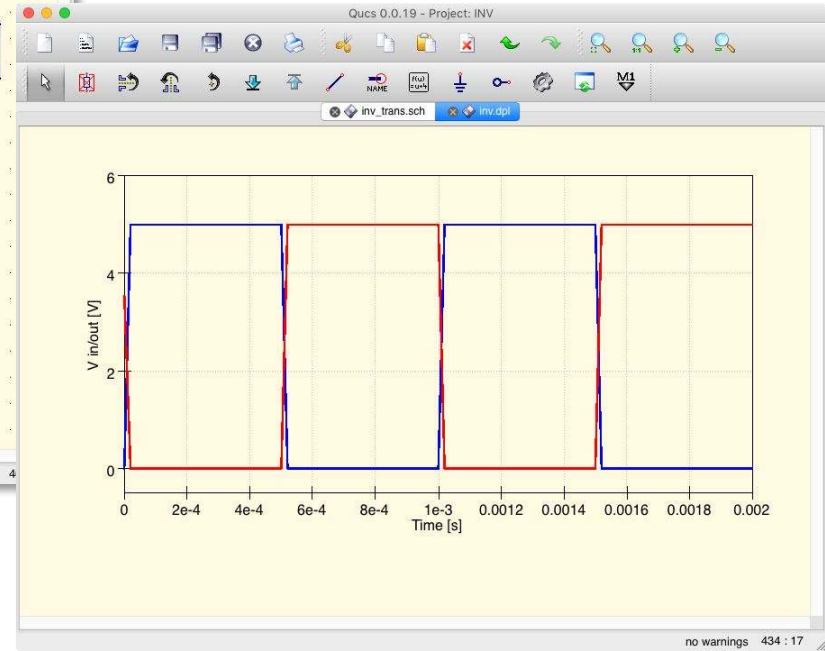
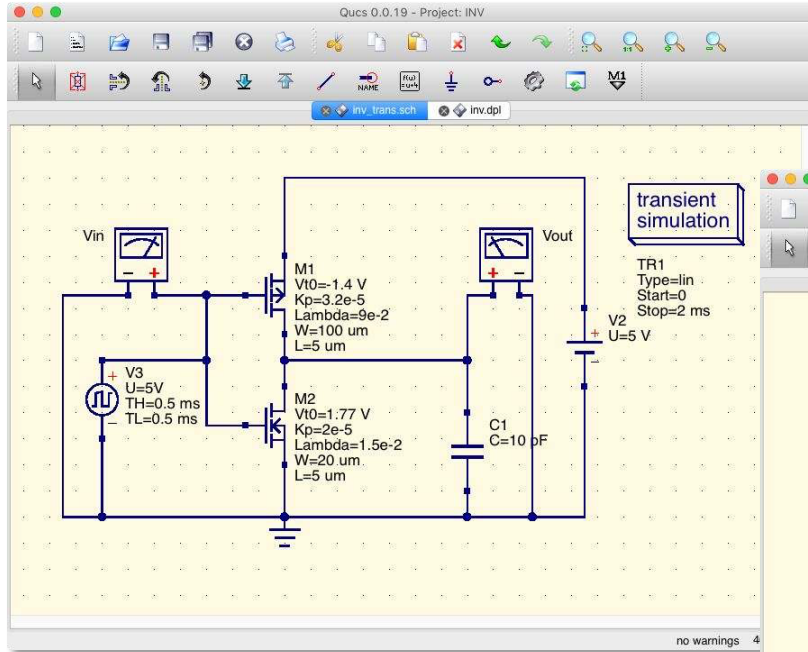
4007 CMOS inverter chip measurement



[REF] <https://espotek.com/labrador>

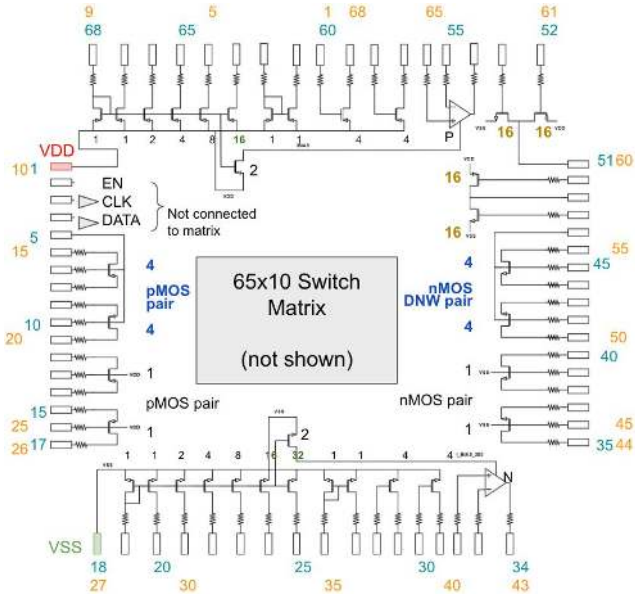
https://archive.fosdem.org/2018/schedule/event/cad_spice/

Qucs: Quite Universal Circuit Simulator

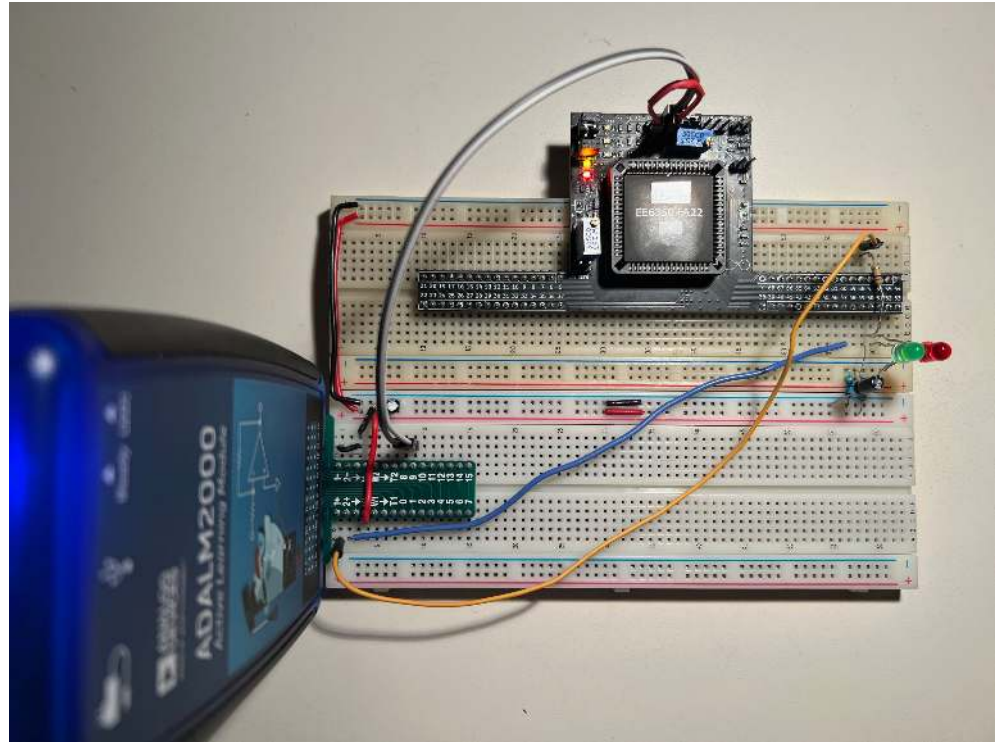


[REF] <http://qucs.sourceforge.net/>

MOSbius Project



The MOSbius chip is fabricated in a foundry 65nm CMOS technology and uses nMOS and pMOS thick-oxide transistors, i.e. the 2.5V I/O devices. It's packaged in a 68-pin PLCC package.



[REF] Peter Kinget leads MOSbius Project <https://mosbius.org/>
Alternative: Andrew Kang's Mini MOSBius <https://tinytapeout.com/news/mini-mosbius/>

IHP Open Source Certificate Courses

Digital Design Course

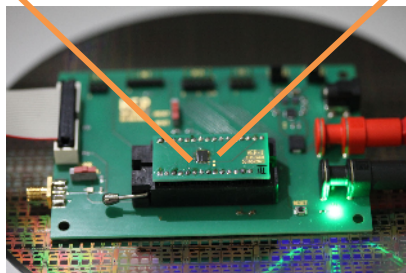
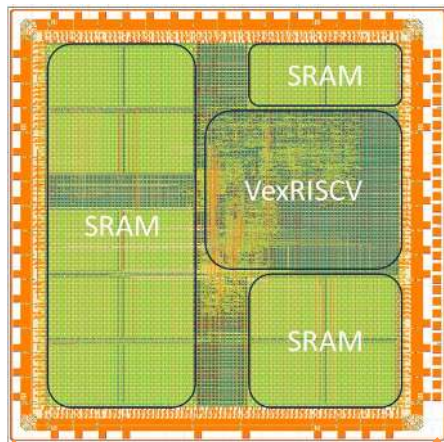
- Full RTL-to-GDSII workflow using OpenROAD and SG13G2 PDK
- Git-based, fully open-source:
<https://github.com/OS-EDA/Course>
- Trial run Feb 2025: 15 on-site participants selected from 85+ applicants
- Feedback integrated via GitHub & live sessions

Analog Design Course

- Git-based, fully open-source:
<https://github.com/IHP-GmbH/IHP-AnalogAcademy>
- Hands-on design with SG13G2 PDK
- Examined Designs: Bandgap, 50GHz PA, SAR ADC
- Tools: Ngspice, Xyce, Xschem, Qucs, Klayout
- Strong emphasis on analog/RF practice
- Focus on layout, verification, and process variation analysis

The Development of this course is funded by the public German project FMD-QNC (16ME083) from BMFTR (Federal Ministry of Research, Technology and Space / Bundesministerium für Forschung, Technologie und Raumfahrt): <https://www.elektronikforschung.de/projekte/fmd-qnc>

IHP early adopter for OSH: Project HEP



Open Security Hardware Module

- Open Processor
- Open EDA
- Open PDK

Main Details

Application	Hardware Security Module
Technology	130nm
Fab	IHP
Type	Prototype
Package	Flip Chip
Dimensions	4610μm x 4580μm (Vex: 1.3mm ² ; SRAM: 10.2mm ²)
Peripherals	UART, SPI, JTAG, GPIO
AES accelerator on the ABP3 bus	(masked AES)

German early adopter OSH project

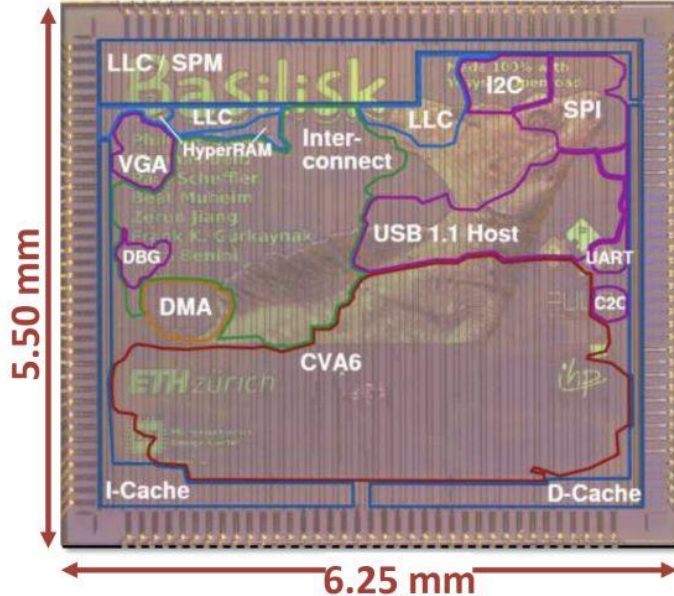
- Start 03/2021
- Initiator for IHP-Open130-G2
- First fully open ASIC TapeOut with IHP-Open130-G2
- Root of Trust extensions for IHP-Open130-G2 planned

REF: [Project GIT](https://github.com/HEP-Alliance) <<https://github.com/HEP-Alliance>>

Project website <<https://hep-alliance.org/>> riscv.org referring the project

Basilisk: Open RTL, Open EDA, OpenPDK

Meet Basilisk: Open **RTL**, Open **EDA**, Open **PDK**



- **Designed in IHP 130nm OpenPDK**
 - 34mm² (6.25mm x 5.50mm)
 - ~5× larger than previous end-to-end OS designs
 - 2.7 MGE total, 1.14MGE logic
 - 24 SRAM macros (114 KiB)
 - 62MHz at nominal voltage (1.2V)
- **RV64GC design runs Linux**
- **Active collaboration with**

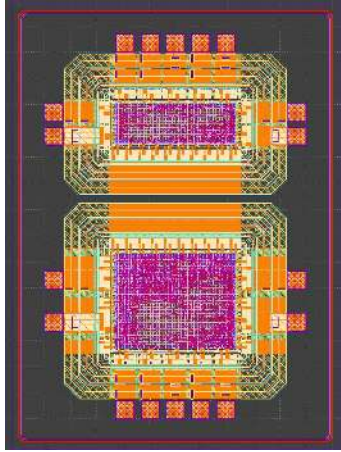


YosysHQ

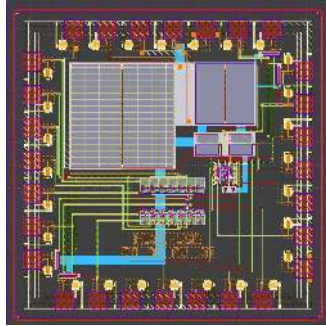
github.com/pulp-platform/cheshire-ihp130-o

OpenPDK MPW: November 2024

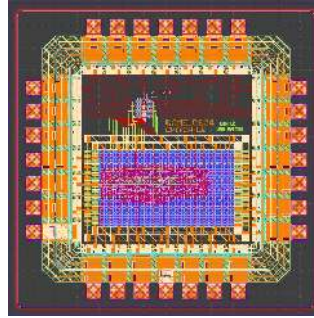
AES masker/unmasked



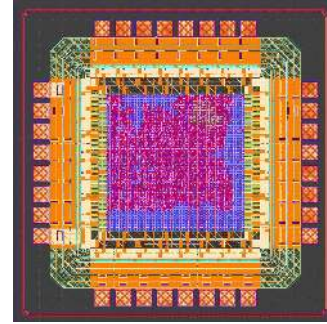
Buck converter



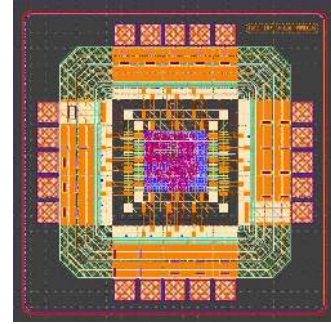
Canelos Workshop



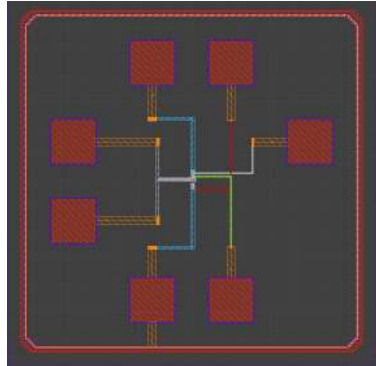
Martin



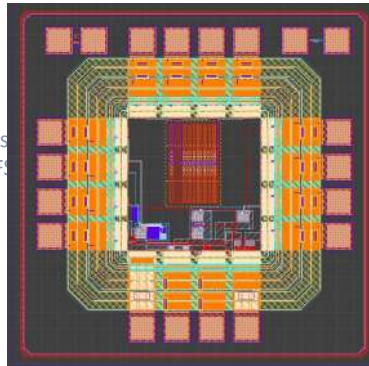
I2c-gpio-expander



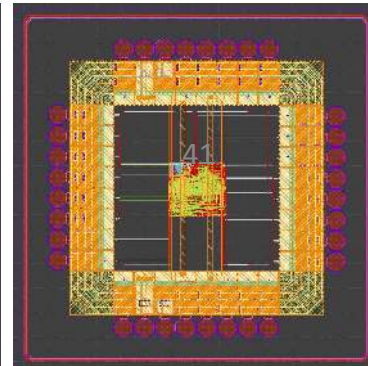
diff_amplifier



mmW_detector

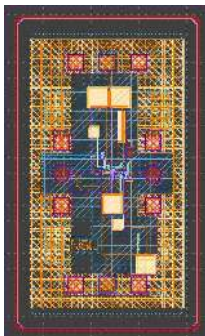


Arlet 6502

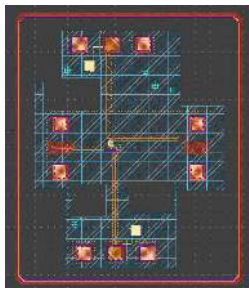


OpenPDK MPW: April 2025 – RF begins

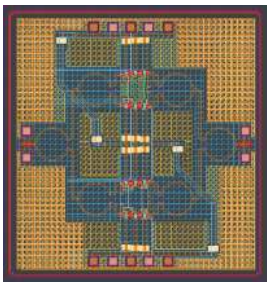
97GHz TIA



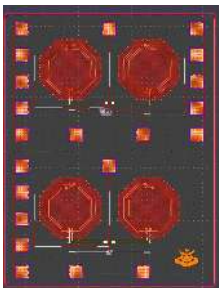
DC to 130GHz TIA



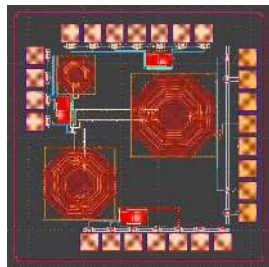
4-way 180GHz PA



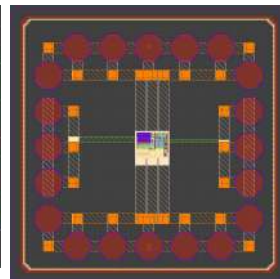
5GHz Mixer



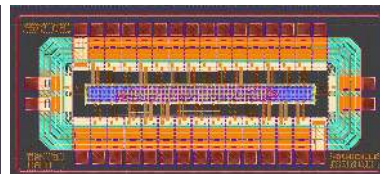
GPS LNA



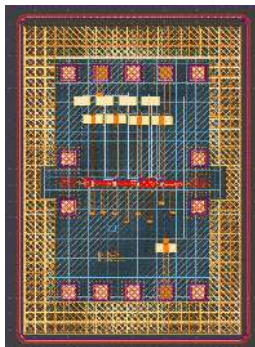
BG - Vref



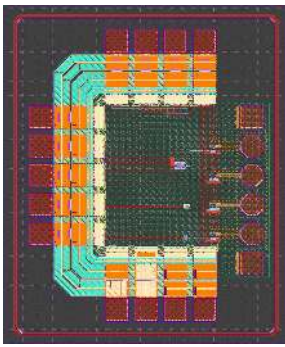
6502 CPU



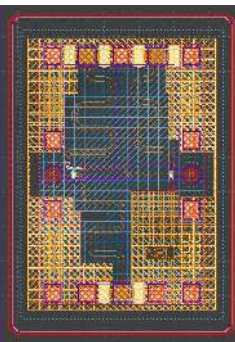
160GHz LNA



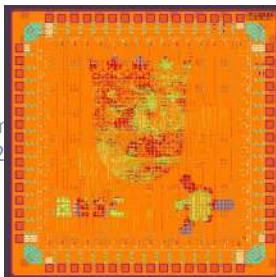
Active L VCO



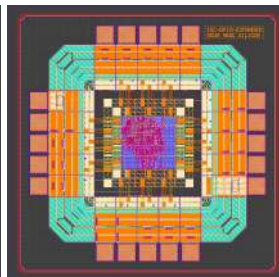
40GHz LN TIA



ElemRV-N

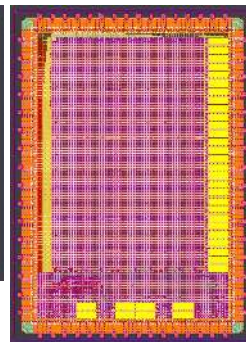


I2c-gpio-expander

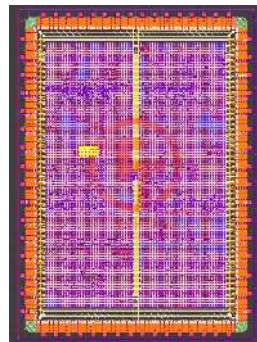


LibreLane Success Stories

Greyhound

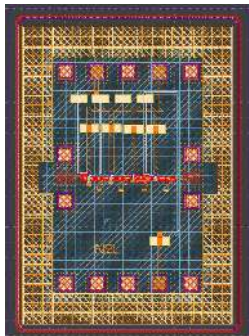


2x TinyTypeout

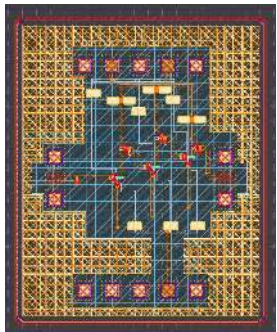


OpenPDK MPW: May 2025 - RF continues

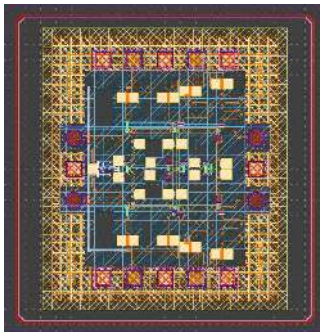
207GHz LNA



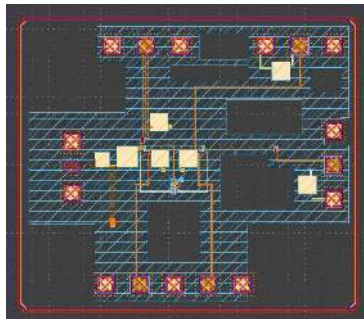
Cascode LNA 107GHz



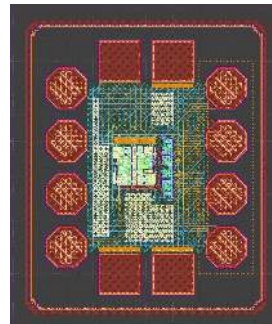
Broadband amp



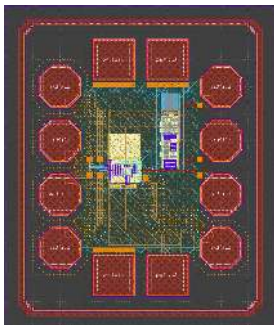
D band power detector



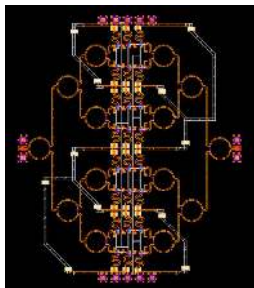
HBT VCO + RO



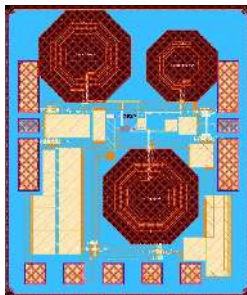
HBT LP amp



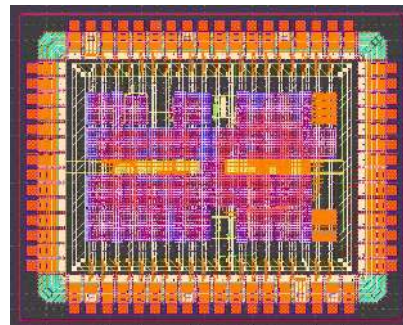
180GHz PA 8 way



LNA 2.45GHz



2x TinyTypeout



Low Cost Open Source MPW Access with IHP 130nm BiCMOS OpenPDK

Terms and conditions

The mentioned prices below refer to the open-source designs, where all the views are compatible with the open source EDA tools.

For customers who do not wish to disclose their IP, we offer participation in the OpenMPW program at a 20% discount off the regular price, as the wafers can be shared with other customers. The turn around processing time is approx. 6 months for SG13CMOS and 8 months for SG13G2. Our/IHP basic offer contains 20 bare die samples. It is also possible to rent the wafer for measurements.

Packaging will be offered on request (additional fee can be applied).

OpenMPW Access at IHP (registration deadline)

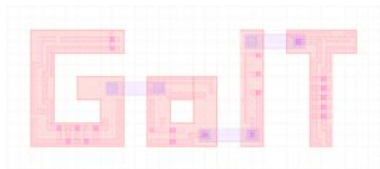
- **CMOS5L** run on 2026-07-13 (2026-06-29)
the initial price is 1500 EUR/mm² and it will scale down to 1000 EUR/mm²
if the total area requested by all customers will be higher than 150 mm²
- **SG13G2** run on 2026-10-06 (2026-09-21)
fully featured G2 with AL BEOL at approx. 2800 EUR/mm²
- **CMOS5L** run on 2026-11-16 (2026-10-26)
new OpenPDK (M1-M4 + TM1) available this 2026 year

Request/reserve your MPW IC Chip area online

<<https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/low-cost-open-source-mpw-access-1>>

What's next?

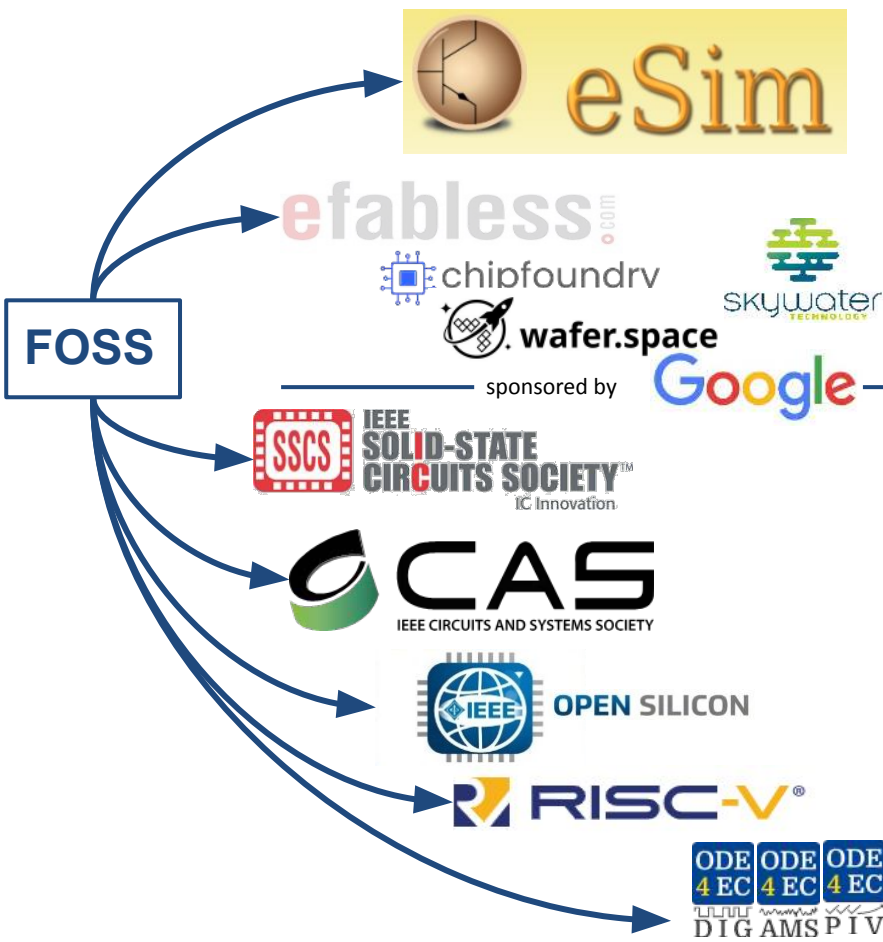
Open Source EDA Roadmap for Europe



- Open-Source EDA Roadmap for Europe, presented at ORConf 2024
- <<https://tinyurl.com/OpenSourceEDARoadmap>>
- Led to HORIZON-JU-CHIPS-2025-IA-EDA two-stage call
 - 20M€ funding from EU, total project 50M€
 - Organized in three sub projects: Digital, Analog, Productivity
 - Currently in Grant Preparation Phase before the kickoff
 - Kickoff in June 2026, more details to follow
- Large consortium <<https://ode4ec.eu/>>
 - Includes broad participation from most open source contributors in EU
 - 24 partners (DIG), 27 partners (AMS), 24 partners (PIV)
 - From 14 Countries:
AT, DK, FI, FR, DE, GR, HU, IT, LT, PT, SI, ES, SE, CH, UK
- Great opportunity to make an open source differentiation



OpenPDK Initiative: Achievements and Current Momentum



FOSSEE eSim offers similar capabilities and ease of use as any equivalent proprietary software for schematic creation, simulation and PCB design, without having to pay a huge amount of money to procure licenses [REF] <https://esim.fossee.in/>



The **IEEE SSCS Pico Program** "Democratizing IC Design" first open-source IC design contest. IC fabrication using **OpenPDK** SKY130, GF180MCU PDK on chipfoundry, Wafer.Space shuttle [REF] <https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program> <https://sscs-ose.github.io/>

The "Universalization of IC Design" CASS (**UNIC-CASS**) program is a structured end-to-end Integrated Circuit (IC) design-to-test experiential learning [REF] <https://ieee-cas.org/universalization-ic-design-cass-unic-cass>

The **IEEE Open Silicon** Initiative (under IEEE R1) is a structured global program aimed at expanding access to microelectronic design education and enabling hands-on chip fabrication through community-led bootcamps [REF] <https://ieee-ceda.org/media/ieee-open-silicon-initiative>

RISC-V is a **free and open source** enabling a new era of processor innovation through open collaboration. Offers a new level of free, extensible software and hardware freedom on architecture, paving the way for the years ahead of computing design and innovation [REF] <https://riscv.org/about/>

Open Source EDA Tools for IC designs <https://ode4ec.eu/>

Acknowledgment

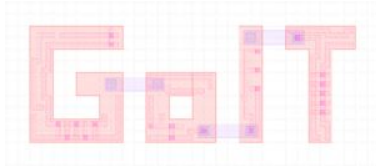
René Scholz, Sergei Andreev, Krzysztof Herman, Alexey Balashov, Mario Krattenmacher, Pascal Kuthe, Markus Müller, Jean-Michel Sallese, Matthias Bucher, Daniel Tomaszewski, Guilherme Torri, Bal Virdee, Mike Brinson, Matthias Köfferlein, Thorsten Liebig, Jan Taro Svejda, Al Davis, Felix Salfelder, Francesco Lannutti, Paolo Nenzi, Dietmar Warning, Holger Vogt, Murat Eskiyeerli, Eric Keiter, Jason Verley, Luca Benini, Frank Gurkaynak, Luca Alloatti, Thomas Kramer, Marie-Minerve Lauerat, Jean-Paul Chaput, Kannan Moudgalya, Sumanto Kar, Harald Pretl, Boris Murmann, Mehdi Saligane, Matt Venn, Tim Ansell

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- ETH Zurich + JKU Linz + IIT Bombay, all the open source community
- German public funded projects:
 - VE-HEP (16KIS1339K) <https://elektronikforschung.de/projekte/ve-hep-1>
 - IHP Open130-G2 (16ME0852) <https://www.elektronikforschung.de/projekte/ihp-open130-g2>
 - FMD-QNC (16ME0831) <https://www.elektronikforschung.de/projekte/fmd-qnc>
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Open-Source EDA Roadmap for Europe



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MOS-AK: 2026/27 Events

- Aalto Microelectronics Fair (FI) March 20, 2026
- OpenPDK at Spanish Chip Chairs, Uni. Malaga (SP) May 27, 2026
- OpenPDK/MIXDES Workshop, Poznan (PL) June 25-27, 2026
- OpenPDK at FSiC, Ljubljana (SI) July 6-8, 2026
- 10th Sino MOS-AK, Wuxi (CN) Aug. 27-28, 2026
- 23st MOS-AK at 52st ESSERC, Palma de Mallorca (SP) Sept 7-10, 2026
- OpenPDK ODE4EC-AMS at ORConf, Ghent (B) Sept. 14-15 2026
- Special OpenPDK Session at IEEE ICTA'26 (SG) Oct. 21-23, 2026
- MOS-AK Silicon Valley Workshop (*online*) Dec, 2026
- OpenPDK at ASP-DAC, Tokyo (J) Jan. 25-28, 2027
- OpenPDK at EDTM, Fukuoka (J) March 8-11, 2027