Advances in Qucs-S schematic capture for compact modelling and simulation

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Proposed compact device modelling and circuit simulation tool-set based on FOSS Qucs-S, Ngspice, Xyce, VerilogAE, OpenModelica and Octave packages
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Qucs-S/Xyce Modular Libraries: New schematic symbols and models

Test library for Qucs-S/Xyce

Points to note:
1. Component and device models in this library are not hard wired into Qucs-S program code;
2. Xyce SPICE dialect becomes the Qucs-S/Xyce netlist format;
3. The functionality of each schematic symbol is set by Xyce SPICE code.

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Qucs-S/Xyce Modular Libraries: Schematic symbols and global variables; 1

Extended EDD diode model:
Diode Id/Vd characteristic constructed from a numeric Table passed as a subcircuit parameter, allowing the diode model current to be set by the voltage across EDD internal nodes p1 and p2.

SPICE diode model

Global parameter dcsweep is Equivalent to a variable that can be changed during simulation.

dcsweep value changed by .dc
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Qucs-S/Xyce Modular Libraries: Schematic symbols and global variables; 2

XYCE script

XYCESCR1
SpiceCode=
.global_param dcsweep = 0.0
.global_param res = 1e-3
.dc lin dcsweep 0.5 1.2 0.02
.step lin res 0.01 1.0 0.2
.print dc format=std file=dc.txt dcsweep + (xammeter1.vprobe) v(xprobe_v1;p1)
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Qucs-S/Xyce Modular Libraries: Schematic symbols and global variables; 3

(a) d_td_edd2
v_p=50e-3
v_v=370e-3
i_p=4.2e-3
i_v=370e-6
v_pp=525e-3
cp=10e-12
rs=1.0
p_temp=27
ls=1e-9

(b) r_linear4
r=rgmin
Pc1
Num=2

(c) ammeter1
voltmeter1

INCLUDE SCRIPT

INCLSCR1
SpiceCode=
.param rgmin=1e9
.param p_q=1.50217646e-19
.param p_k=1.3806503e-23
.param tempK=(p_temp+273)
.param vth=(p_k*tempK)/p_q

dTd_edd3
v_p=50e-3
v_v=370e-3
ip=4.2e-3
iv=370e-6
vpp=525e-3
cp=10e-12
rs=1.0
p_temp=27
ls=1e-9

XYCESCR1
SpiceCode=
.global param dcsweep=0.0
.ac dec 20 1 1e5
.step dcsweep 0.1 0.3 0.01
.lin format=touchstone sparcalc1 linetype=z
.print ac format=std file=sparam.txt dcsweep+
+zi(1,1) zi(1,1) zm(1,1) zp(1,1)

xyover
xover
-200
-400
0
1
10
100
1e03
1e04
1e05
FREQ (Hz)

-200
-400
0
1
10
100
1e03
1e04
1e05
FREQ (Hz)
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Qucs-S/Xyce Modular Libraries: CMC Verilog-A standardized device models

Xyce Verilog-A HICUM10 BJT model with default parameters - except where changed in symbol parameter list

INCLUDE SCRIPT

XYCE script

XYCESCR1
SpiceCode=
global_param sweep_v=0.0
global_param sweep_i=0.0
dc lin sweep_v 0 1.2 0.02
.step lin sweep_i 1u 10u 1u
.print dc format=std file=dc.txt
+sweep_v i(xammoterv1:1vprobo)
+v(xvvoltmeter1:1vtron)

i_dc1
dc=(sweep_v)

v_dc2
dc=(sweep_v)

q_hicumi0_rnpn
DTOH=1.1e-18
RC1=520
RCX=0.5
RE=0.05
T0=16.2e-12
TBVL=3.2e-12
THCS=140e-12
VPT=43

q_hicumi0_rnpn
DT0H=1.1e-18
RC1=520
RCX=0.5
RE=0.05
T0=16.2e-12
TBVL=3.2e-12
THCS=140e-12
VPT=43

voltage

ammmeter1

voltage

voltage

voltage
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Qucs/S/Xyce Modular Libraries: Tunnel diode netlist code

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*Xyce model*

SPICE subcircuits

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Subcircuit

X call statements

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Xyce control and data output statements

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Device count summary

<table>
<thead>
<tr>
<th>Level</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>3</td>
</tr>
<tr>
<td>C</td>
<td>3</td>
</tr>
<tr>
<td>G</td>
<td>1</td>
</tr>
<tr>
<td>L</td>
<td>1</td>
</tr>
<tr>
<td>R</td>
<td>4</td>
</tr>
<tr>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

Total Devices 14
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Qucs-S/Xyce/Modelica: Multi-HDL schematic capture and code generation; 1

Symbol and SPICE component type
Multiple additional information lines: these allow long strings of SPICE and other HDL data to be passed to Xyce netlists to form a component specification
Qucs-S component template: built into C++ GUI code

SPICE netlist generated by Qucs-S GUI for Xyce simulation

Qucs-S post-simulation data visualization

Xyce SPICE netlist with Verilog-A embedded HDL code

Note: lines with an * in column 1 are treated by Xyce as documentation COMMENTS

Xyce schematic drawing

Qucs-S schematic drawing

Qucas 0.8.22 C:\Users\brini.qucks-s\METRasSamSlides_prjtest\LCRXyce.sch
.SUBCKT NGenSub1_net0 n2 R1 L=100n C=0.1u
.include "disciplines.vams"
.include "constants.vams"
.module NGenSub1 n2, R1;
.inout n2, R1;
.electrical n2, R1, n3;
.parameter real R=1.5;
.parameter real C=100e-6;
.analog begin
   C1 C(n2 R1)
   C_Line 2*n va (n2, n3) <= ddt(C V(n2, n3));
   R1 R(n2, R1)
   Line 2*n va (n3) <= V(n3);R1;
   ENDS
   V1 in 0 dc 0 ac 1
   XLCRI n in n, out NGenSub1 R=1.5 L=100u, C=100n
   AC lin 1000 4x4 64
   PRINT AC format=std file=ac.txt
   + V(i_Sn) V(i_out) Vm(in) Vm(out)
   - VP(i_Sn) VP(i_out)
   =va end =va endmodule

Xyce

Xyce SPICE and Verilog-A subcircuit

.include "disciplines.vams"
.include "constants.vams"
.module NGenSub1 n2, R1;
.inout n2, R1;
.electrical n2, R1, n3;
.parameter real R=1.5;
.parameter real C=100e-6;
.analog begin
   C1 C(n2 R1)
   C_Line 2*n va (n2, n3) <= ddt(C V(n2, n3));
   R1 R(n2, R1)
   Line 2*n va (n3) <= V(n3);R1;
   ENDS
   V1 in 0 dc 0 ac 1
   XLCRI n in n, out NGenSub1 R=1.5 L=100u, C=100n
   AC lin 1000 4x4 64
   PRINT AC format=std file=ac.txt
   + V(i_Sn) V(i_out) Vm(in) Vm(out)
   - VP(i_Sn) VP(i_out)
   =va end =va endmodule

ENDS
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Qucs-S/Xyce/Modelica: Multi-HDL schematic capture and code generation; 2

```
function ExtractVa(ModuleName);
% An Octave function to extract a Verilog-A module from a
% Xyce/Ngspice netlist.
% (C) 2021 Mike Brinson; Published under GNU General
% Public License V2 or later.
% ==============================================================
% netlistName = strcat(ModuleName, ".cir");
% VaModuleName= strcat(ModuleName, ".va");
% fidread=fopen(netlistName,"r"); fidWrite=fopen(VaModuleName,"w");
% ==============================================================
line=fgetl(fidread);
while 1
  if strcmp(line,""va")
    line=[line(4:end)];
    fprintf(fidWrite,"%s\n",line);
  endif
  line=fgetl(fidread);
  if eof(fidread)
    break
  endif
endwhile
fclose(fidread); fclose(fidwrite);
display("Verilog-A module extraction finished.\n"); return
```
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Qucs-S/Xyce/Modelica: Multi-HDL schematic capture and code generation; 3

The tunnel diode model revisited

Tunnel Diode compact model example

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