

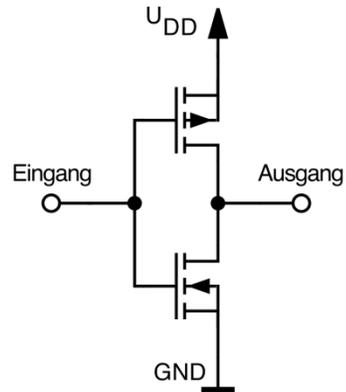
Ngspice circuit simulator

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ngspice – what is it ?

Circuit simulator that numerically solves equations describing (electronic) circuits made of passive and active devices for (time varying) currents and voltages

Open source successor of venerable spice3f5 from Berkeley



the circuit

```
CMOS inverter

.include ../bsim4soi/nmos4p0.mod
.include ../bsim4soi/pmos4p0.mod
.option TEMP=27C

Vpower VD 0 1.5
Vgnd VS 0 0

Vgate Ein VS PULSE(0 1.5 100p 50p 50p 200p 500p)

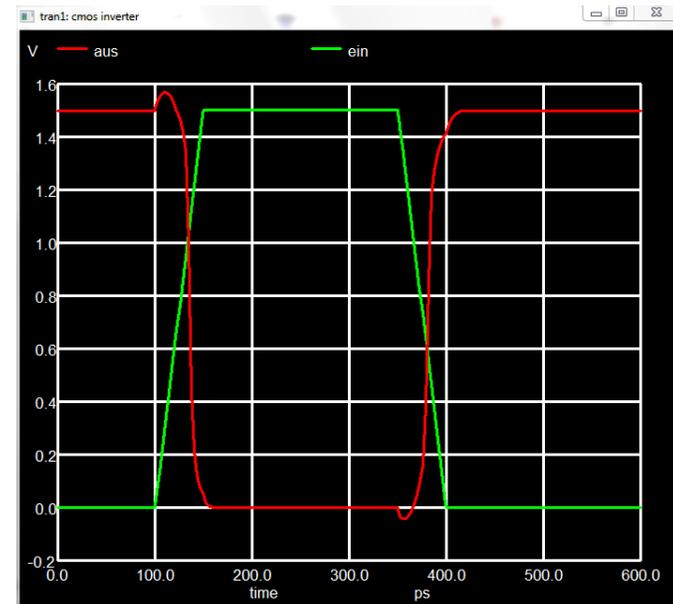
MN0 Aus Ein VS VS N1 W=10u L=0.18u
MP0 Aus Ein VD VS P1 W=20u L=0.18u

.tran 3p 600ps

.control
  run
  plot Ein Aus
.endc

.END
```

the input



the output

The two major application areas

PCB design support

Circuits are made with a mix of ICs and discrete components

Requirements:

Comfortable user interface (offered by third parties)

PSPICE and LTSPICE model compatibility

KiCad, Eagle, Altium, PartSim, Qucs-S, CoolCAD, PSIM, WeSpice ...

IC design support

Circuits are made of (MOS) transistors and (parasitic) passive components

Requirements:

BSIM 3, 4, BULK, CMG models etc.

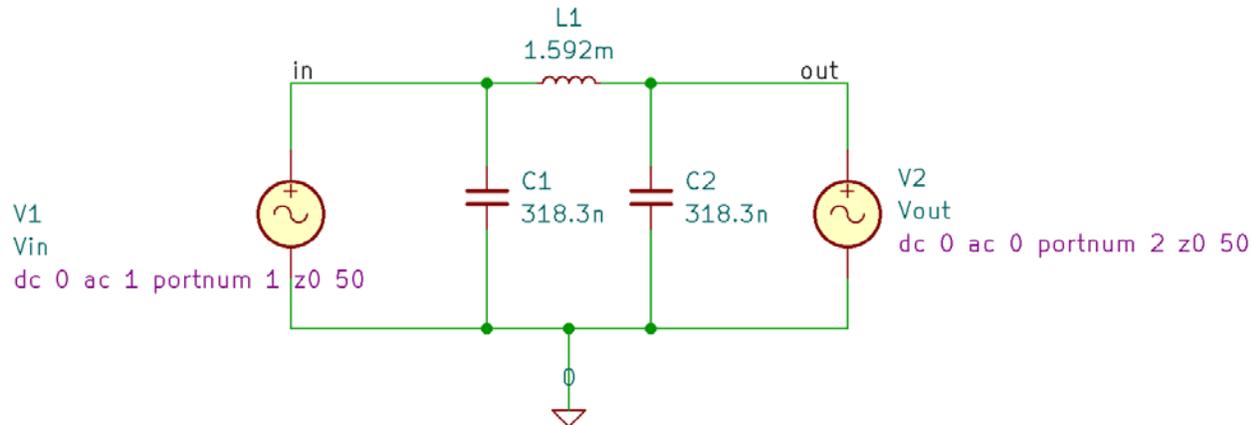
Large circuit capability, speed

HSPICE PDK compatibility

gEDA, Yosys, efabless, Isotel, Google/Skywater PDK, XSCHEM

Current developments – towards ngspice-37

RF simulation capability: determining multi-port S parameters



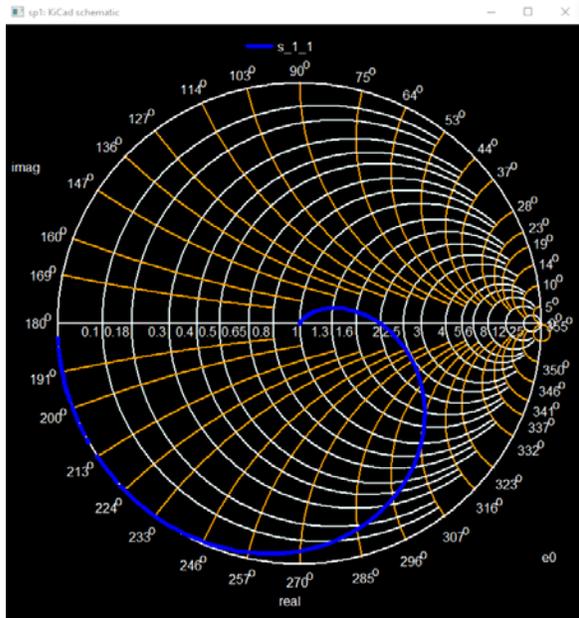
V1
Vin
dc 0 ac 1 portnum 1 z0 50

V2
Vout
dc 0 ac 0 portnum 2 z0 50

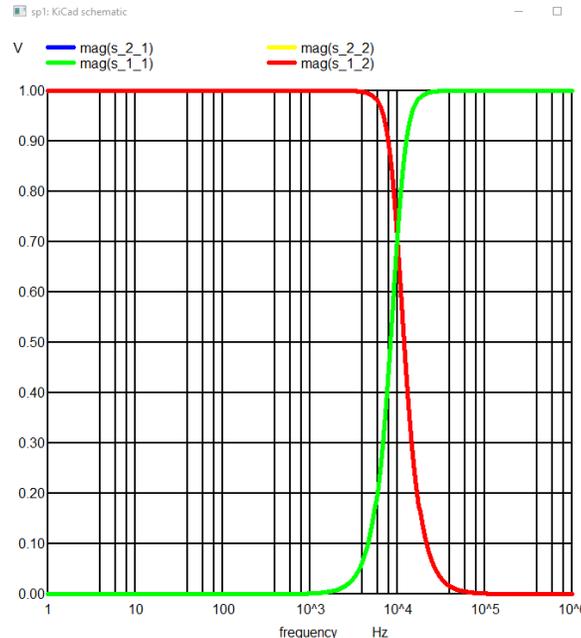
Ports as voltage source option

New command `.sp dec 100 1 1e6 0`

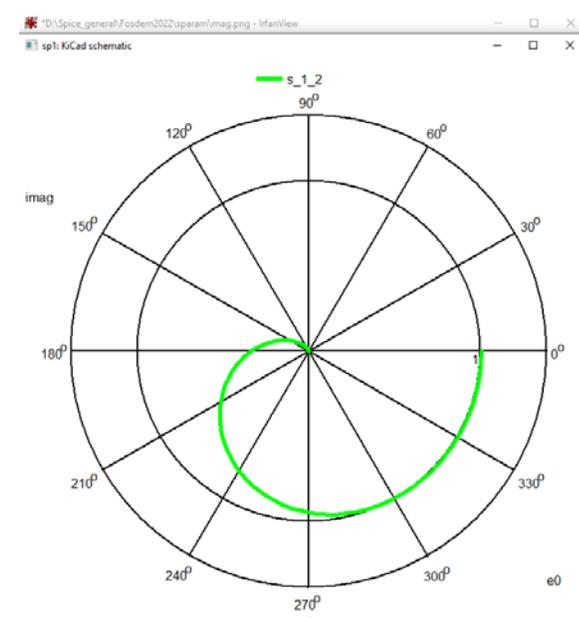
Various plotting and saving options



Smith plot



Magnitude plot



Polar plot

Current developments – towards ngspice-37

XSPICE memory management

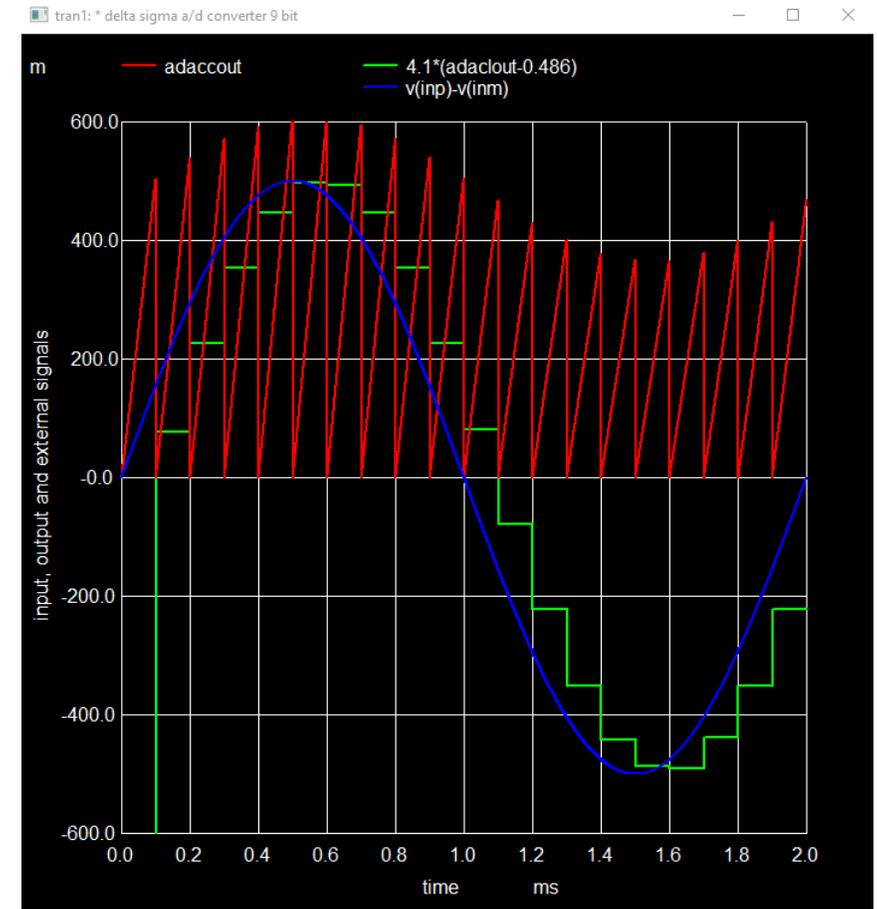
Optimize internally the re-use of allocated memory for digital event nodes

Dramatically reduce memory consumption during simulation

Example: basic $\Sigma\Delta$ A/D converter

Memory consumption reduced from 391.1 MBytes down to 14.6 Mbytes

XSPICE is now ready to support mixed-signal simulations
A first step will be supporting discrete digital devices like 74... and 40... series



Development items under preparation 1

Verilog-A capability

Obtain a new model compiler to read modern device models into ngspice, successor to adms (use the new compiler under development at TU Dresden)

Long term goal: Simulate complete analog-digital systems which are described in Verilog/Verilog-A

KLU matrix solver

Add KLU matrix solver, allow selection of venerable Sparse 1.3 or KLU. Simulation speed-up of large circuits (e.g. using Skywater PDK) is expected.

IBIS

Signal integrity simulations, using vendor provided IC interface descriptions

ToDo: Parsing the IC interface data, setting up driver and receiver circuits, obtaining interconnection models, simulating, presenting the results

A cooperation between KiCad and ngspice

Development items under preparation 2

Ngspice interface

Vastly improved human interface to simulator, based on KiCad (simulator control, schematic entry).
Another cooperation between KiCad and ngspice.

U devices

Make ngspice read PSPICE or μ Cap compatible digital devices, like models for 74... and 40... series