A Stack-Based Routing methodology for nanometric CMOS Devices

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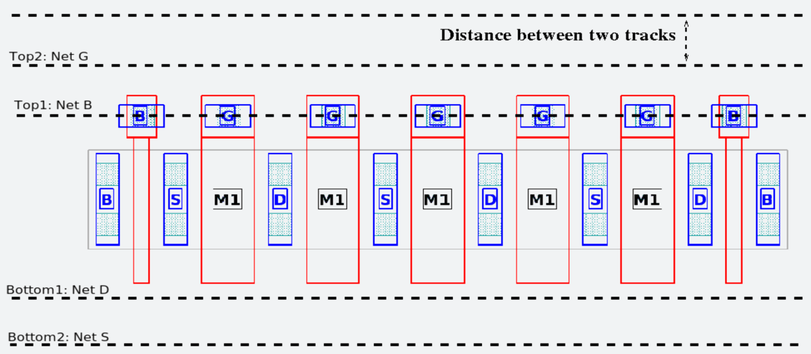
Target: Procedural routing implemented in our nanometric layout generation tool for analog devices.

Application: The differential pair device: interdigitated, symmetrical, M2-Module and 2D-Common Centroid styles.

1 Intra–Stack Routing Methodology

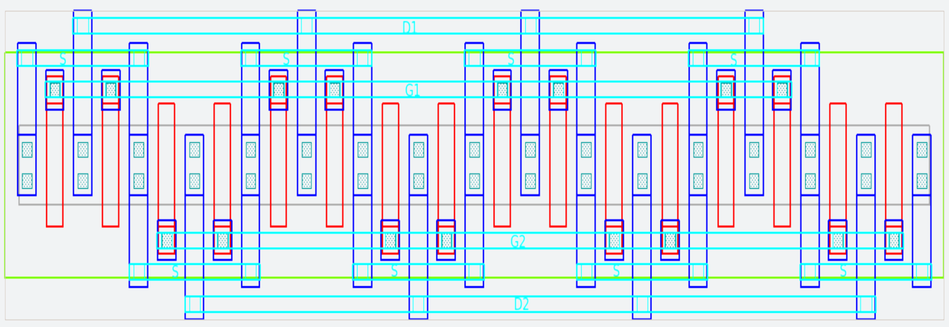
I. Idea:

a. Reserved tracks for routing the nets of the stacks.
b. Net by Net ex: D1, D2, S, G1, G2, .. etc.
c. Pattern: Comb, Serpentine or mixed.
d. Routing is kept inside the stack's width.

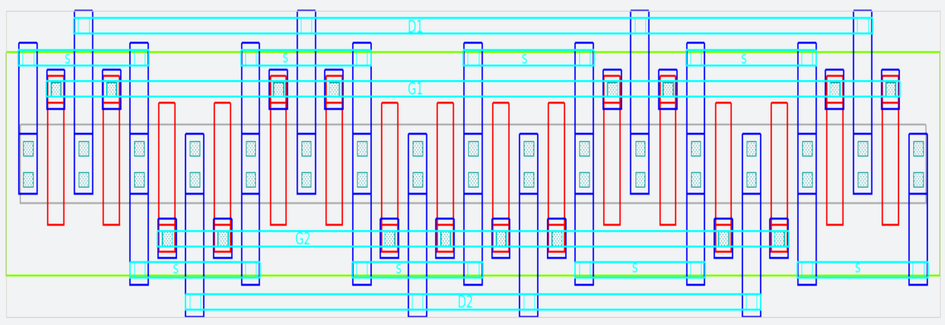


One stack with reserved tracks.

II. Examples:



a. Differential pair interdigitation style



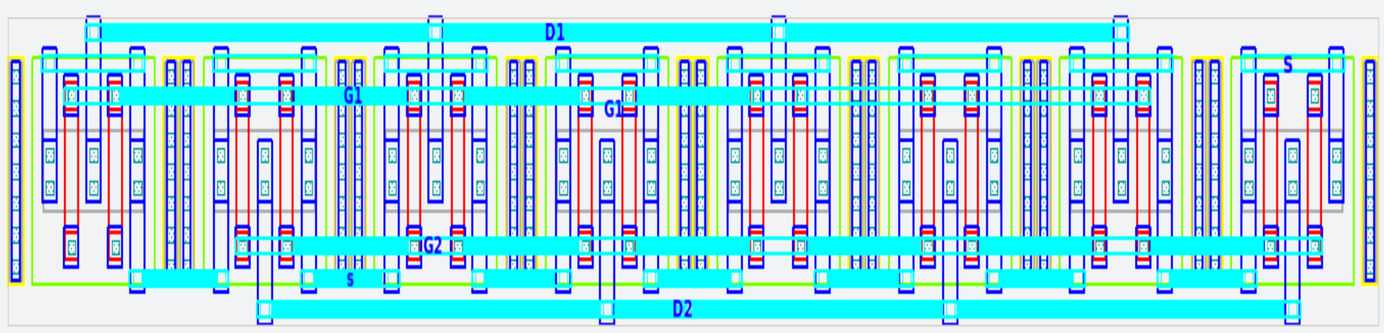
b. Differential pair symmetrical style

2 Inter–Stack Routing Methodology

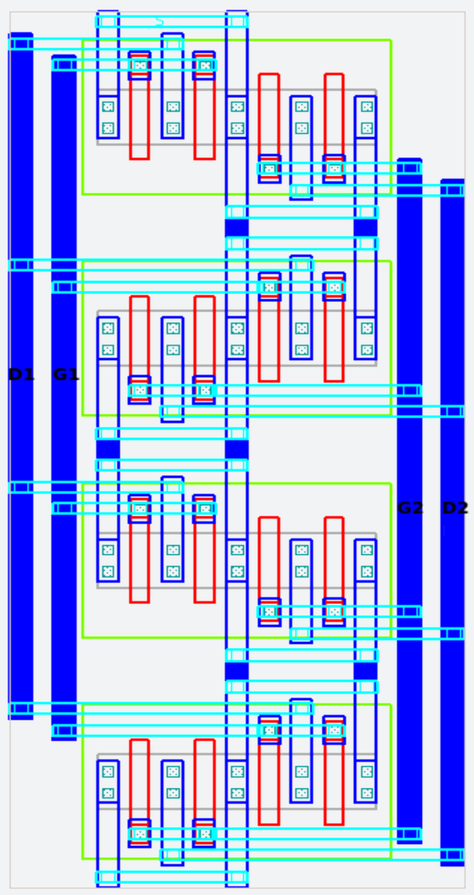
I. Idea:

a. A set of intra-routed Stacks.
b. Segment to segment routing.
c. Pattern: Line, L-shape, U-shape or Z-shape.
d. Routing performed around and between stacks.

II. Examples:



a. Differential pair M2 module style.



b. Differential pair 2D common centroid

3 Parameters for compact modeling:

Automatic layout-dependent computation:

- Style parameters ex: M, NDint, NDext, NSint, NSext, .. etc
- Diffusion parameters: As, Ad, Ps, Pd.
- Stress effect parameters: Sa, Sb, .. etc
- Routing parameters: Parasitic capacitors and resistances

$$\mu_{eff} = \frac{1 + \rho_{\mu eff}(S_a + S_b)}{1 + \rho_{\mu eff}(Sa_{reff} + Sb_{reff})} \mu_{eff0}$$

$$V_{sat} = \frac{1 + K.\rho_{\mu eff}(S_a + S_b)}{1 + K.\rho_{\mu eff}(Sa_{reff} + Sb_{reff})} V_{sat0}$$