

Introduction to Accelicon's Modeling Tools And Services



Accelicon Technologies, Inc.

- Founded by Xisheng Zhang in July, 2002
- Head office in Cupertino, CA, US
- Full time employees 27, contractor 5.
- Well-known technical adviser board
 - SPICE Modeling expert (BSIM4, PSP and Mextram)
 - Analog/RF designer
 - EDA experts in placement/routing



Expertise from Many Years Experience

Key Team Members

- Dr. Xisheng Zhang
 - President, was VP of R&D, Celestry
- Tim Smith
 - CEO, was VP of Sales, Cadences
- Dr. Xiaolan Wu
 - VP of Marketing, was Director of Marketing, Cadence
- Yanfeng Li
 - Manager of SPICE modeling, was Principle Engineer of PDF
- Yuping Wu
 - Manager of Analog layout group, was Technical Leader of Synopsys
- 22 R&D engineers, many from top universities of China

15 years

Expertise



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Selected Customer List

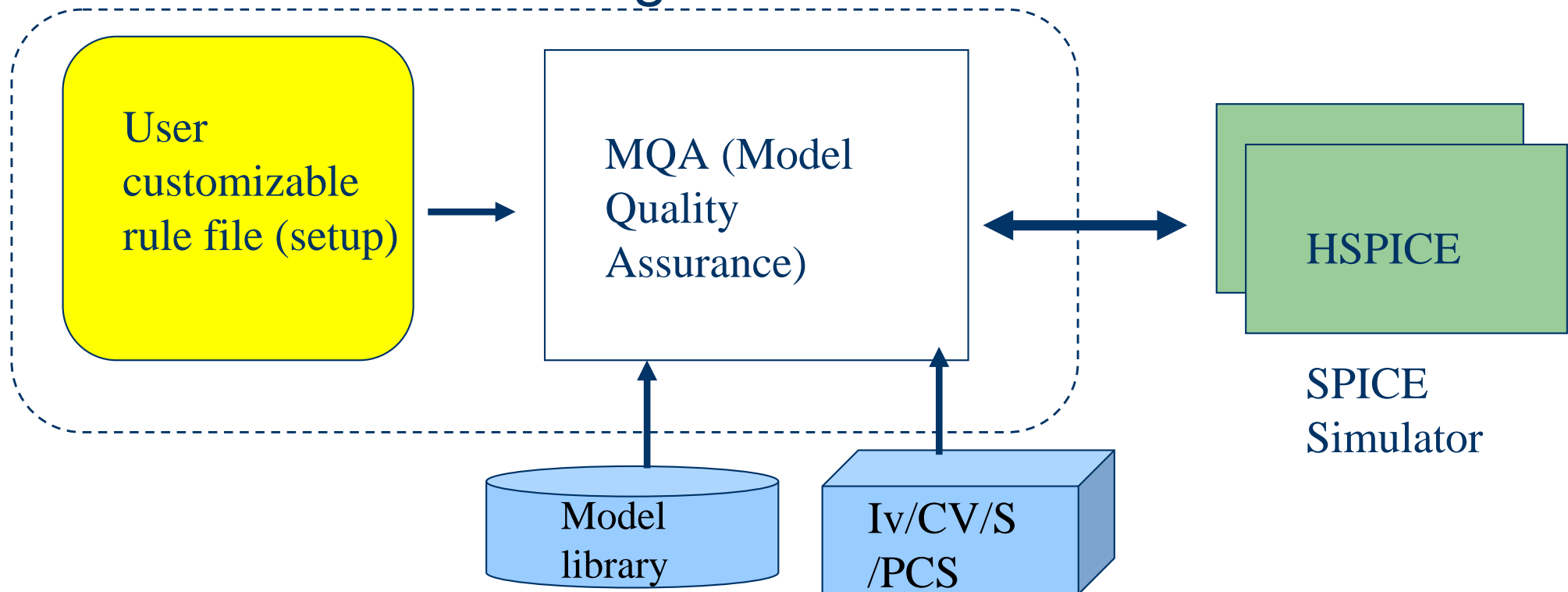


Accelicon's MQA

- Turn-key, fully automated model validation solution for IC designer and modeling engineers.
- Market leader.
- IBM, AMD, Infineon, Sony, Qualcomm, AMIS, Xilinx, Altera and many others use it very heavily in their daily work.
- It provides a great platform to accommodate all user's model QA and validation routines.

Accelicon's MQA

- Turn-key, fully automated SPICE model validation solution for IC designer

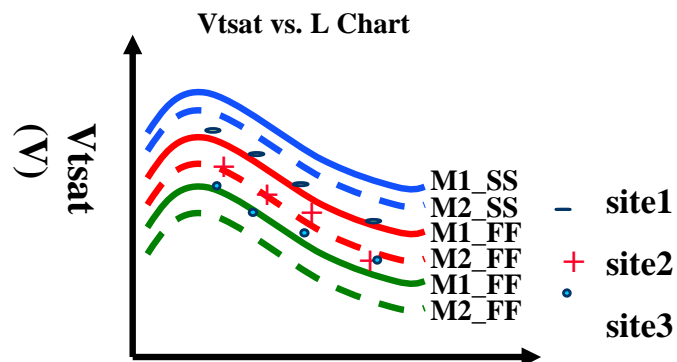


Why MQA (I)

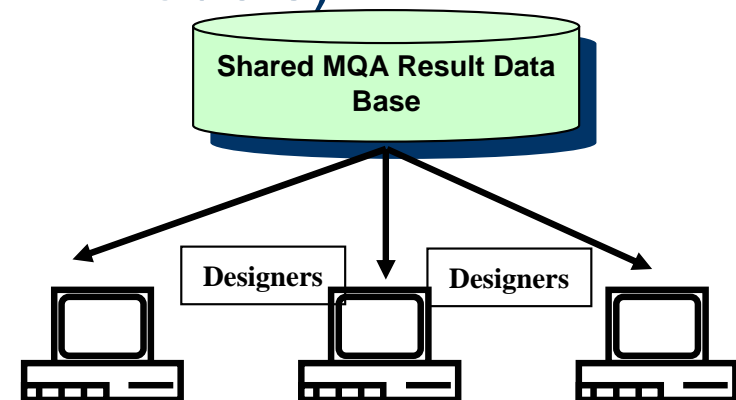
- Accuracy
 - Validate Foundry's generic SPICE model (digital model) vs. customer's special design application
 - Process variations (corner), temperature, yield analysis
- Comparison
 - Foundry's revision of model
 - Different foundries, technology nodes
- Documentation
 - Design documentation for new technology

Why MQA (II)

- Flexibility is the key!
- Open environment allows user to build and automate QA routines for new models and new methodologies.
- Unique data structure eases model data sharing.
- Provide a flexible platform for user to develop QA and documentation procedures for various models (SPICE models, backend models, and DFM models).

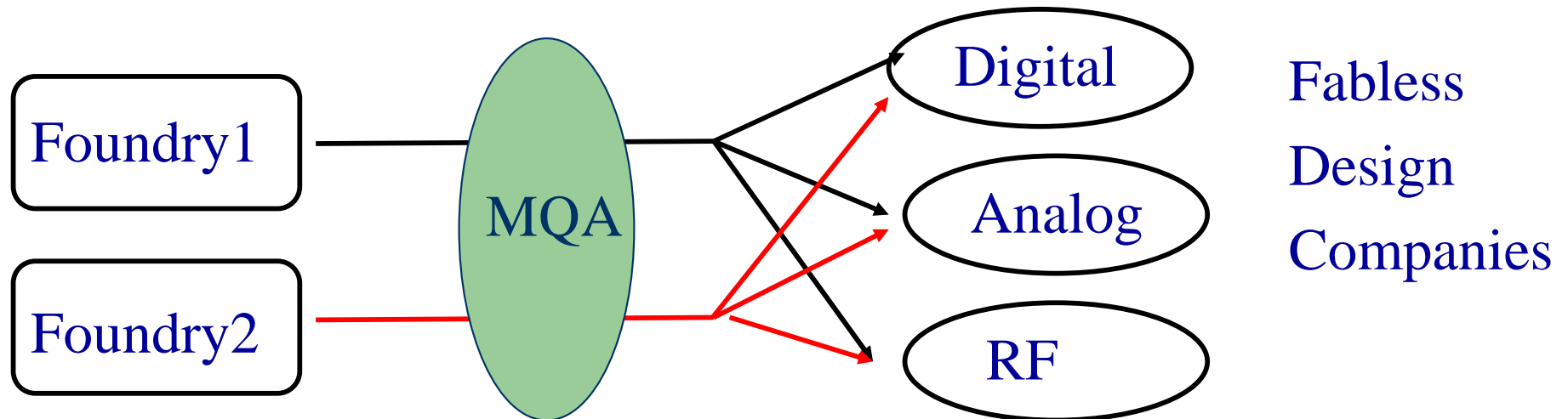


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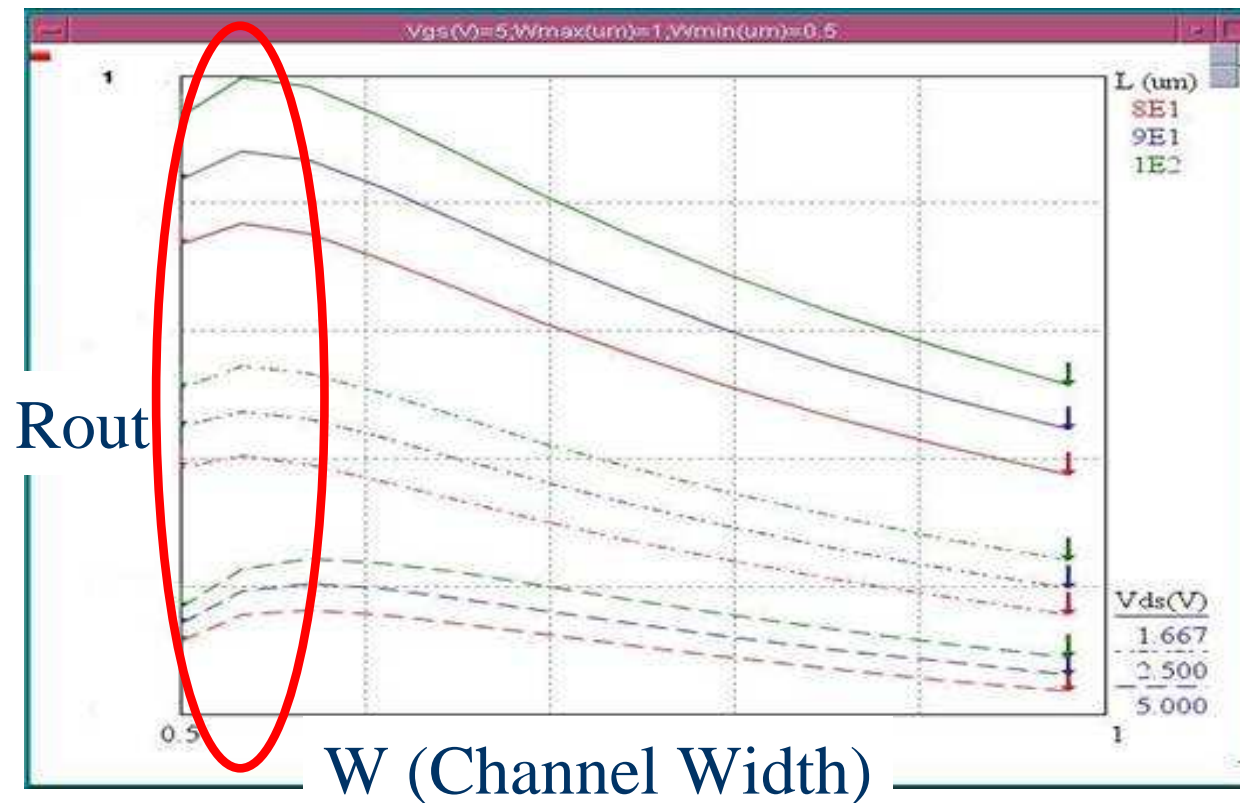
Modeling in Foundry/Fabless

- Model generator (foundry) and model user becomes more insolated to each other
- Foundry's generic model vs. different design applications

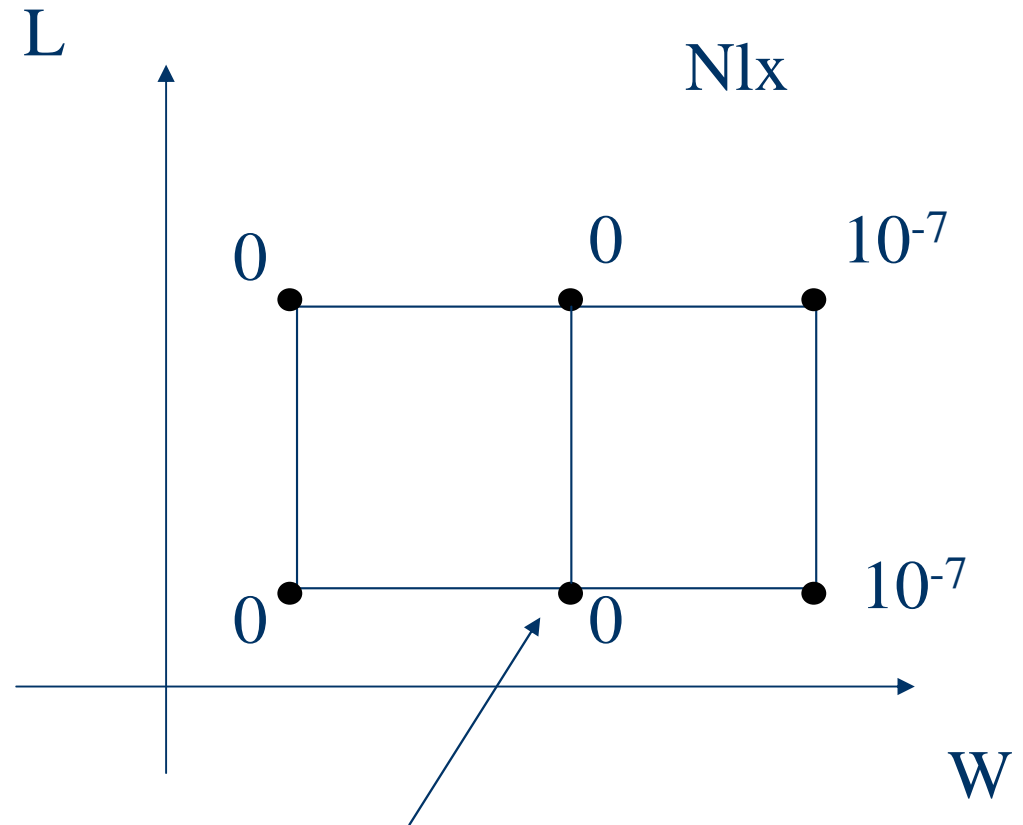
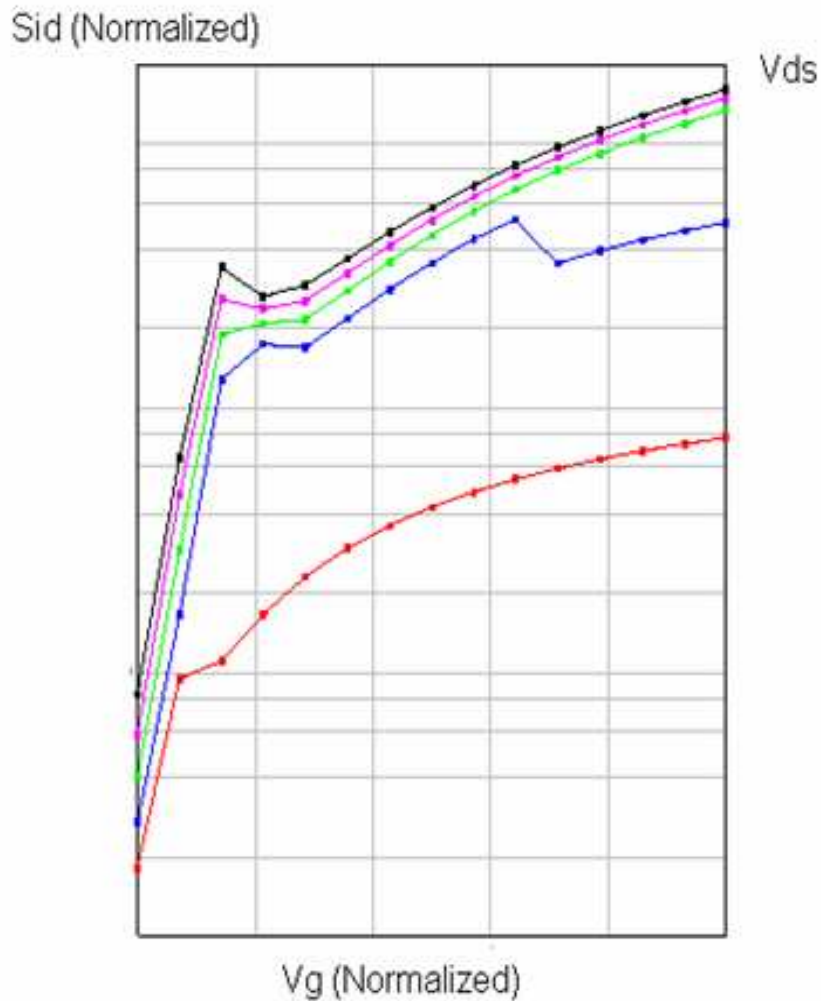


Example of Problematic Model Card

- Rout vs W is not right for long and narrow device



Example of Problematic Model Card (II)



Spectre calculation result = -1.19E-13.
Report a warning

MQA's Basic Facts

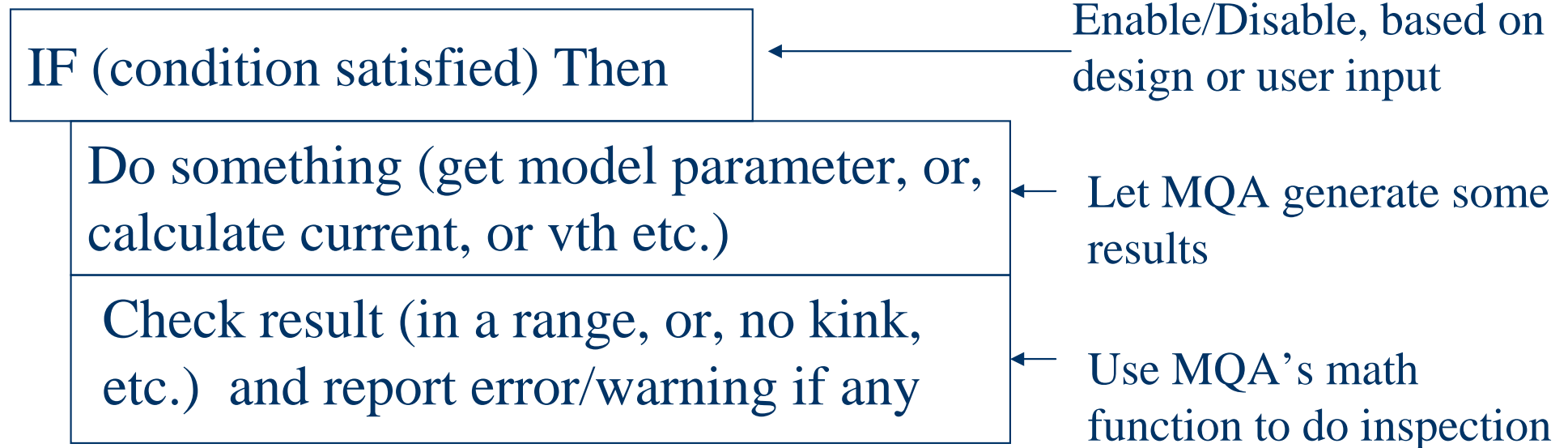
- Written using Java, run in every platform
- Support all compact models supported by commercial simulators.
 - MOS: Bsim3/4, PSP, HiSIM, BsimSOI and sub-circuit models.
 - BJT: GP, Mextram, others (Black box testing)
 - Resistor, Capacitor, Inductor, and other passive elements
 - Support any circuit block validations
- Support all popular simulators.
- Support different measurement formats
 - IV, CV, S, Noise, ET
 - Different file formats from different tools

MQA's Main Features

- Rule driven model validation
 - Knowledge based rule, and check functions
- Flexible Interface
- Run time comparison
- Model report function
- Data management and data sharing
- Model Advisor

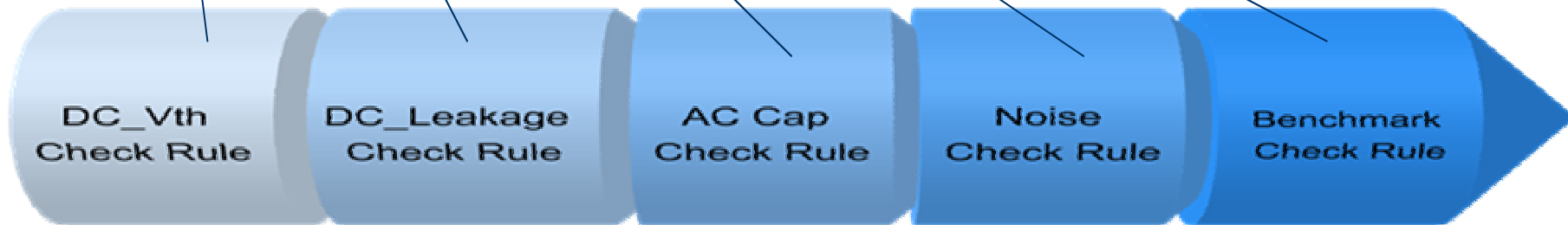
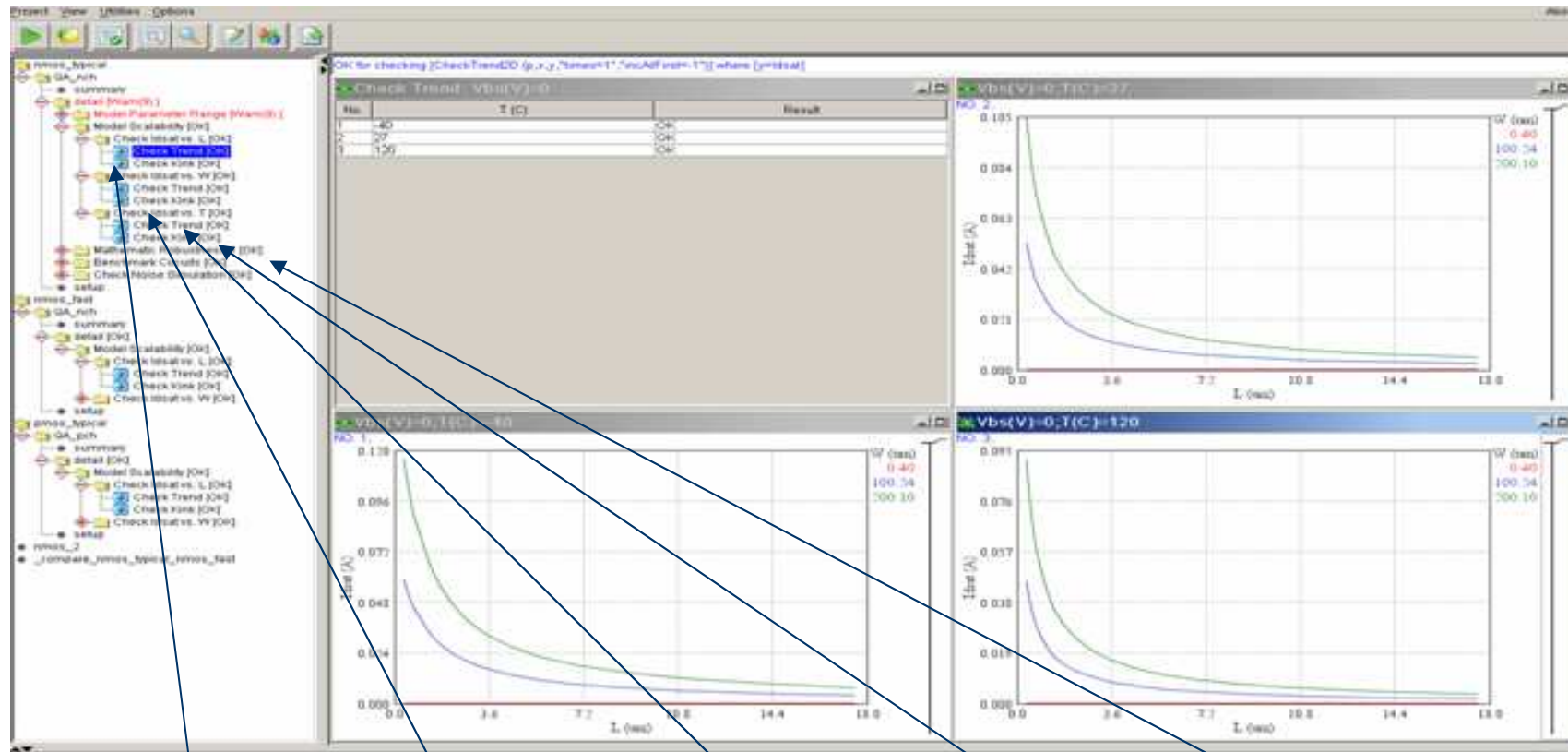
Rule File for Model Validation

- Contain many rules, knowledge based
- One rule check one specific characterization of model. The structure of one rule



Users can write their own rules

Knowledge Based Rule Driven QA

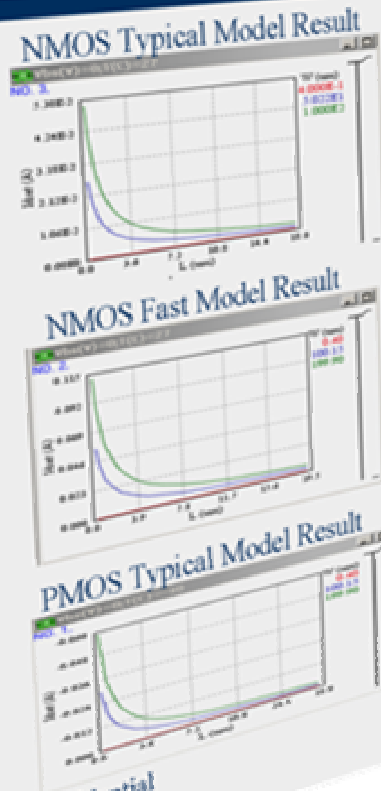


Flexible Interface

- Rule driven and fully customizable.
- Support batch mode.
- User customizable targets and check functions.
- Easy to support new models.
- Easy to adjust to any QA flow.

Run Time Comparison

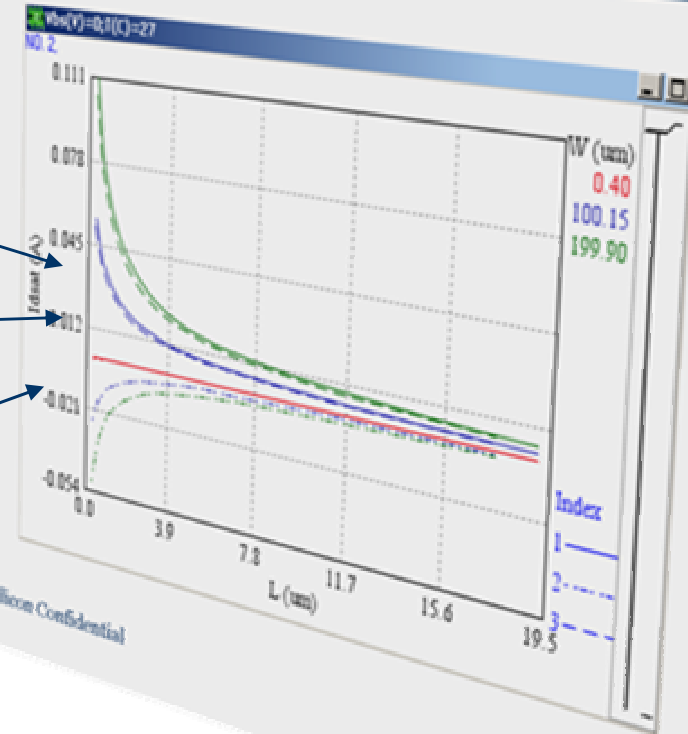
MQA's Result



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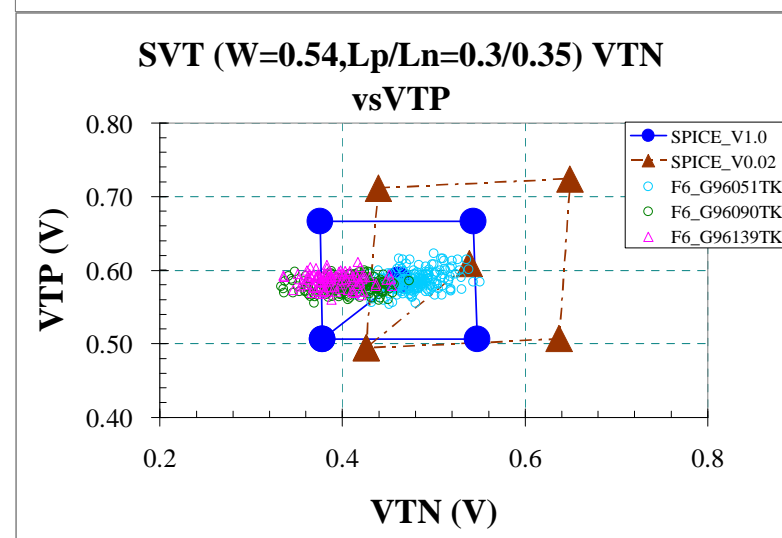
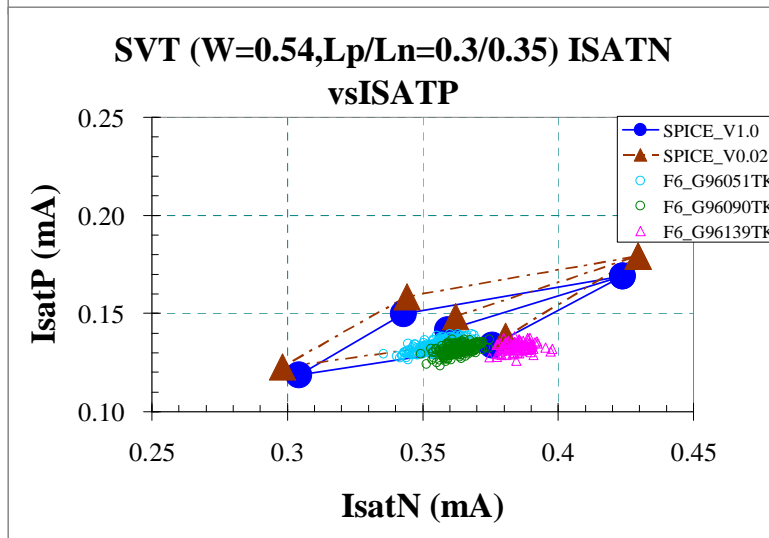
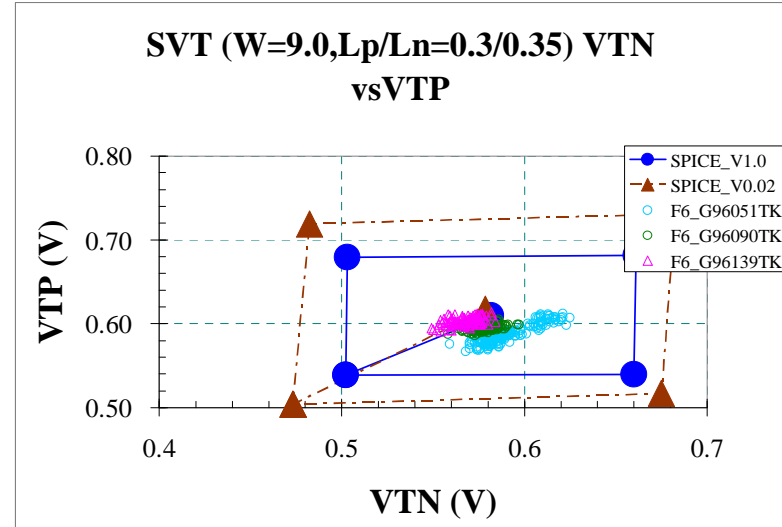
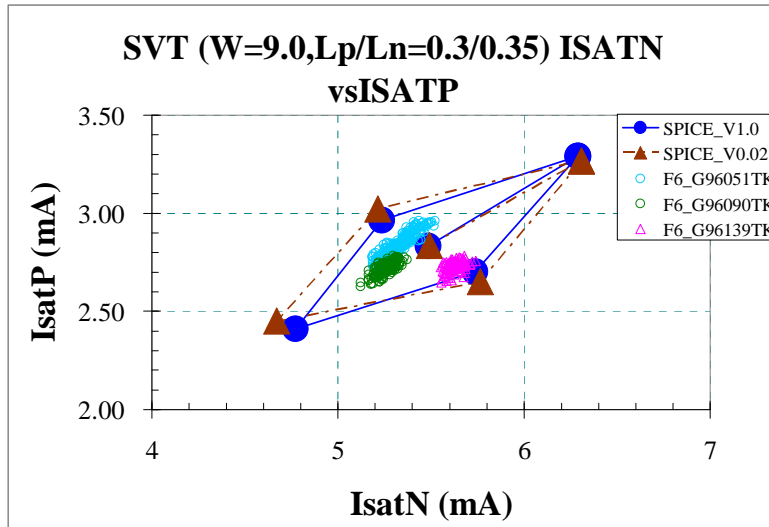
New Graphic



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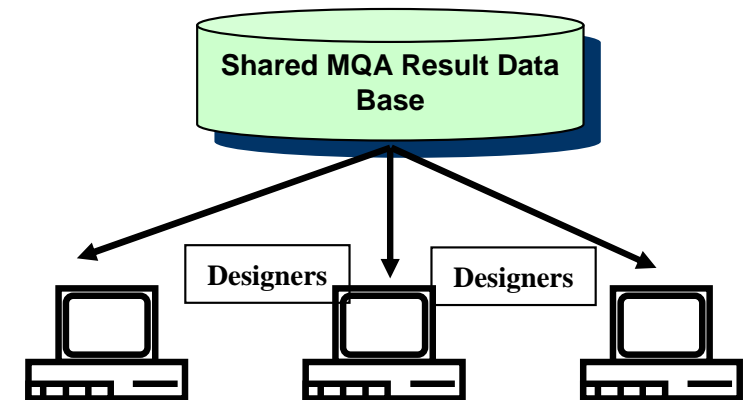
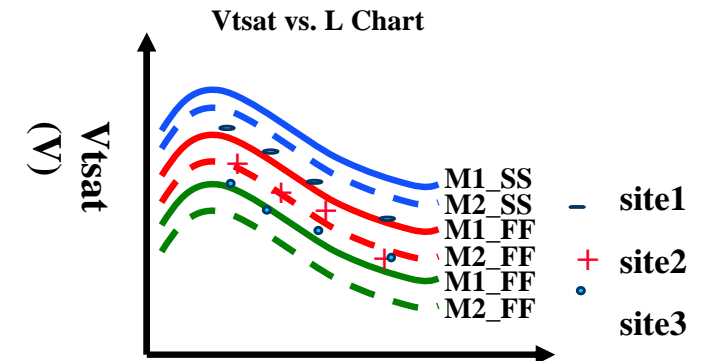


Automatic Report Generation Example



Summary of MQA Features

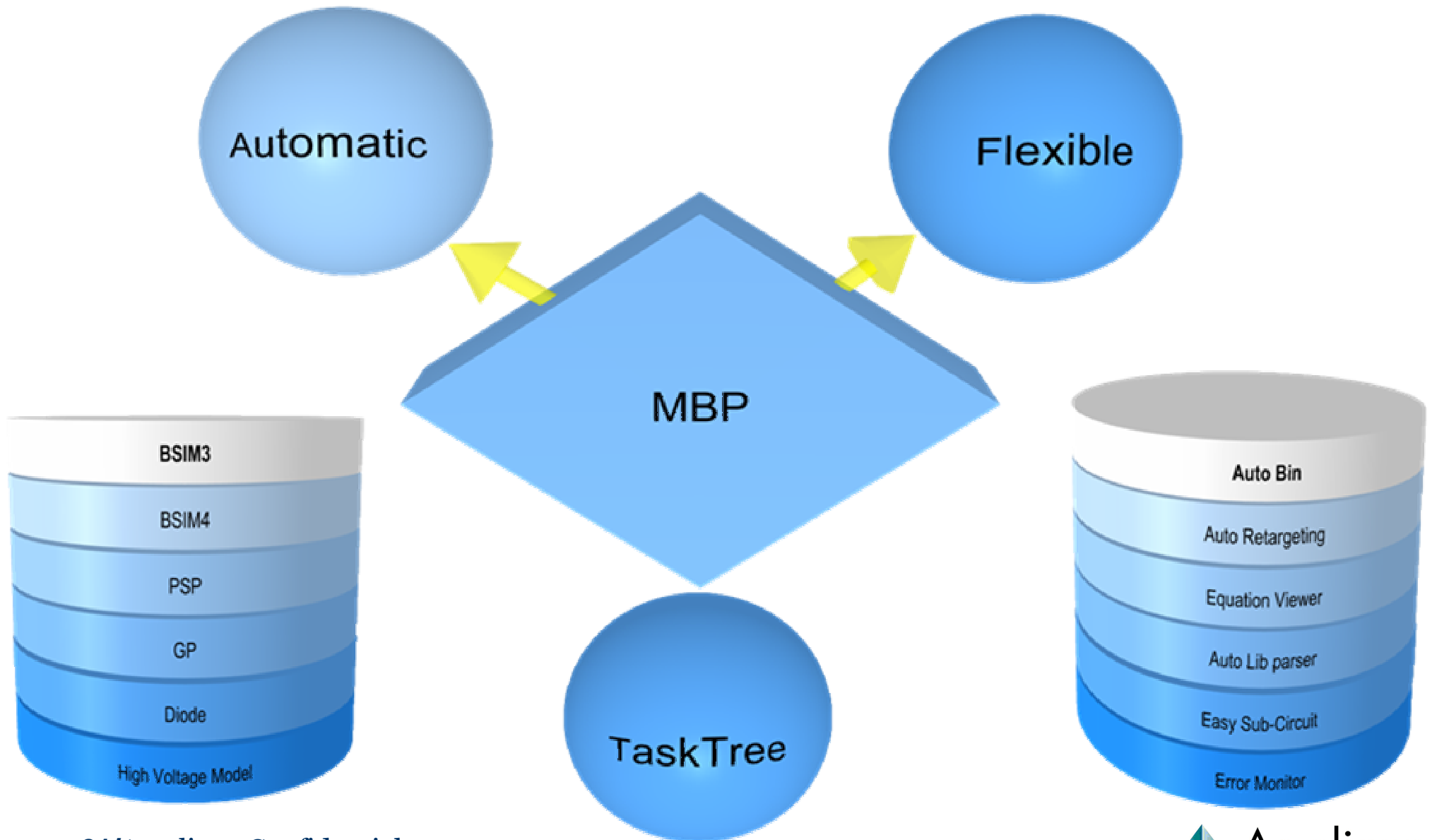
- SPICE model qualification tool
 - Knowledge based rule
 - Can handle huge amount of data
- Design documentation tool
 - Overlay with measurement data
 - Dynamic graphic to zoom/change scale
- Design interface (foundry interface) tool
 - Comparison
 - Sharing the new technology characterization
- Flexible environment
- Model Advisor



MBP's Basic Facts

- SPICE Model Extraction Tool
- Engine: Modified SPICE3f5
 - Support BSIM3v3, BSIM4, GP, PSP, HiSIM, Diode
 - DC, AC (s parameter), Noise
- Optimizer
 - Working with world best known experts in math optimization field
 - State of the art optimizer combines speed, accuracy and robustness
- Development tool: Java

Model Building Program (MBP)



MBP Feature Highlight

➤ User customizable TaskTree

- Allow user to customize and automate extraction/optimization process
- Better task definition and arrangement
- A complete model extraction methods based on optimization methodology
- Automatic extraction of global model, temperature and corner model.

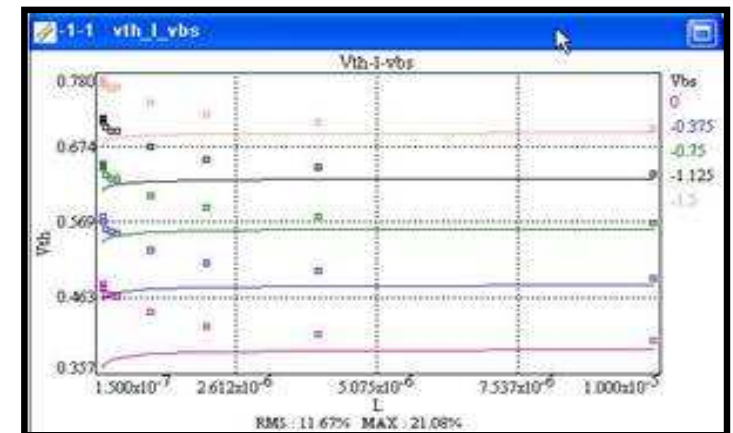
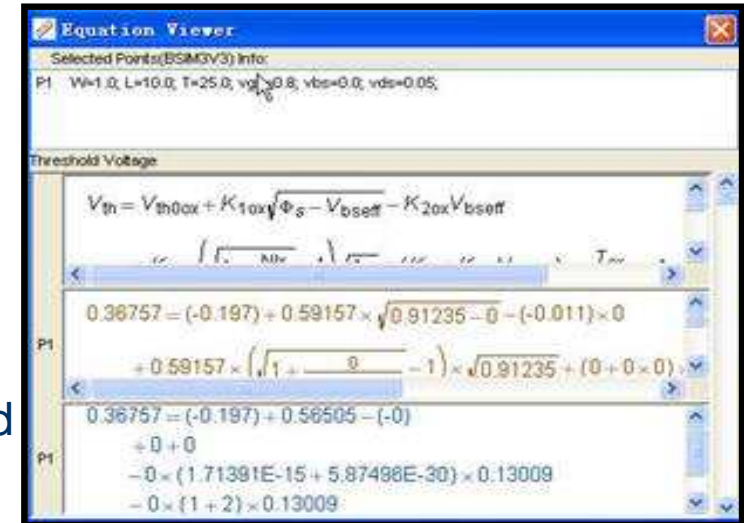
➤ Powerful Equation Viewer

- Enable user to easily view the model equations and the related variable values, it provides a great tool for model issue debugging.
- Model tweaking linked with equation viewer
- Output OP, intermediate variables and equivalent circuits

➤ Optimization on Intermediate Variables

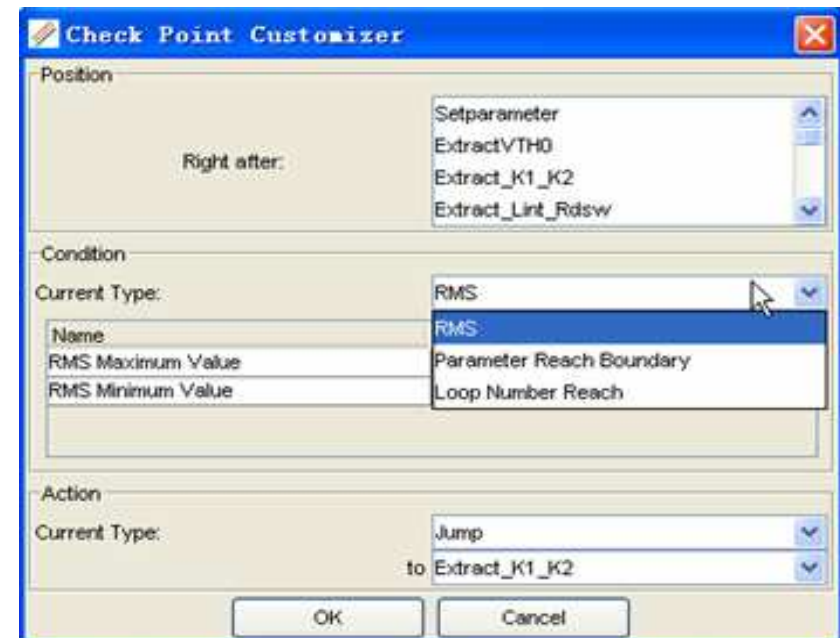
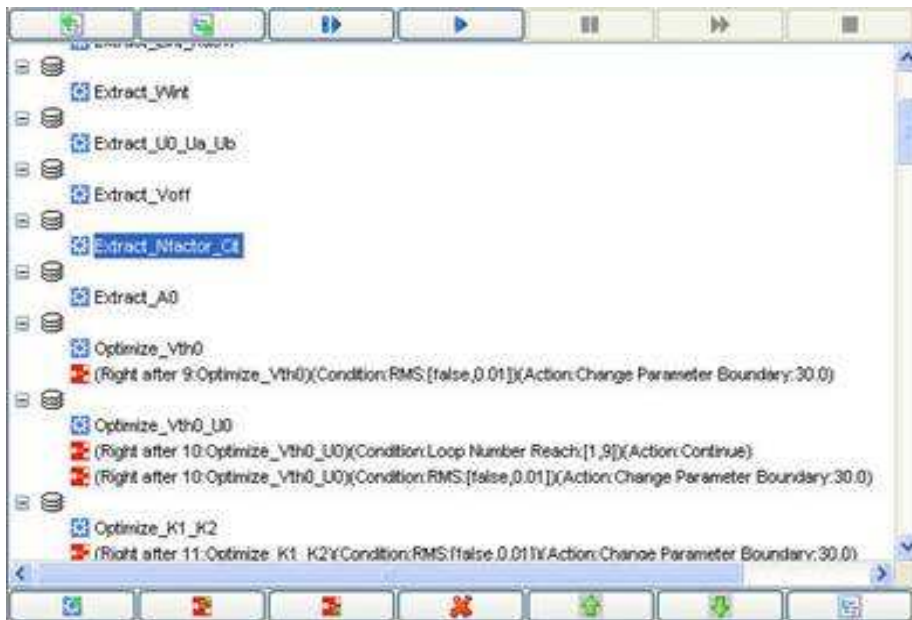
- Provide optimization with more physical meaning

➤ Powerful error monitor to ensure accurate global fitting



State of the Art TaskTree

- Combines flexibility and automation
- Offer different levels of extraction
- User can develop their own modeling methodology



State of the Art TaskTree

- Everything is based on TaskTree



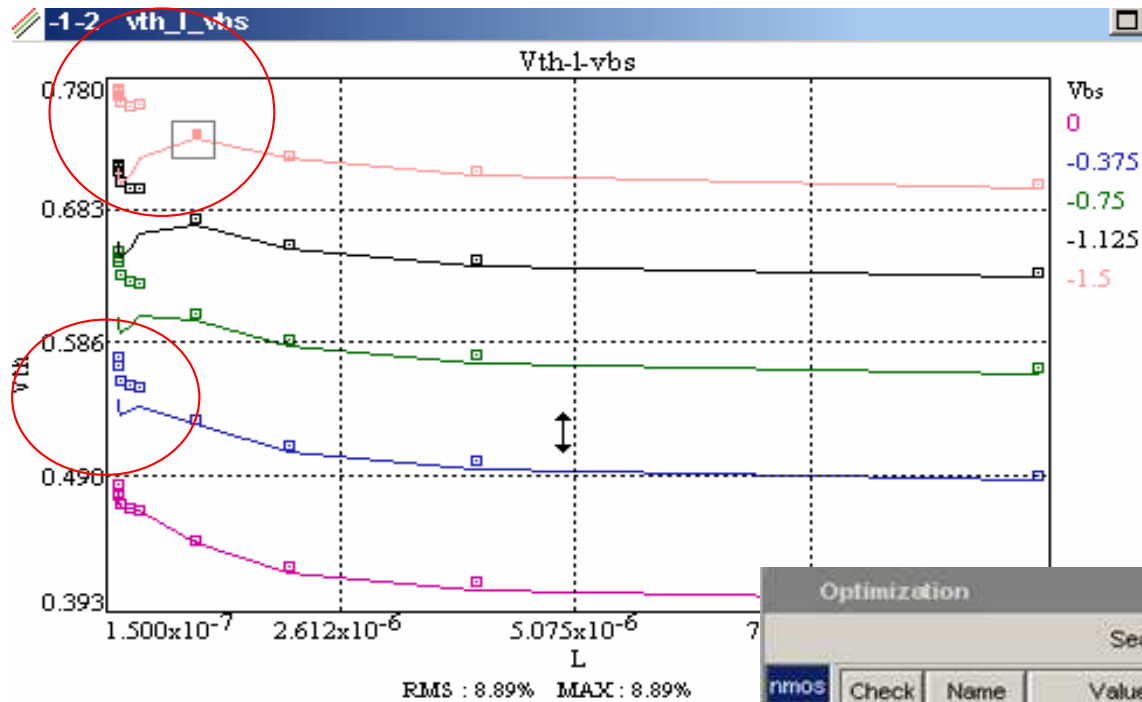
Other Applications

- Taskstree can be also used for running many other modeling applications:
 - Measurement QA, Data screening, Golden Die Selection.
 - Automatic corner model generation.
 - Automatic model re-targeting.
 - Automatic extraction routines for other device models.

MBP's Task Tree

- Benefits to customers
 - Auto extraction/Optimization
 - Productivity increase
 - Easier to get good quality model
 - Open for customer's customization

Model Equation Viewer



Optimization

Search : k1

nmos	Check	Name	Value	Lower	Upper	Step
	<input type="checkbox"/>	keta	0	-0.1	0	1E-4
	<input type="checkbox"/>	tox	1.5E-8	0	1E-6	1.5E-9
	<input type="checkbox"/>	xj	1.5E-7	0	1.5E-5	1.5E-8
	<input type="checkbox"/>	nch	1.7E17	1E16	1E20	1E16
	<input type="checkbox"/>	vth0	0.29625	-2	2	0.01
	<input checked="" type="checkbox"/>	k1	0.46099	0	1	0.01
	<input type="checkbox"/>	k2	0.03098	-0.05	0.03098	1E-4
	<input type="checkbox"/>	k3	80	0.001	100	0.01

ntx: 2.24E-7
 dvt0: 7.06E-1
 dvt1: 5.83E-1
 dvt2: -9.6E-2
 k1: 4.6099E-1

Vth's Equation of BSIM3v3

$$V_{th} = V_{th0ox} + K_{1ox} \sqrt{\Phi_s - V_{bseff}} - K_{2ox} V_{bseff}$$

$$+ K_{1ox} \left(\sqrt{1 + \frac{N_{lx}}{L_{eff}}} - 1 \right) \sqrt{\Phi_s} + (K_3 + K_{3b} V_{bseff}) \frac{T_{ox}}{W'_{eff} + W_0} \Phi_s$$

$$- D_{VT0w} \left(\exp \left(- D_{VT1w} \frac{W'_{eff} + L_{eff}}{2l_{tw}} \right) + 2 \exp \left(- D_{VT1w} \frac{W'_{eff} L_{eff}}{l_{tw}} \right) \right) (V_{bi} - \Phi_s)$$

$$- D_{VT0} \left(\exp \left(- D_{VT1} \frac{L_{eff}}{2l_t} \right) + 2 \exp \left(- D_{VT1} \frac{L_{eff}}{l_t} \right) \right) (V_{bi} - \Phi_s)$$

$V_{th0}=0.295$, $N_{lx}=2.94e-7$, $D_{vt0}=1.106$ $D_{vt1}=0.493$ $D_{vt2}=-0.092$ $K_1=0.47$
 $W=10\mu m$ $L=0.13\mu m$ $T=25C$

How big is L_t ? How big is the D_{vt1} term? Why adjust D_{vt2} , curve does not change?

MBP Shows the Full Equation with Parameter Turner

Selected Points(BSIM3V3) Info:
 P1 W=0.204,L=0.452,T=25,Vbs=0,Vds=0.1,Vgs=1.2,

Threshold voltage

$$V_{th} = V_{th0ox} + K_{1ox}\sqrt{\Phi_s} - V_{bseff} - K_{2ox}V_{bseff}$$

$$+ K_{1ox}\left(\sqrt{1 + \frac{N_{ox}}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + (K_3 + K_{3b}V_{bseff})\frac{T_{ox}}{W_{eff} + W_0}\Phi_s$$

$$- D_{VT0W}\left(\exp\left(-D_{VT1W}\frac{W_{eff}L_{eff}}{2l_{be}}\right) + 2\exp\left(-D_{VT1W}\frac{W_{eff}L_{eff}}{l_{be}}\right)\right)(V_{bi} - \Phi_s)$$

$$- D_{VT0}\left(\exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)(V_{bi} - \Phi_s)$$

$$- \left(\exp\left(-D_{sub}\frac{L_{eff}}{2l_{be}}\right) + 2\exp\left(-D_{sub}\frac{L_{eff}}{l_{be}}\right)\right)(E_{1a0} + E_{1ab}V_{bseff})V_{ds}$$

P1

$$0.415 = (-4.4E-3) + 0.385 \times \sqrt{0.885 - (-6.393E-5) - (-0.027) \times (-6.393E-5)}$$

$$+ 0.385 \times \left(\sqrt{1 + \frac{1.459E-7}{3.724E-7}} - 1\right) \sqrt{0.885} + ((-0.148) + 0.331 \times (-6.393E-5)) \times \frac{4.19E-9}{1.900E-7 \times 0} = 0.865$$

$$- 0 \times \left(\exp\left(-2.807E-8 \times \frac{1.906E-7 \times 3.724E-7}{2 \times 2.896E-8}\right) + 2 \times \exp\left(-2.807E-8 \times \frac{1.906E-7 \times 3.724E-7}{2.896E-8}\right)\right) \times (1.019 - 0.885)$$

$$- 14.548 \times \left(\exp\left(-2.069 \times \frac{3.724E-7}{2.2896E-8}\right) + 2 \times \exp\left(-2.069 \times \frac{3.724E-7}{2.896E-8}\right)\right) \times (1.019 - 0.885)$$

$$- \left(\exp\left(-0.615 \times \frac{3.724E-7}{2.2896E-8}\right) + 2 \times \exp\left(-0.615 \times \frac{3.724E-7}{2.896E-8}\right)\right) \times (0.063 + (-0.046) \times (-6.393E-5)) \times 0.1$$

P1

$$0.415 = (-4.4E-3) + 0.358 - 1.708E-5$$

$$+ 0.084 + (-2.807E-3)$$

$$- 0 \times (0.032 + 2.058E-3) \times 0.154$$

$$- 14.548 \times (1.67E-6 + 5.575E-12) \times 0.154$$

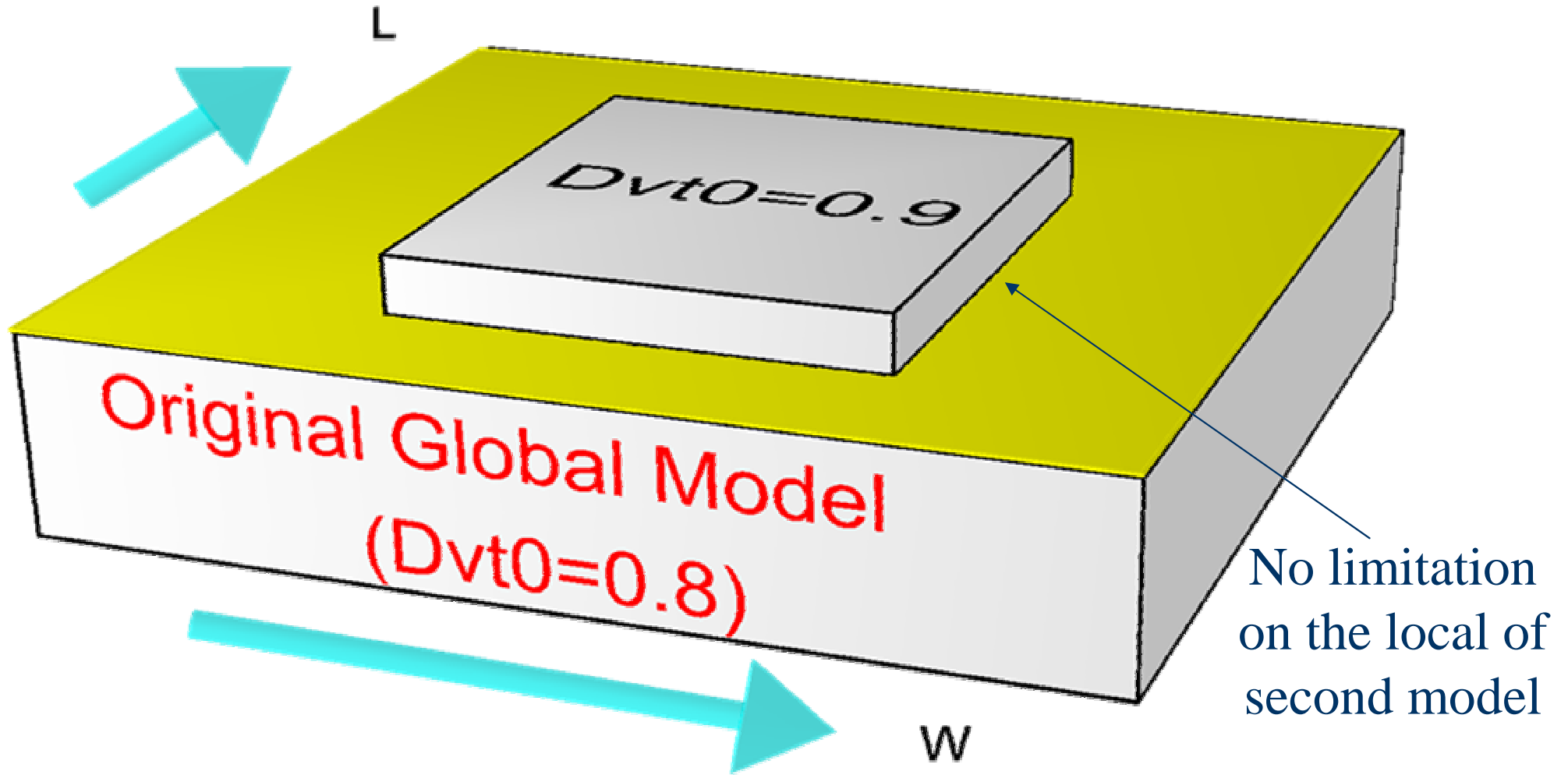
$$- (0.019 + 7.388E-4) \times 6.339E-3$$

Optimization

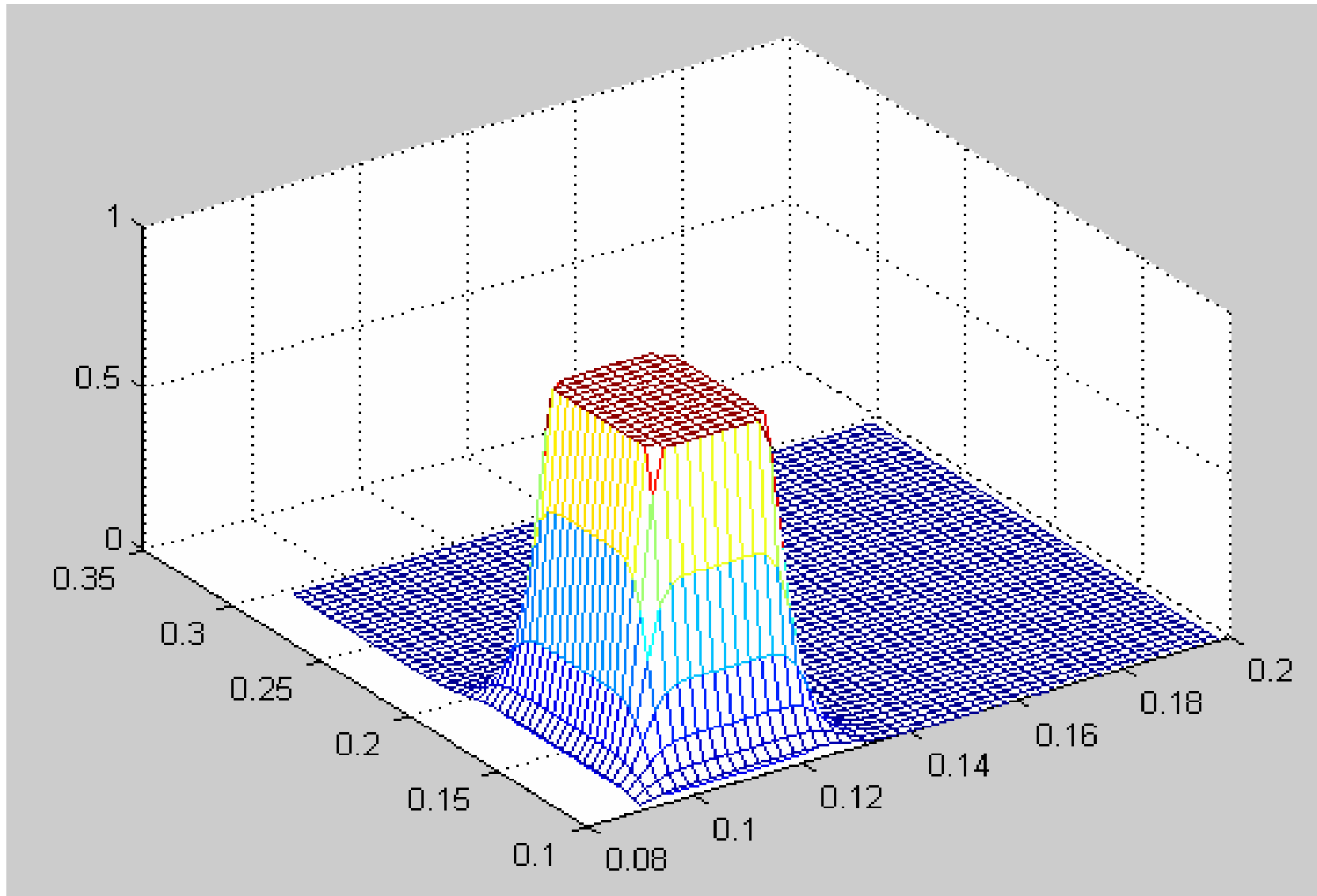
vth0 3.5383E-1 u0 3.8025E-2 dvt0 1.4548E1 dvt1 2.0691E0

Adjust Parameter,
and see the real time change of equation

Hybrid Global Model

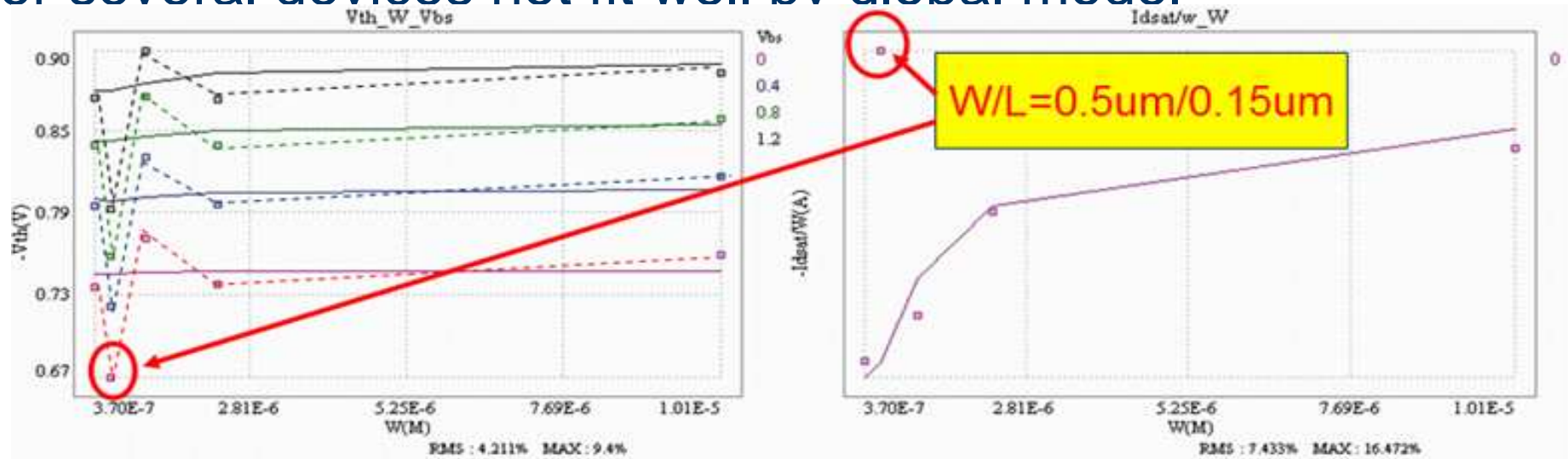


Smooth Boundary

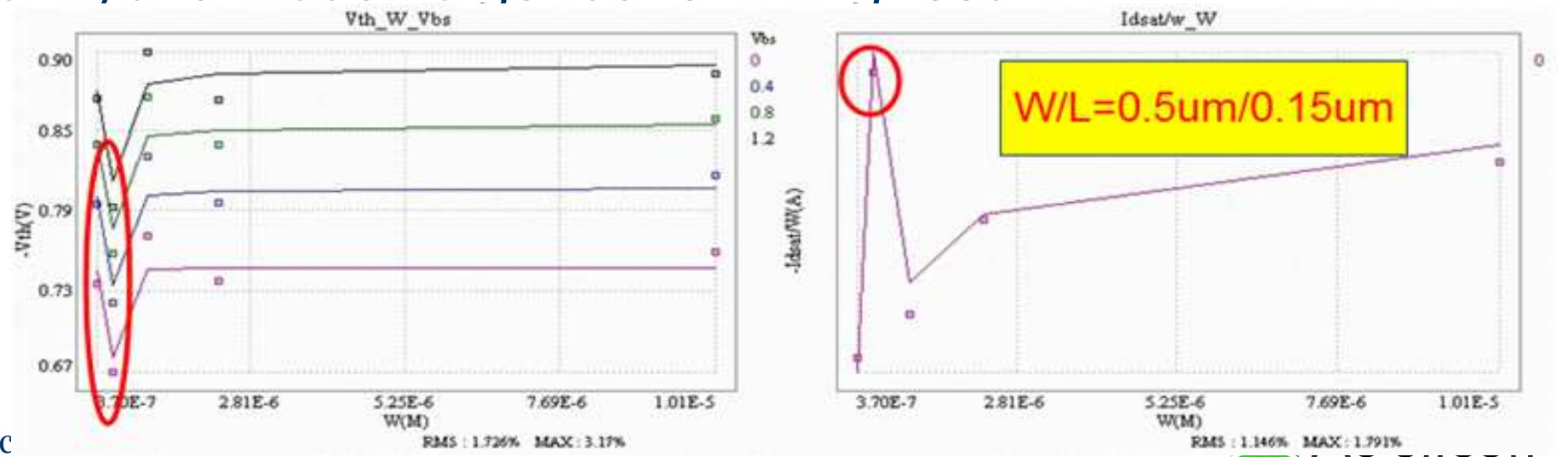


Compare of Hybrid and global model

- One or several devices not fit well by global model



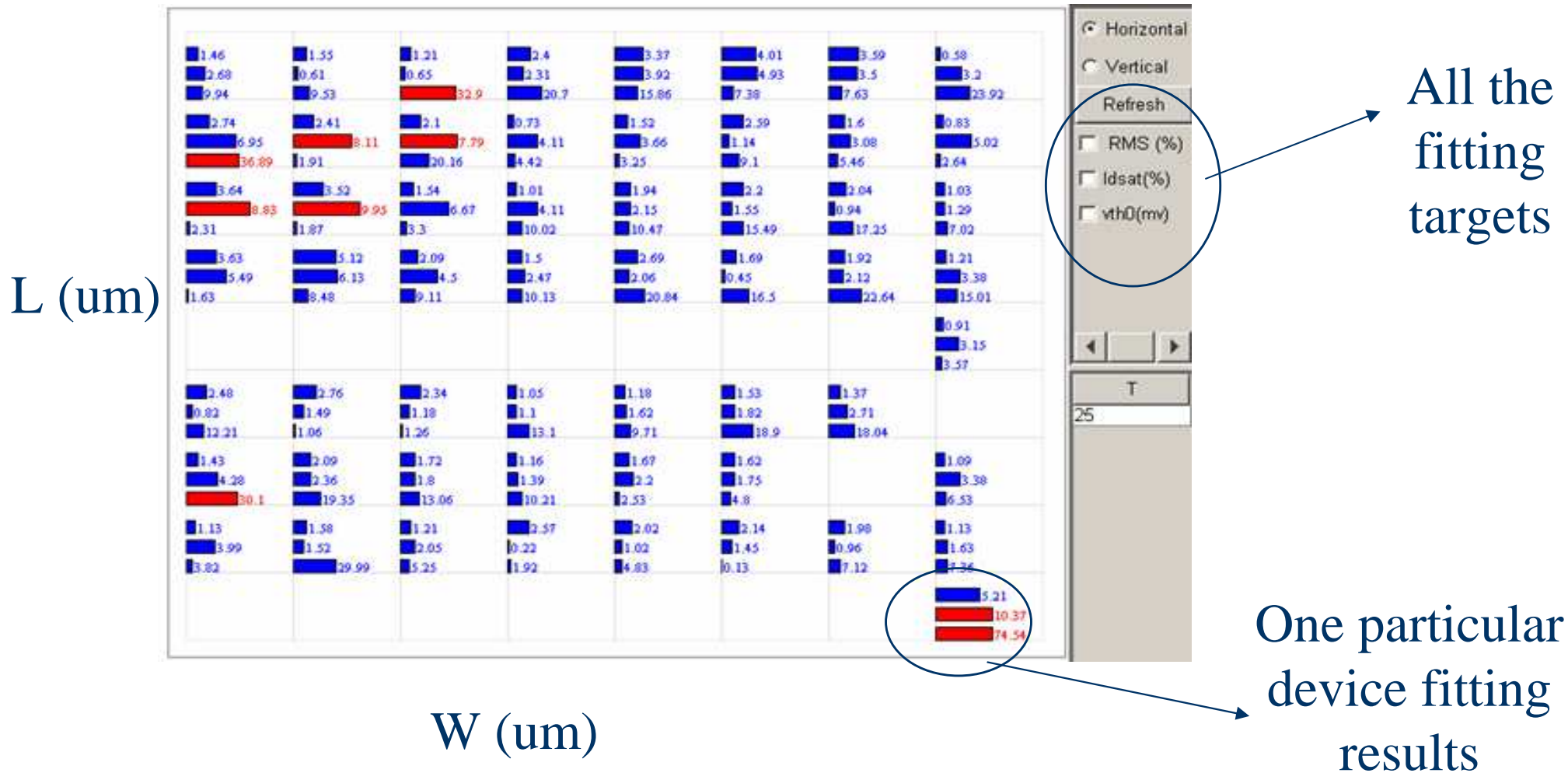
- Use of hybrid model to get better fitting result



Compare the three formats of model

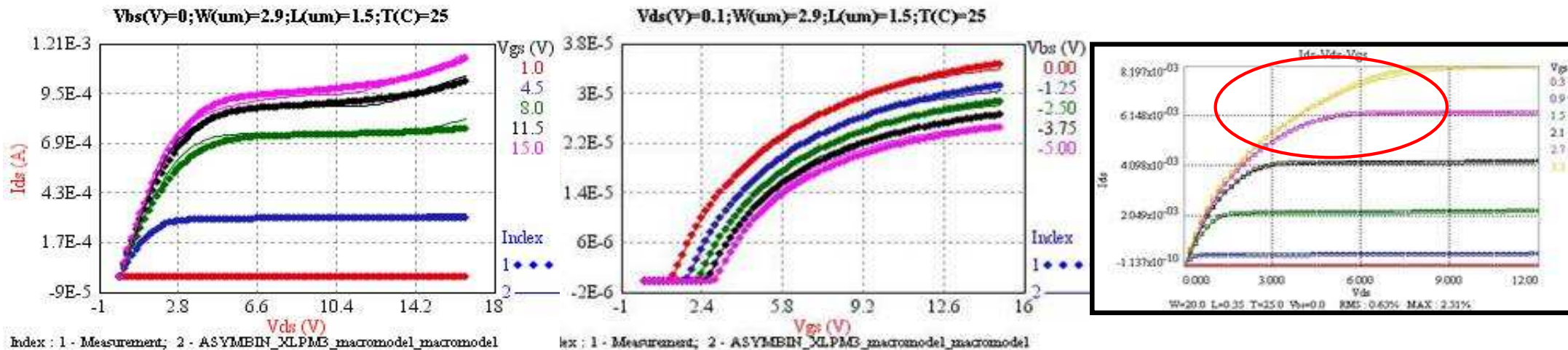
	Global Model	Binning Model	Hybrid-Model
Model format	All parameters are same for different special caution)	Region model, each region's O/I/w/p parameters are calculated from point models	Global model with some selected parameters become function of device size in a user defined region (w/l's region)
Advantage	Physical meaning, easy to maintain, easy to generate corner model	Accuracy is better, if the bin region is small	Combine the advantage of both binning model and global model
Disadvantage	May have problems to fitting some device's behavior	Extraction is tedious, time consuming, and special caution must be taken when generate the point model. Difficult to maintain. Difficult to generate corner model	Remove the limitation of global model
Continuity	Characterization vs L(or W) is continual	Characterization vs L (or W) is first-order continual cross the bin boundary, the trend may not right inside bin boundary if extraction is not carefully done	Same as global model
Extraction tool	Public domain methodology, supported by all modeling tool	Public domain methodology, supported by all modeling tool	Accelicon's patent-pending methodology, available only in MBP

Check All the Modeling Criteria



Easy Sub-circuit Modeling - HV

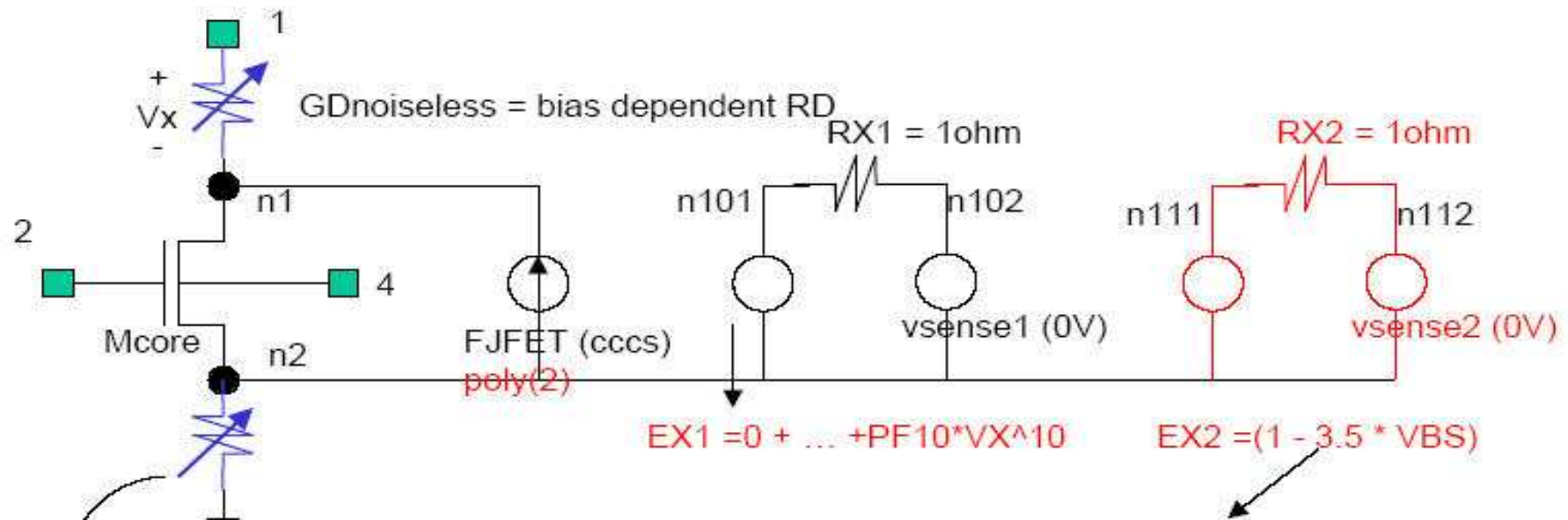
- Accelicon uses macro model approach that accurately models:
 - Quasi-saturation effect
 - V_{bs} dependency of R_d and R_s
 - Severe impact ionization
- Our methodology is very flexible and can model many unexpected effects (such as the one highlighted below)
 - Sufficient to address all kinds of parasitic elements



Sample Schematic

- A common circuit used for HV modeling is shown below, impact ionization is not modeled with this circuit.

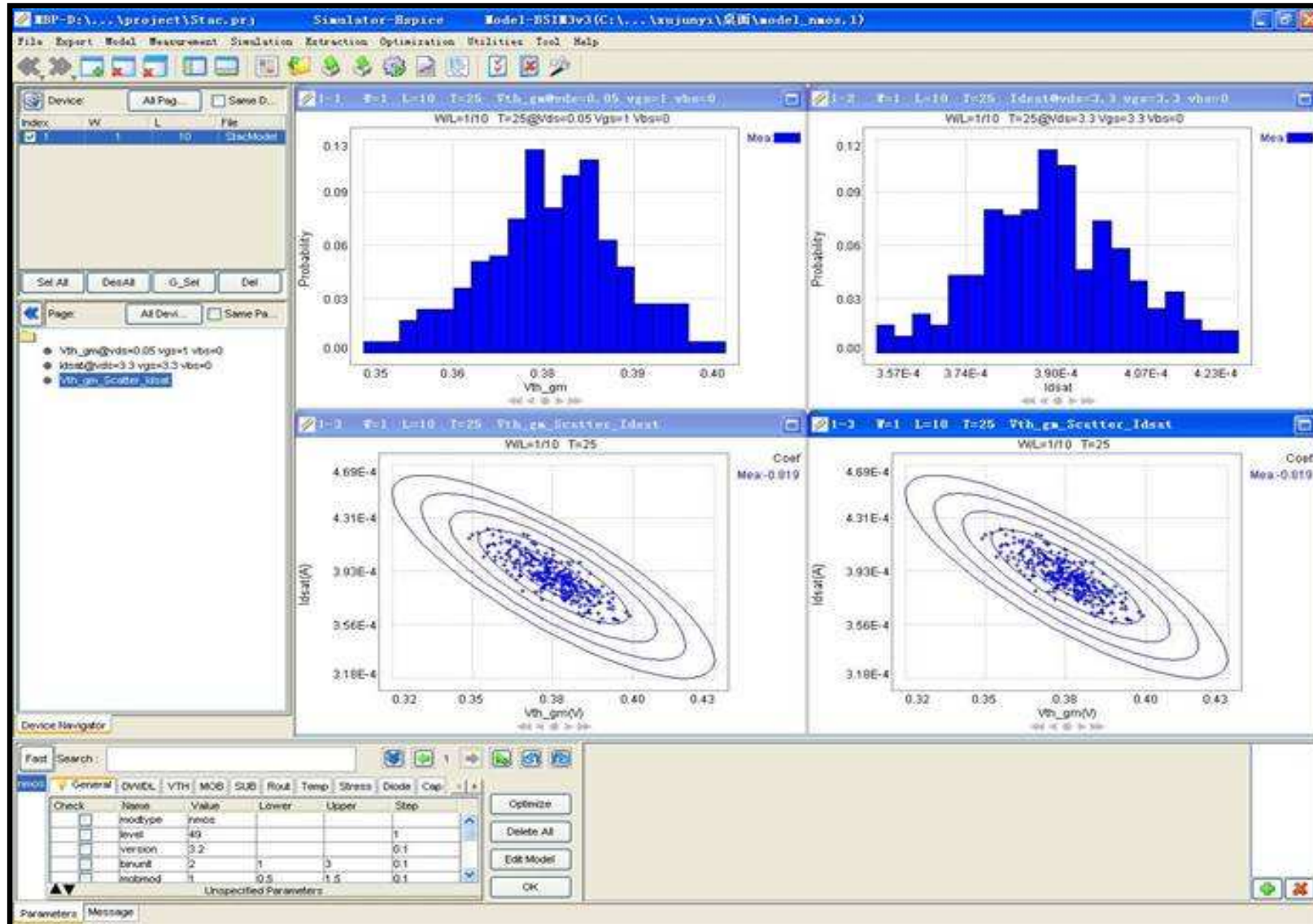
New Circuit Schematic



Easy Sub-circuit Modeling – Layout effect

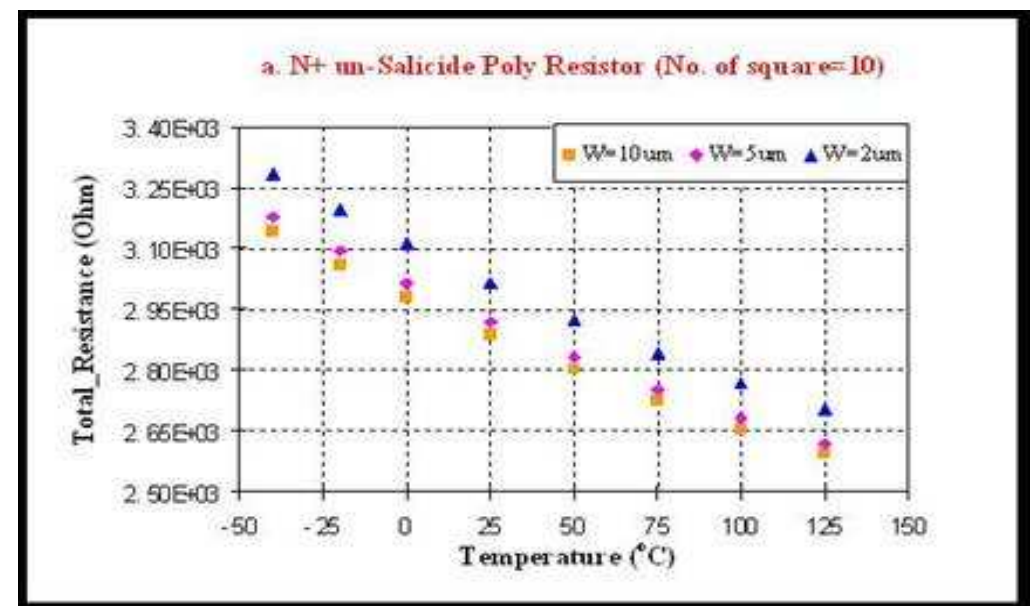
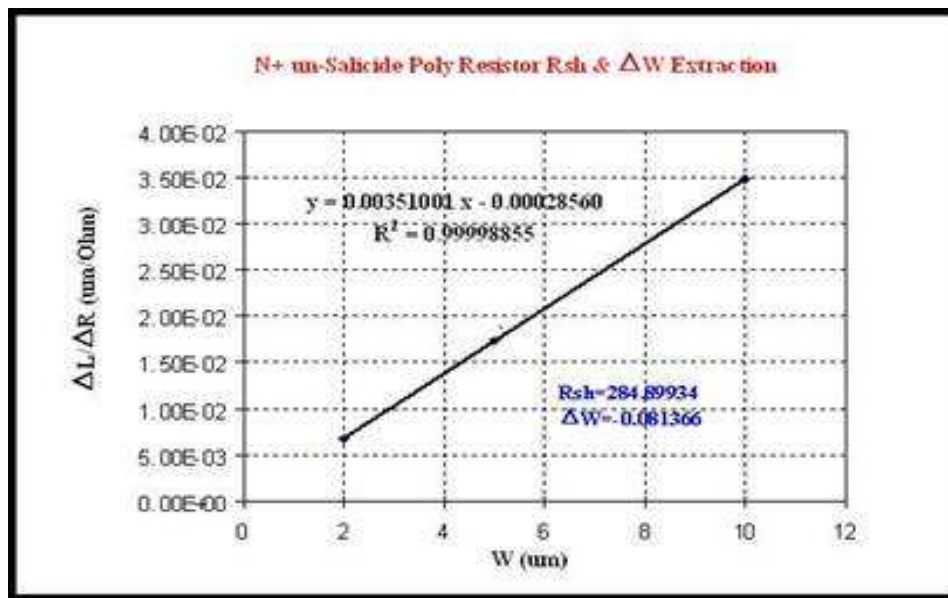
- MBP allows user to define and optimize on new measurements
 - Device performance vs. layout parameters, such as I_{dsat} vs. SCA
- User can define equations in sub-circuit model format to address layout effects and utilize MBP to easily adjust these parameters.

Statistical, Mismatch Functions



Auto Resistor Model Extraction

- Automatically process resistor data and model simulation.
- Plot resistor performance.
- Automatically extract model parameters.

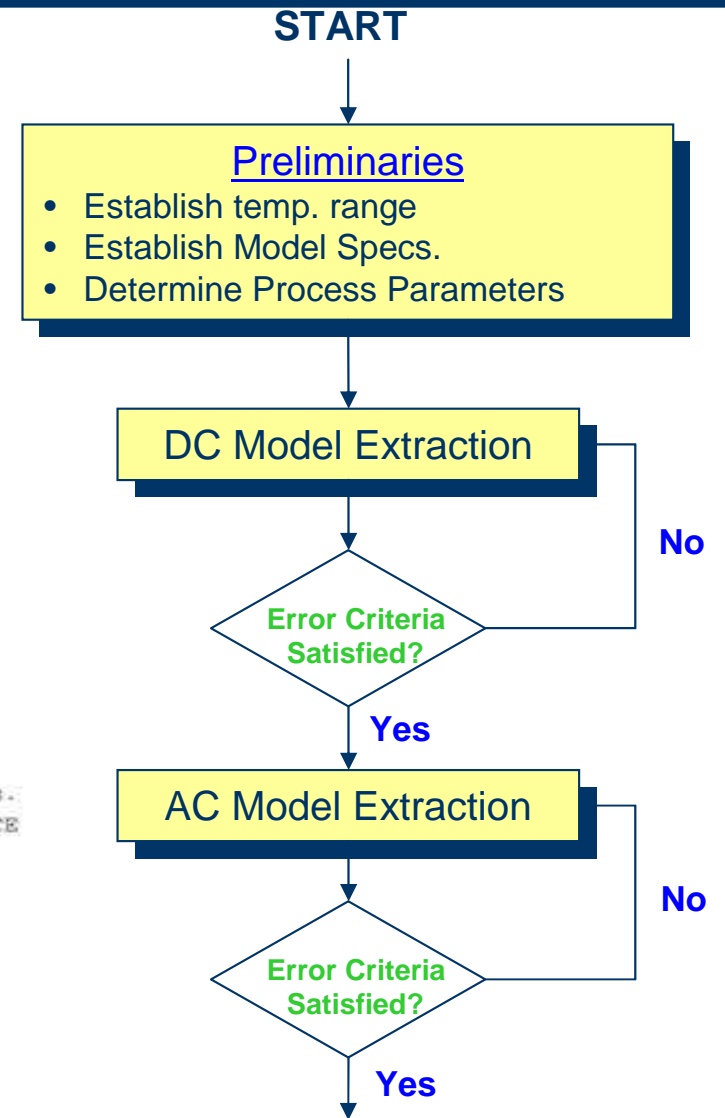
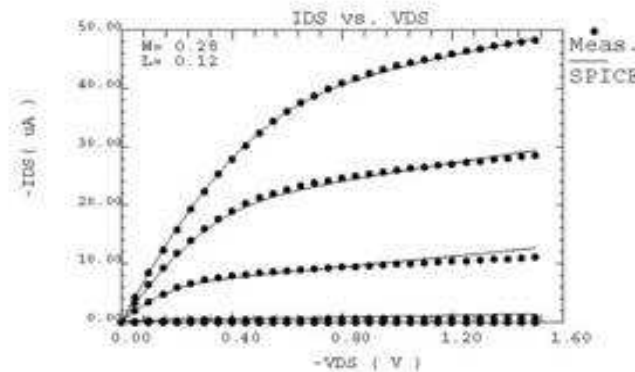


Accelicon's Modeling services

- The modeling experts have years of modeling experiences with various technologies
- Currently several world-leading foundries are using Accelicon's modeling services
- We can provide service on both front end and back end modeling
- Accelicon's SPICE modeling services include
 - BSIM3/4/PSP model extraction services (temperature model with corners)
 - Bipolar models
 - RF modeling
 - HV and FG devices sub circuit modeling
 - Interconnect modeling
 - Physical verification deck generation including DRC, LVS and RCX.

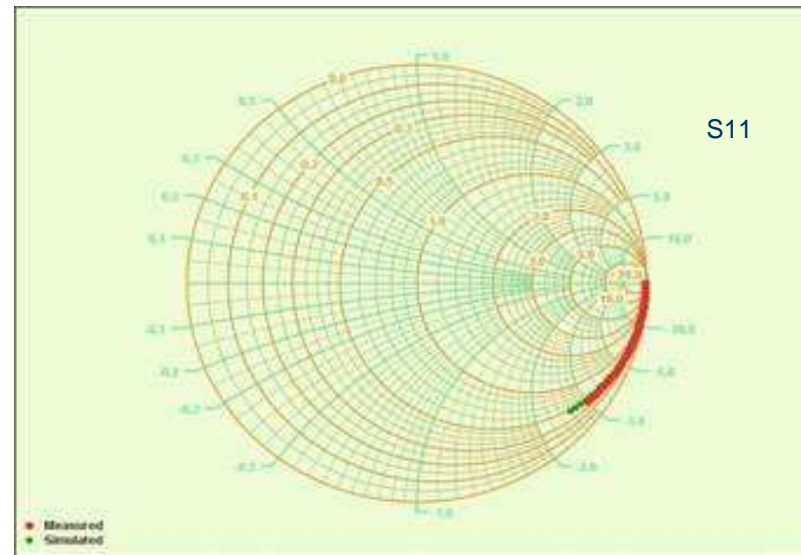
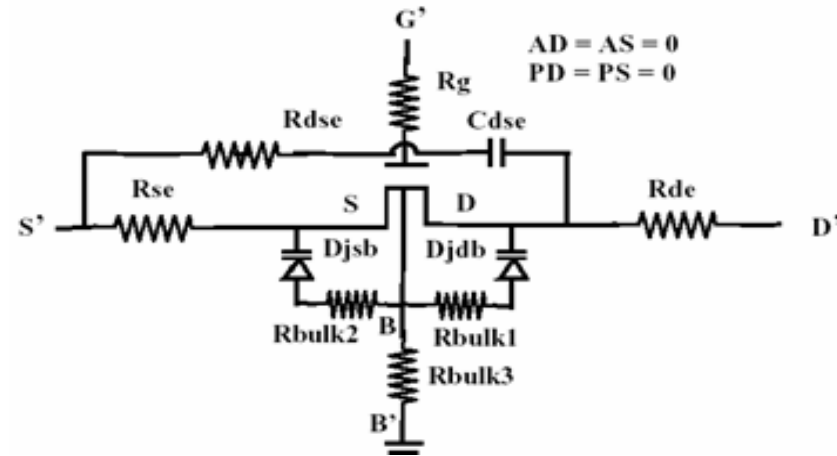
MOS SPICE Modeling

- Supported Compact Model
 - BSIM3v3.2
 - BSIM4
 - PSP : in development
 - Supported Simulators
 - HSPICE
 - Spectre
- Chose of Global or Binning According to
 - Applications
 - Client Preference
- High Quality Model with Rigorous QA Procedure
 - DC
 - AC
 - Temperature
 - Corner models
 - Best case (Fast)
 - Worst case (Slow)



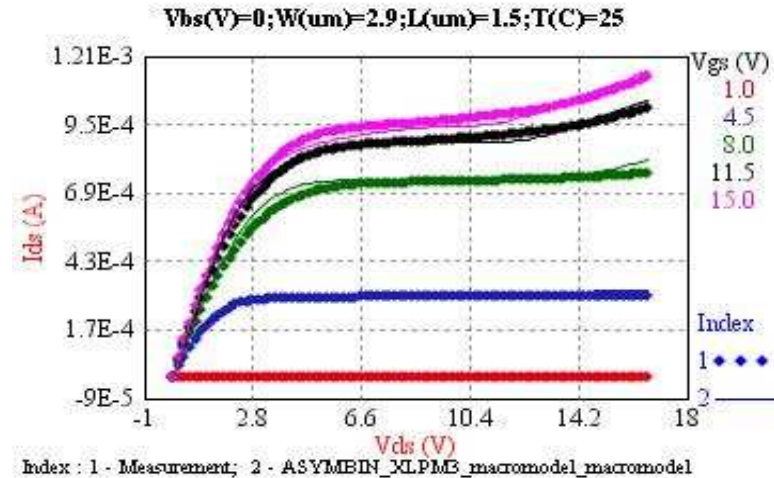
RF SPICE Modeling

- Device Type
 - MOS
 - On-chip inductors
 - MIM-Caps
 - Varactors
- Lumped Circuit Model
 - Scalable
 - Valid up to 6Ghz
- Rigorous QA Procedure
 - Ensure model quality



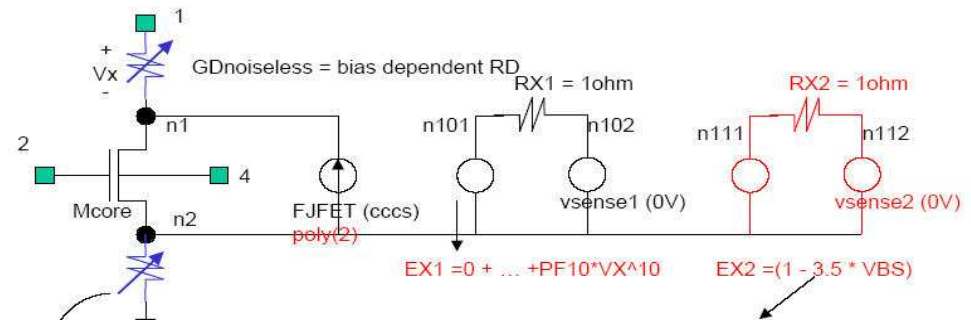
Macro Modeling

- Device Type
 - HV devices, typically LDMOS
- Macro Circuit Model
 - BSIM3V3 core model
 - Optimized the macro circuit elements to obtain the best fit



- Rigorous QA Procedure
 - Ensure model quality

New Circuit Schematic



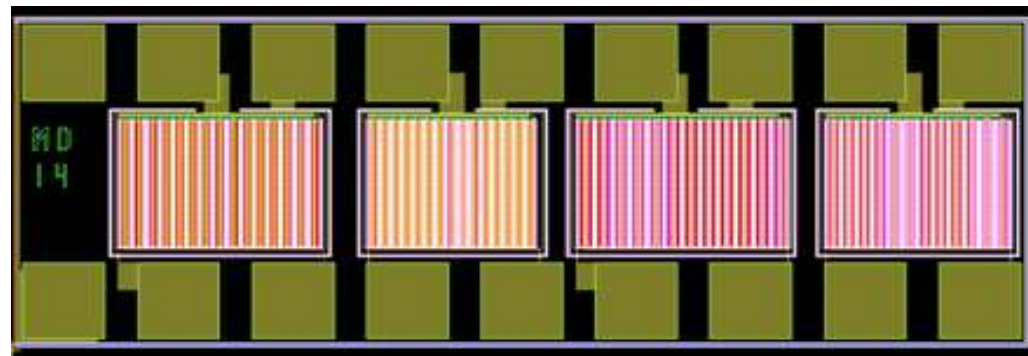
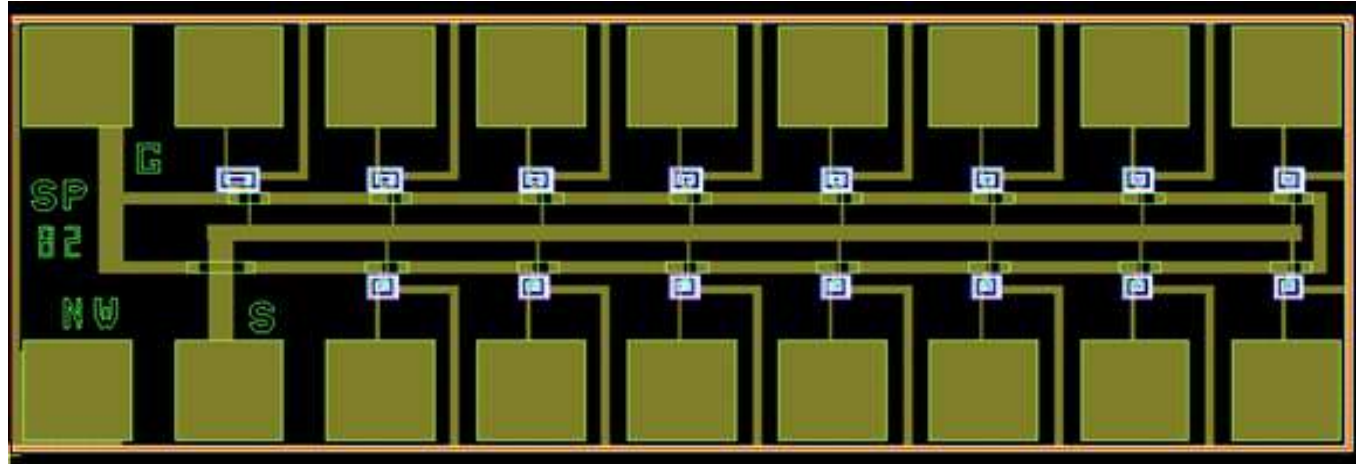
TEG Design

➤ Digital Block

- SPICE
- Interconnect

➤ Analog & RF

- Mismatch
- BJT
- RF structures
- Substrate coupling
- ESD



Interconnect Modeling

- Accelicon has industry's first complete interconnect parasitic extraction solution
- This methodology has been exercised many times with excellent success
- Accelicon expertise covers structures design, characterization, interconnect modeling and layout parasitic extraction
- In Accelicon, interconnect modeling is referred as RCX

Summary

- Accelicon has the best SPICE modeling tools
 - MQA: validation, documentation, comparison, sharing
 - MBP: equation viewer, Hybrid-model, HV solution
- Accelicon's tools have been used by worldwide foundry, IDM, design companies