

1/f Noise Corner Modeling

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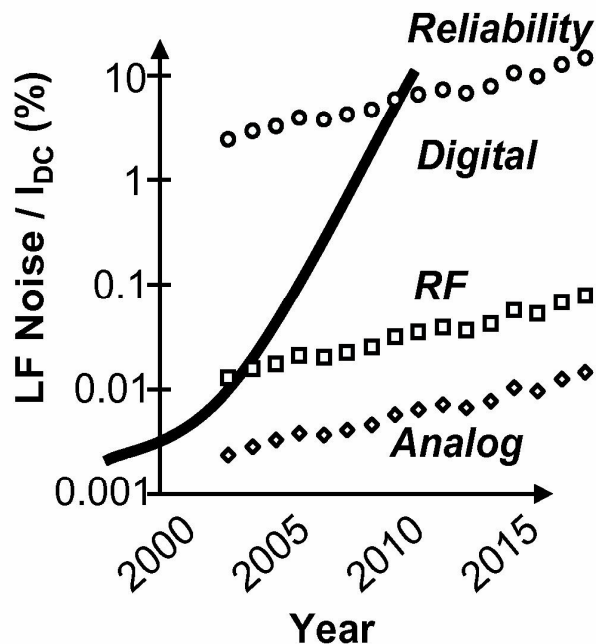
Agenda

- “Appetizer” – Why to model LF noise?
- LF noise critical design areas
- Some basic theory
- Methodology for corner generation & implementation
- Design example
- Status quo – software, models, equipment ...
- Summary

“Appetizer” – Why to model LF noise?

Future technologies

--> increased noise mainly due to new process generations and additional defects!



- **Digital:** $W \times L = 3 \times 1 L_{\min}^2$, p-p Noise
 $f_{\max}/f_{\min} = 1/\text{error rate} = 10^{12}$, $t \times \sigma = 12\text{dB}$
- **RF:** $W \times L = 1000 \times 1 L_{\min}^2$, RMS Noise
 $f_{\max}/f_{\min} = 1\text{MHz}/1\text{Hz}$, $t \times \sigma = 10\text{dB}$
- ◇ **Analog:** $W \times L = 500 \times 20 L_{\min}^2$, RMS Noise
 $f_{\max}/f_{\min} = 100\text{kHz}/1\text{Hz}$, $t \times \sigma = 6\text{dB}$

[Rev. ICNF2005 - “Noise in Advanced Electronic Devices and Circuits”, J. Deen et al.]

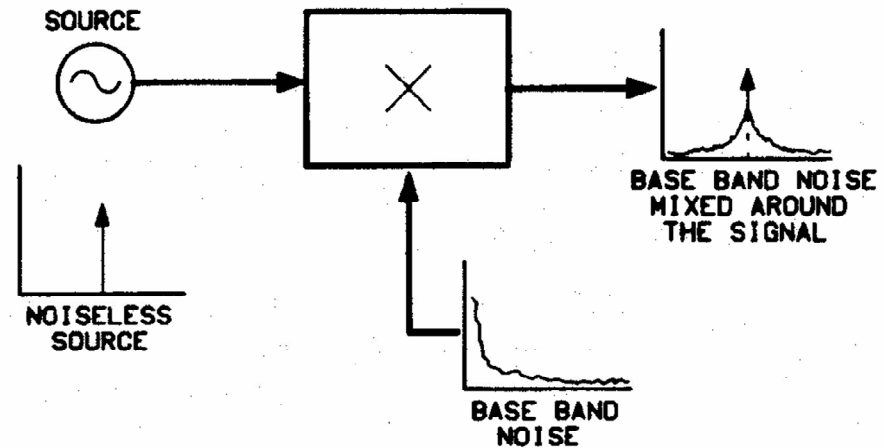
LF Noise Critical Design Areas I

- Audio (0-20kHz)
- RF Systems (phase noise, ...)
- Low Power (medical applications like pacemaker, ... or watches)
- High precision analog circuits for sensors, ≥ 24 bit AD/DA converters

In principle: Noise is the main limitation for high resolution analog design and all RF systems are affected by noise (!)

LF Noise Critical Design Areas II

RF System - phase noise:

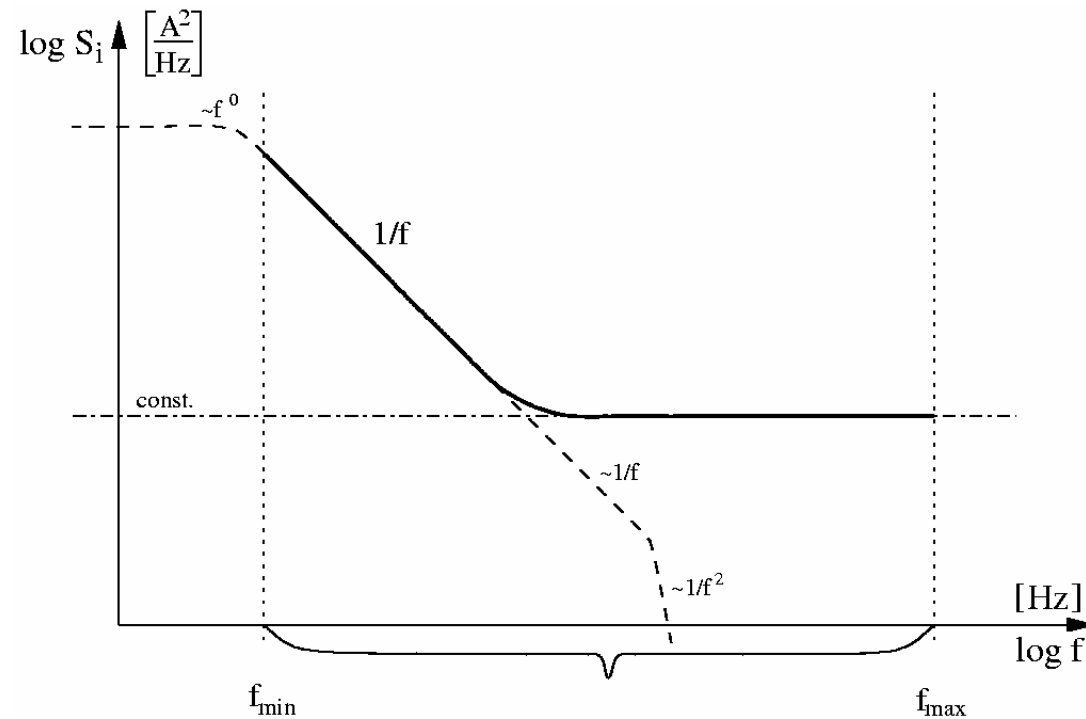


- *Q-factor of the resonator and varactor (tradeoff to bandwidth)*
- *1/f noise of active device (transistor)*
- *DC bias and external tuning voltage noise*

Some Basic Theory I

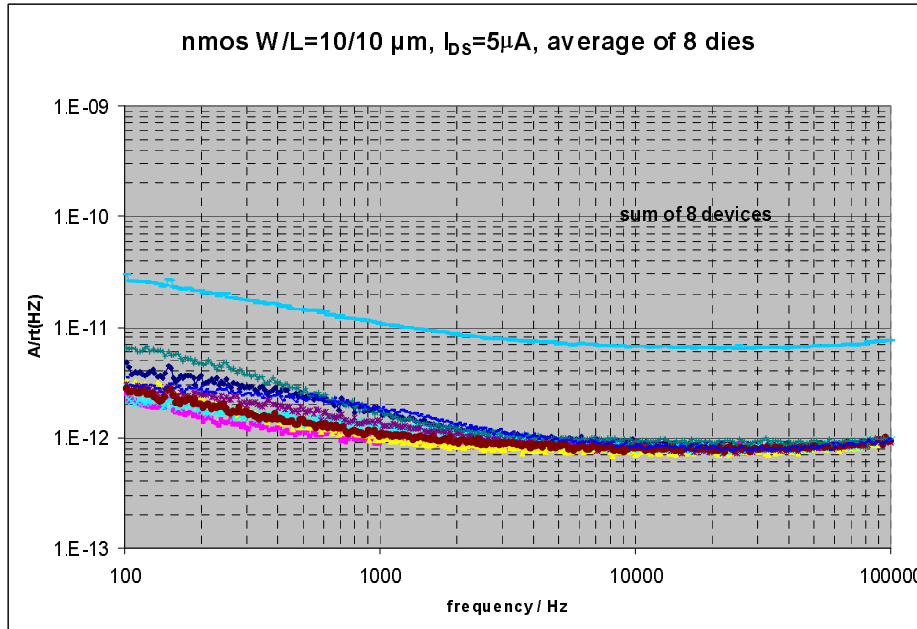
Typical LF drain-current noise of a MOS

device:



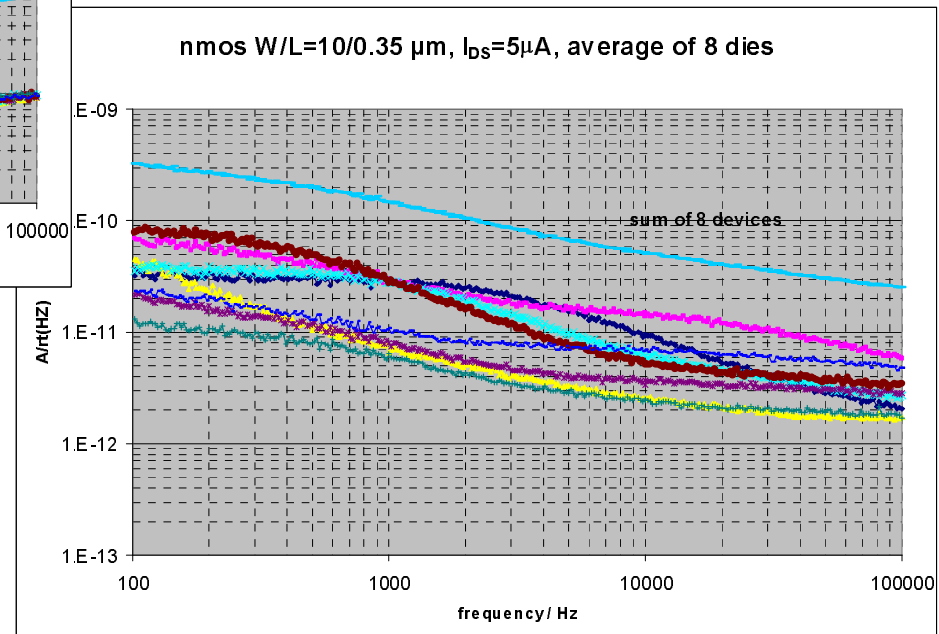
Some Basic Theory II

Typical LF draincurrent noise of a real MOS device:



In case for robust design it is sufficient to know the maximum noise level!

In case for LF noise design optimization it is necessary to know the spread also!



Some Basic Theory III

MOS SPICE Formulas:

$$S_{in} = \frac{1}{C_{OX} \cdot L^2} \frac{KF \cdot I_{DS}^{AF}}{f^{EF}} + \frac{8}{3} \cdot k \cdot T (gm + gmb + gds)$$

$$S_{in} = \frac{1}{C_{OX} \cdot W \cdot L} \frac{KF \cdot I_{DS}^{AF}}{f^{EF}} + \frac{8}{3} \cdot k \cdot T (gm + gmb + gds)$$

Some Basic Theory III

BSIM3V3 Formulas (valid for both NMOS and PMOS):

(derived from oxide-trap induced carrier and surface mobility fluctuation mechanism)

$$V_{gs} \geq V_{th} + 0.1 \quad S_i(f) = \frac{q^2 \cdot V_t \cdot \mu_{eff} \cdot I_{ds}}{1 \times 10^{18} \cdot C_{ox} \cdot L_{eff}^2 \cdot f} \cdot \left[NOIA \cdot \log \left(\frac{N_0 + NSTAR}{N_l + NSTAR} \right) + NOIB \cdot (N_0 - N_l) + NOIC \cdot \frac{N_0^2 - N_l^2}{2} \right] +$$

$$\frac{V_t \cdot \Delta L_{clm} \cdot I_{ds}^2}{W_{eff} \cdot L_{eff}^2 \cdot f} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N + NSTAR)^2}$$

$$N_0 = \frac{C_{ox}}{q} \cdot (V_{gs} - V_{th})$$

$$N_l = \frac{C_{ox}}{q} \cdot (V_{gs} - V_{th} - \text{Min}(V_{ds}, V_{dsat}))$$

$$V_{gs} < V_{th} + 0.1 \quad S_{limit}(f) = S_i(V_{gs} = V_{th} + 0.1) \quad S_{wi}(f) = \frac{NOIA \cdot V_t \cdot I_{ds}^2}{1 \times 10^8 \cdot W_{eff} \cdot L_{eff} \cdot f \cdot (NSTAR)^2}$$

$$S_i = \frac{\bar{i}_{n,f}^2}{\Delta f} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}}$$

flicker term + thermal noise term = LF noise characterisation

[<http://www-device.eecs.berkeley.edu/~bsim3/latenews.html>]

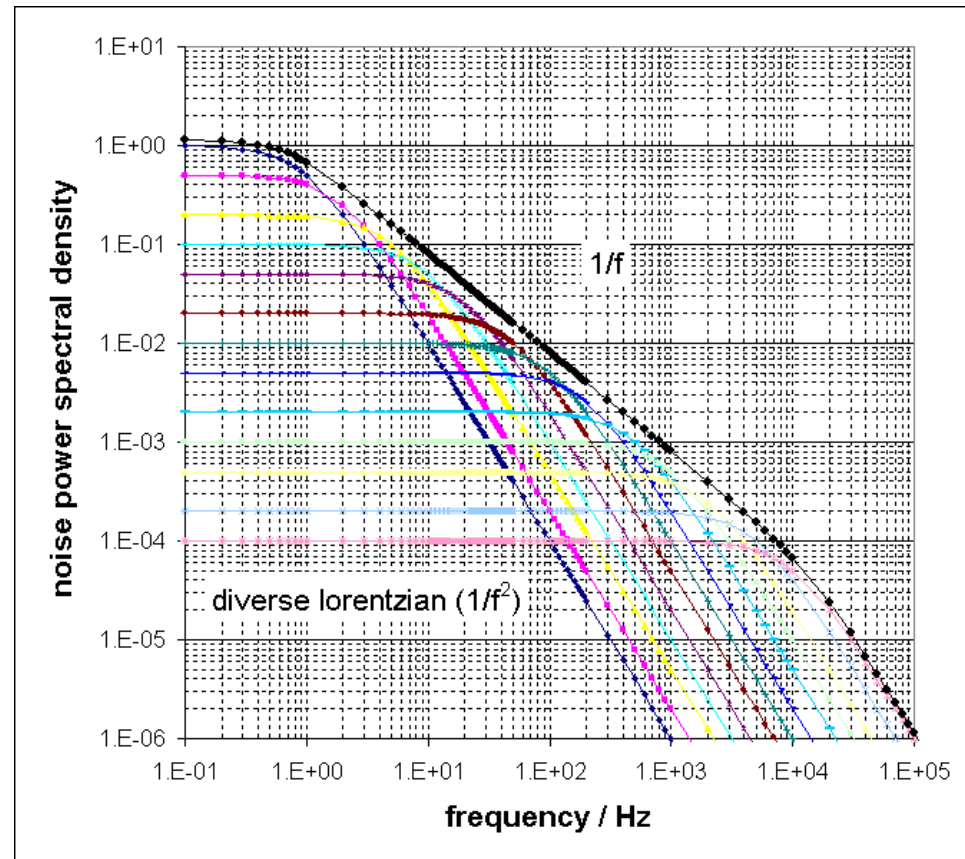
Some Basic Theory IV

LF noise as a sum of Lorentzians:

$$S_N(f) \approx \frac{\tau}{1 + \tau^2 f^2}$$

$$S_N(f) \approx \sqrt{\sum_{\tau=\tau_0}^{\tau_1} \left(\frac{\tau}{1 + \tau^2 f^2} \right)^2} \approx \frac{1}{f}$$

A large enough sample of devices will exhibit on the average 1/f behaviour in case of equally distributed Lorentzians!



Methodology For Corner Generation & Implementation

- 1.) Measurement of several geometries @ different bias settings per wafer per lot
- 2.) Calculation of the average and 3 sigma deviation for each geometry/bias
 → typical mean data base (tm) and worst case data base (wc)
- 3.) Parameter extraction for tm and wc
- 4.) Simulator implementation → → → →
- 5.) check: simulation versus measurement

MOS model data set	Noise data set
<i>typical mean</i>	<i>WC noise</i>
<i>WC power</i>	<i>WC noise</i>
<i>WC speed</i>	<i>WC noise</i>
<i>WC one</i>	<i>WC noise</i>
<i>WC zero</i>	<i>WC noise</i>
<i>typical mean</i>	<i>typical mean</i>

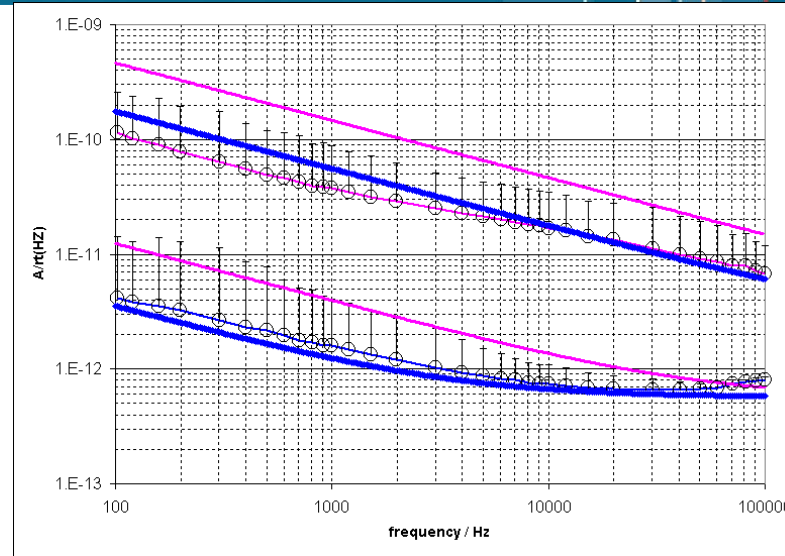
Methodology for Corner Generation & Implementation

Simulation versus Measurement

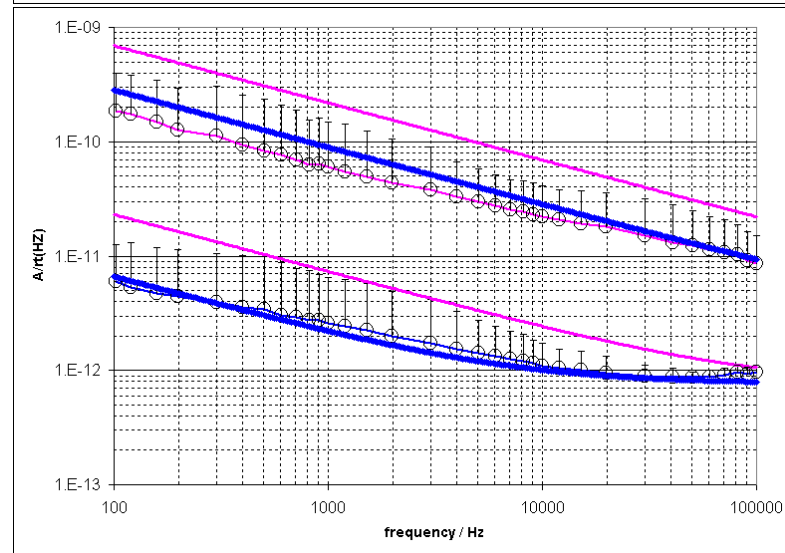
NMOS W/L=10/1.2

VDS=2V

IDS=1 and 100µA



IDS=2 and 200µA



Design - Example

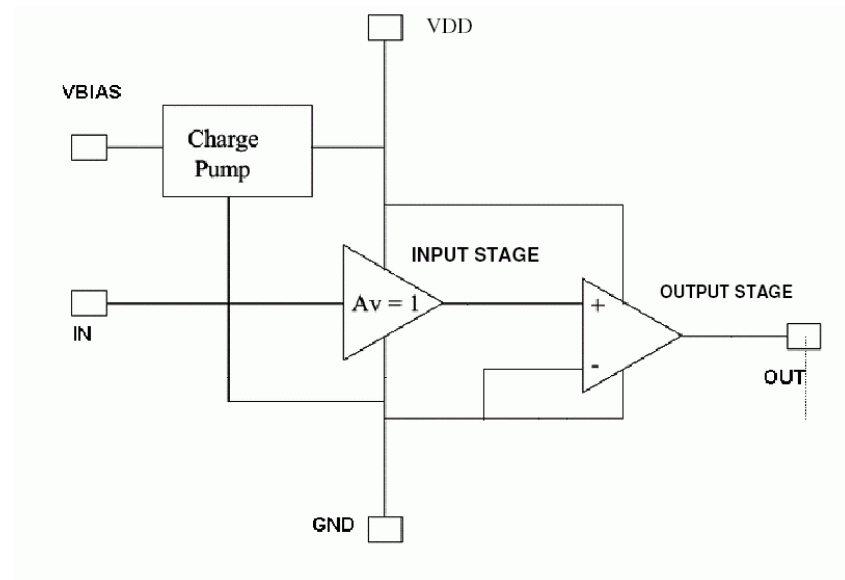
Low noise audio amplifier

Specification : $7\mu\text{V}$ @ 0.5pF load for LF BW 1.5-14kHz

Simulated : $t_m=2.7\mu\text{V}$; $w_c=3.5\mu\text{V}$

Measurement : $3.06\mu\text{V}$ for several circuits

→ good agreement with the
LF noise WC models



Status Quo - Software, Models, Equipment ...

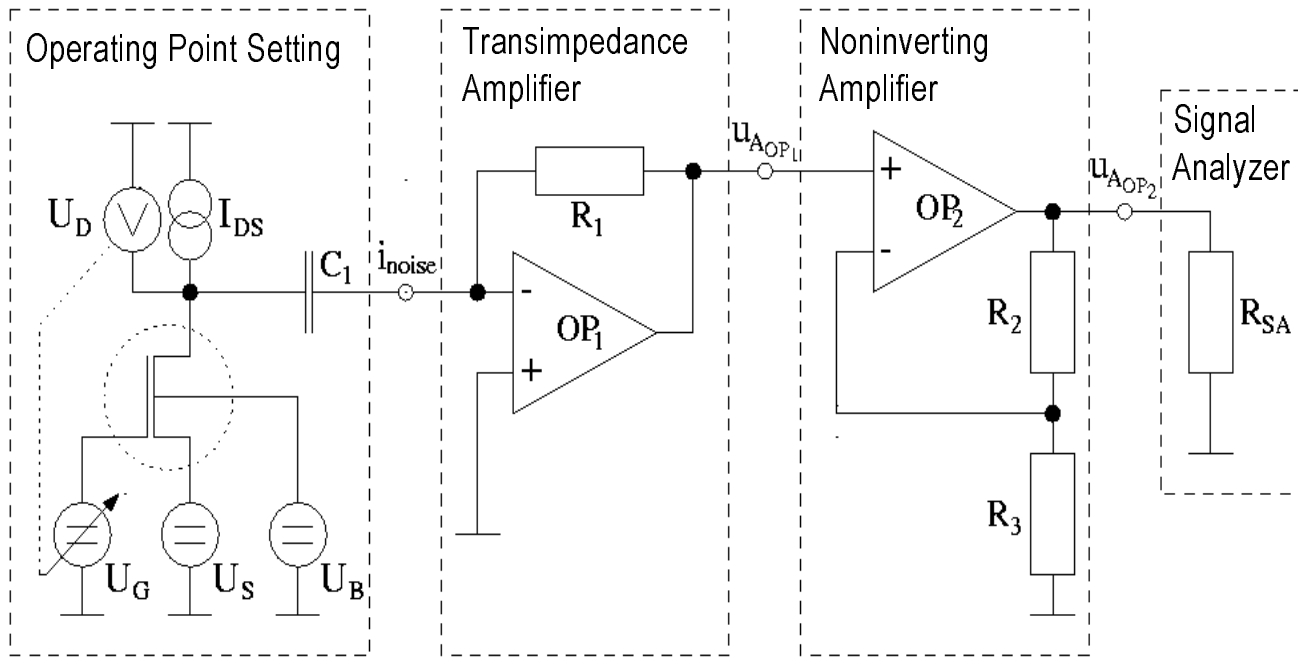
Supported models	:	BSIM3v3, (SPICE)
Supported Simulators	:	SPECTRE, ELDO, ...
Extraction environment:		MATLAB, ICCAP
Measurement Software:		LABVIEW (HP4155, HP89410A), (ICCAP)
Processes	:	0.35μm CMOS and High Voltage CMOS (\geq50V) BiCMOS

Summary

- For LF noise critical designs → sample spread for design optimization
- Methodology for WC generation and simulator implementation
- Benchmark with a design example

Thank you very much for your attention!

APPENDIX - Noise Box - pictures



Biasing Concept:

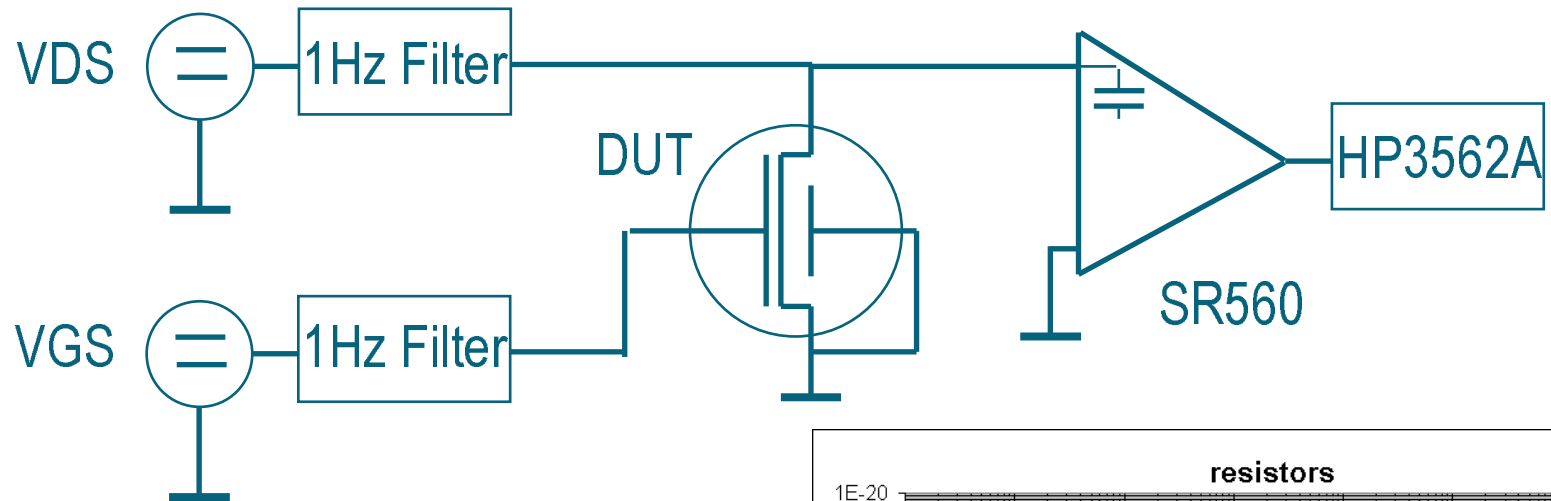
SMU and battery driven buffer amplifier (in house development)
totally screened in a metal box for packaged devices

Electrical specifications: $V_{GS} = \pm 0$ to 8V; $V_{DS} = \pm 0$ to 8V; V_{BS} additionally (also ± 0 to 8V)

$I_{DS} = 1\mu A$ to $200\mu A$

Freq. = 100Hz to 30kHz (with some restrictions to 100kHz; 2.5 to 3 decades)

APPENDIX – On wafer equipment



Biasing Concept: SMU with 1Hz filters

Electrical specifications:

VGS= 0 to +-10V, VDS= 0 to +-3V

IDS= 1µA to 100µA, GSG probes only

Freq.= 1Hz to 1kHz (with some restrictions to 100kHz)

