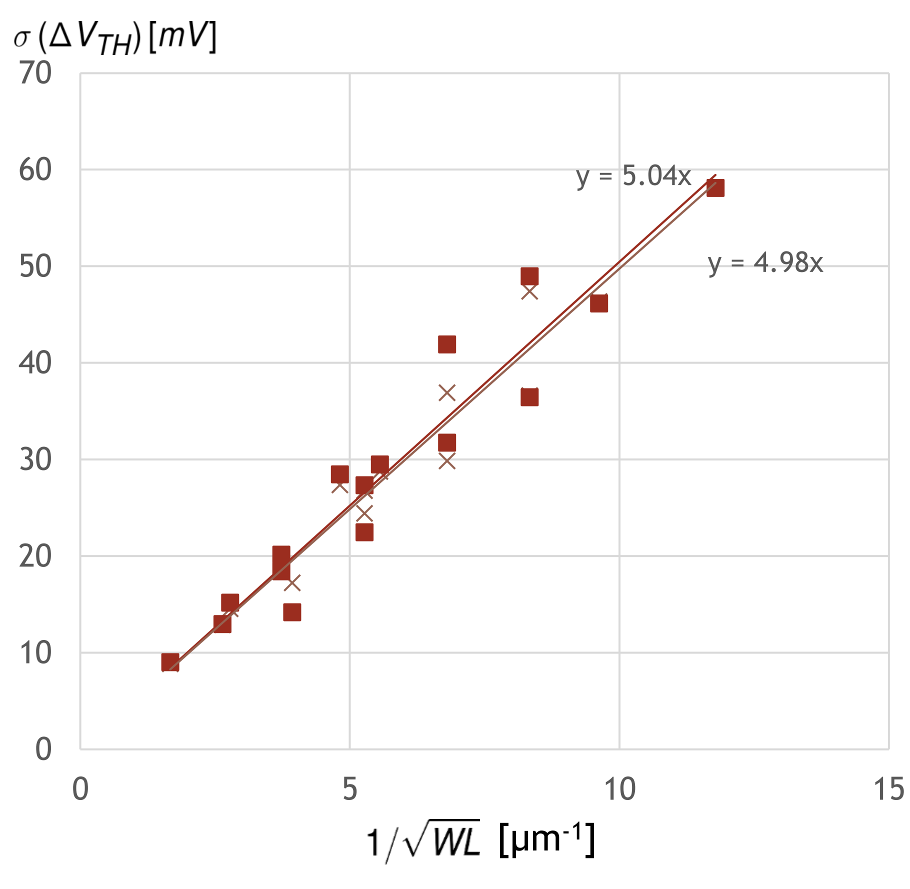
MOSFET mismatch characterization made easier: A 2-Transistor test array structure for a voltage-only measurement approach

Juan Pablo Martinez BRITO*, Sergio BAMPI**
*IMPINJ Brazil
**Federal University of Rio Grande do Sul (UFRGS)

Let's start backwards…



$$\sigma(\Delta V_{TH}) = \frac{A_{V_{TH}}}{\sqrt{WL}}$$

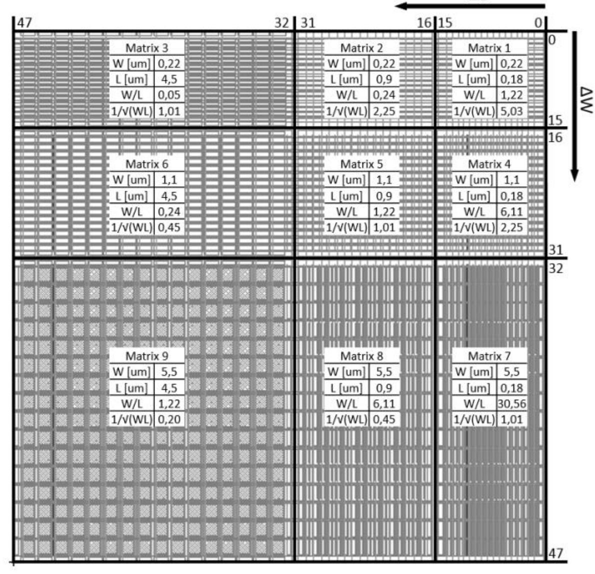
A_{VTH} = 4.98 mV. μm ⇨ Traditional method

A_{VTH} = 5.04 mV. μm ⇨ New method

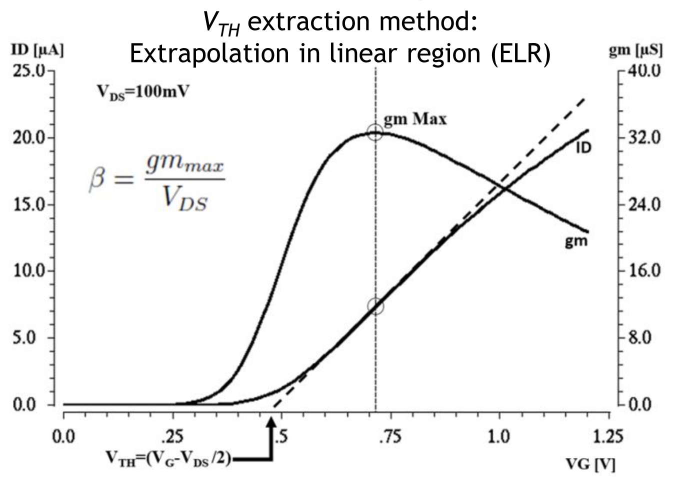
About 1% error when extracting A_{VTH}

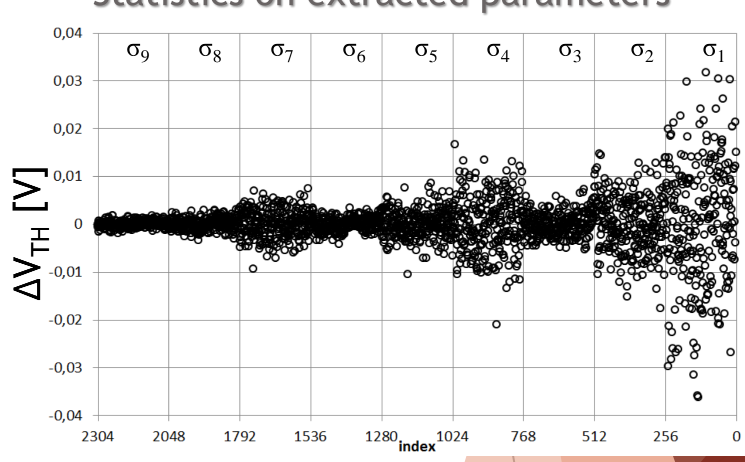
Traditional Method - Mismatch evaluation

Measure lots of same size devices



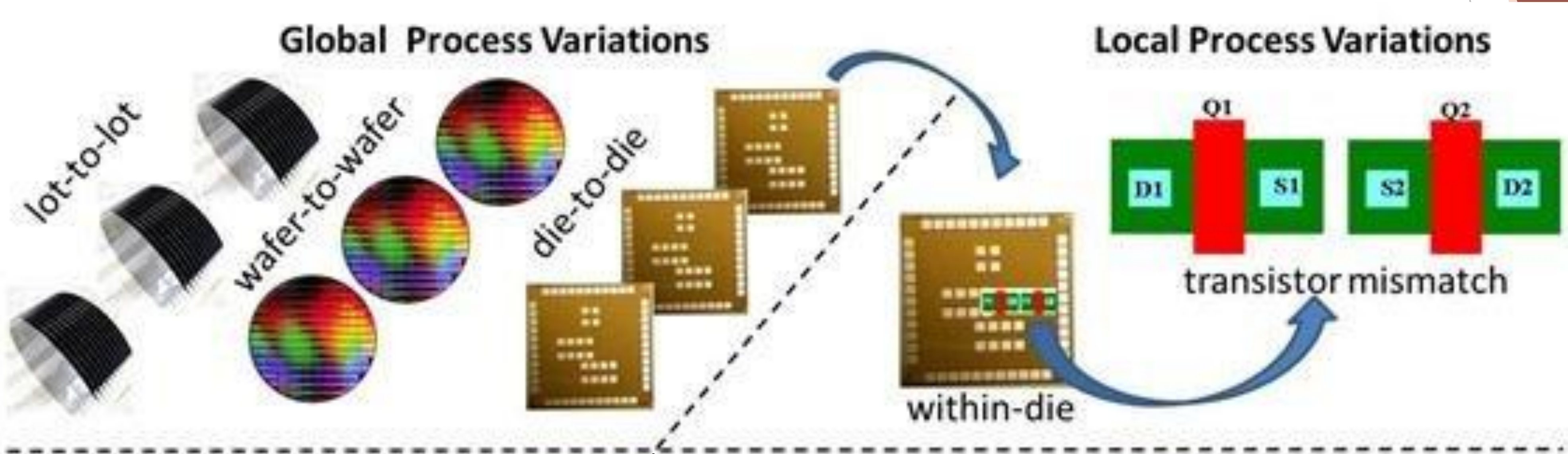
Extraction MOSFET parameters





Long testing periods due to large numbers of DUTs that requires to be measured with a high precision test equipment.	Involves parameters extraction methods that sometimes gives noisy values due to math (derivatives and/or divisions, etc)	Requires lot of data post-processing sometimes taking long time due to its complexity.

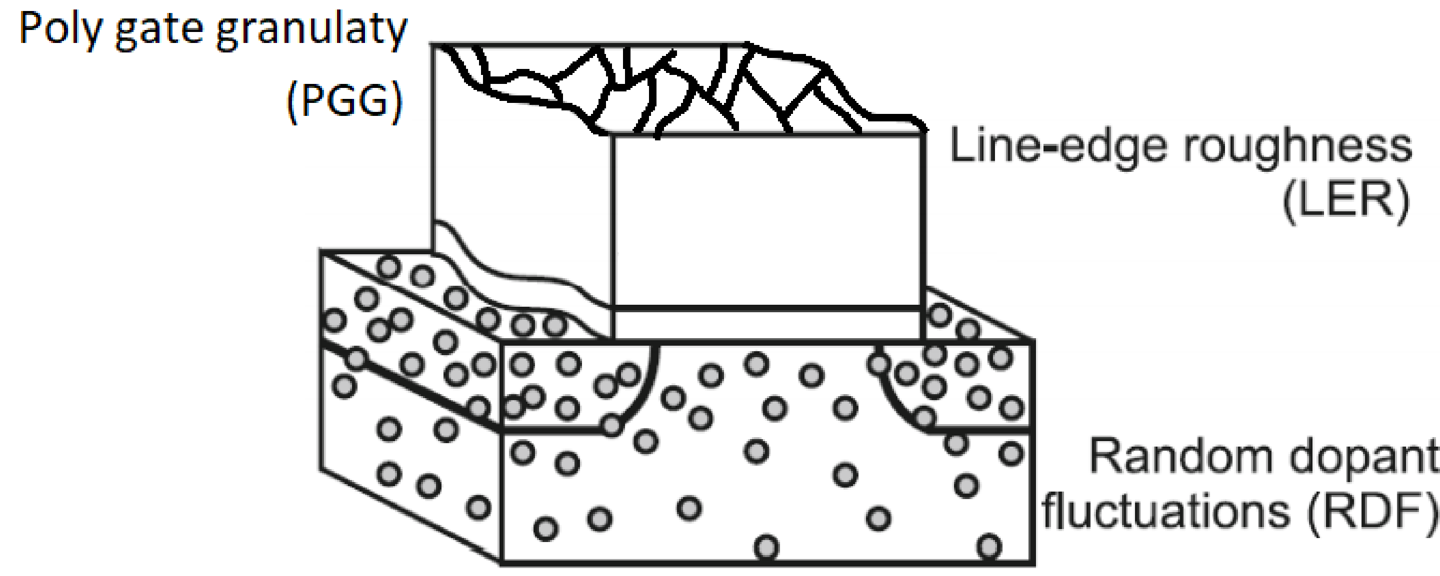
Variability Classification



- Systematic behavior.
- Independent on device size.
- Handled by fab process control.

- Random in nature.
- Dependent on device size.
- Random effects are harder to control on the manufacturing side

Major sources of local variations in a bulk MOSFET

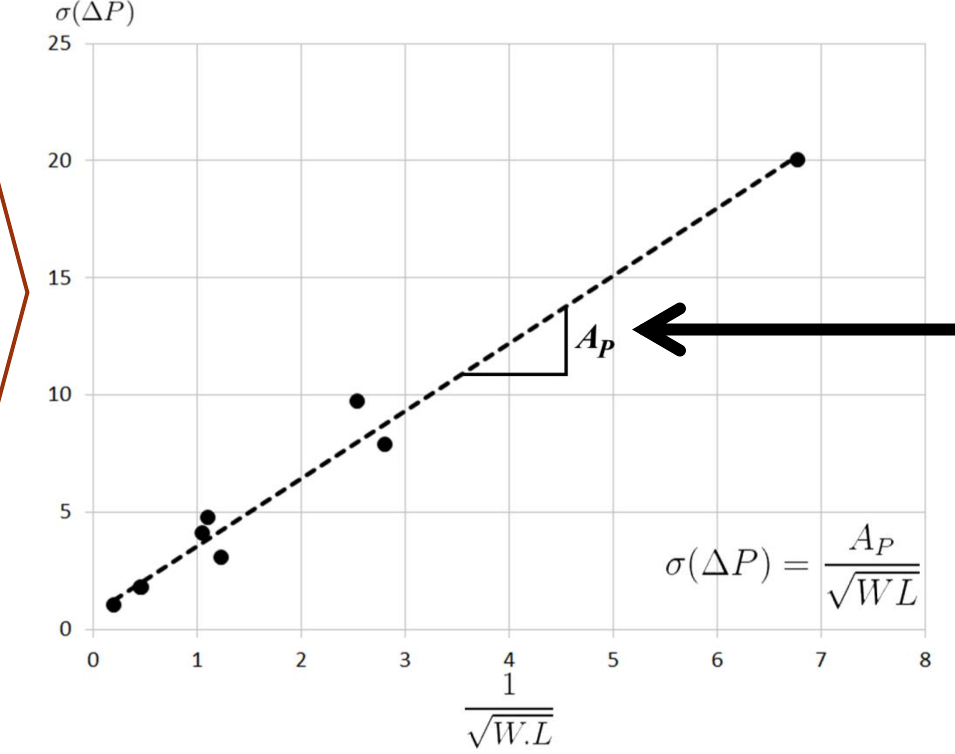


Other sources of variability: Oxide thickness variation (OTV), Free charge trapping/detrapping, etc.

Pelgrom Model

The standard deviation of the mismatch of a generic parameter P (σ(ΔP)) is linearly and directly proportional do the square root of the area (1/√(WL)).

PELGROM, Marcel et al. Matching properties of MOS transistors. **IEEE Journal of solid-state circuits**, v. 24, n. 5, p. 1433-1439, 1989.



The slope (A_P) of this curve is used for Monte Carlo statistical analisys of Analog Integrated Circuits.

Key transistor parameters for mismatch modeling

The major keys parameters affected by transistor mismatch are:

- Threshold voltage (V_{TH})
- Current factor ($\beta = \mu_0 C_{ox} W/L$)

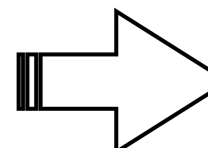
$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \left(\frac{gm}{I_D}\right)^2 \cdot \sigma^2(\Delta V_{TH})$$

General MOSFET current mismatch model for all regions of operation

Challenges in MOSFET Mismatch Measurements

Measuring MOSFET mismatches requires:

- ✓ **Long Testing Times**
- ✓ **Large I_D vectors for several biases**
- ✓ **Large Number of Samples**
- ✓ **Lots of Data Post-processing**
- ✓ **Test Equipment High Accuracy.**
- ✓ **Design of Special Test Structures**

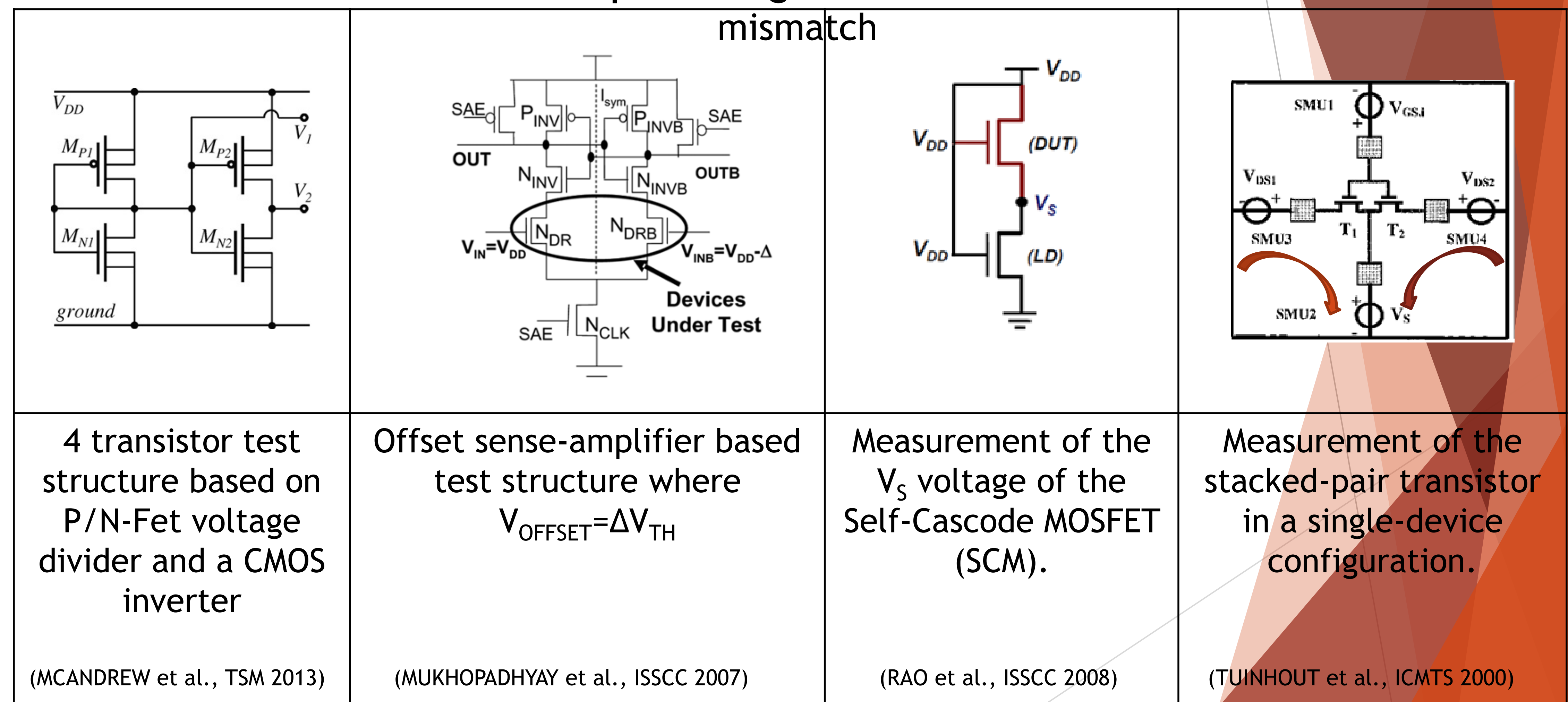


*Hence a **NEW TEST STRUCTURE*** and ***MEASUREMENT METHODOLOGY*** is required in order to obtain **fast** process variability data with **reliable results.**

A mandatory need to support the introduction of new devices in new process nodes.

Related work

Test structures based on a **pre-configured circuit** for indirect measurement mismatch



4 transistor test structure based on P/N-Fet voltage divider and a CMOS inverter	Offset sense-amplifier based test structure where $V_{OFFSET}=\Delta V_{TH}$	Measurement of the V_S voltage of the Self-Cascode MOSFET (SCM).	Measurement of the stacked-pair transistor in a single-device configuration.
(MCANDREW et al., TSM 2013)	(MUKHOPADHYAY et al., ISSCC 2007)	(RAO et al., ISSCC 2008)	(TUINHOUT et al., ICMTS 2000)

The inspirational paper (JJAP 2008)

Commonly used in Analog IC circuits as:

- **VPTAT generator,**
- **High output transresistance ,**
- **VREF generator,**
- Even for **Automatic analog circuit generation!**

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Test Circuit for Evaluating Characteristics Mismatch in Metal–Oxide–Semiconductor Field-Effect Transistor Pairs by Estimating Conductance Variation through Voltage Measurement

Mamoru TERAUCHI* and Kazuo TERADA

Faculty of Information Sciences, Hiroshima City University, Hiroshima 731-3194, Japan

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A procedure is described for evaluating characteristics mismatch in a pair of metal–oxide–semiconductor field-effect transistors (MOSFETs), which are nominally designed to be identical. This procedure is based on conductance variation estimation through voltage measurement. By measuring the gate voltage dependence of the voltage of the middle point of a MOSFET pair connected in series, various pieces of information on difference in characteristics (e.g., channel width difference and threshold voltage difference) in the MOSFET pair can be extracted. The applicability of the proposed procedure to fabrication process monitoring is also described and the principle of a suitable test circuit structure is illustrated.
[DOI: 10.1143/JJAP.47.4480]

KEYWORDS: MOSFET pair, conductance measurement, characteristics mismatch, fabrication process monitor

1. Introduction

There are many circuit blocks such as sense amplifiers utilized in dynamic random access memories and cross-coupled inverter pairs consisting of static random access memory cells that require the precise matching of characteristics of their circuit elements. Among them metal–oxide–semiconductor field-effect transistors (MOSFETs) are of utmost concern, since the fluctuation of their characteristics becomes significant as their nominal size decreases. This is because the fluctuation of their characteristics originates mainly from the spatial distribution of impurity atoms in the gate depletion layer, which is determined by stochastic processes.[1–4] That is, this type of characteristics fluctuation cannot be controlled in principle, and frequently referred to as "random characteristics variation". On the other hand it is

*MOSFET stacked-pair test structure

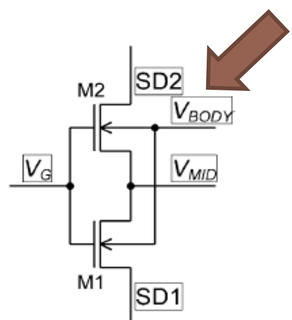
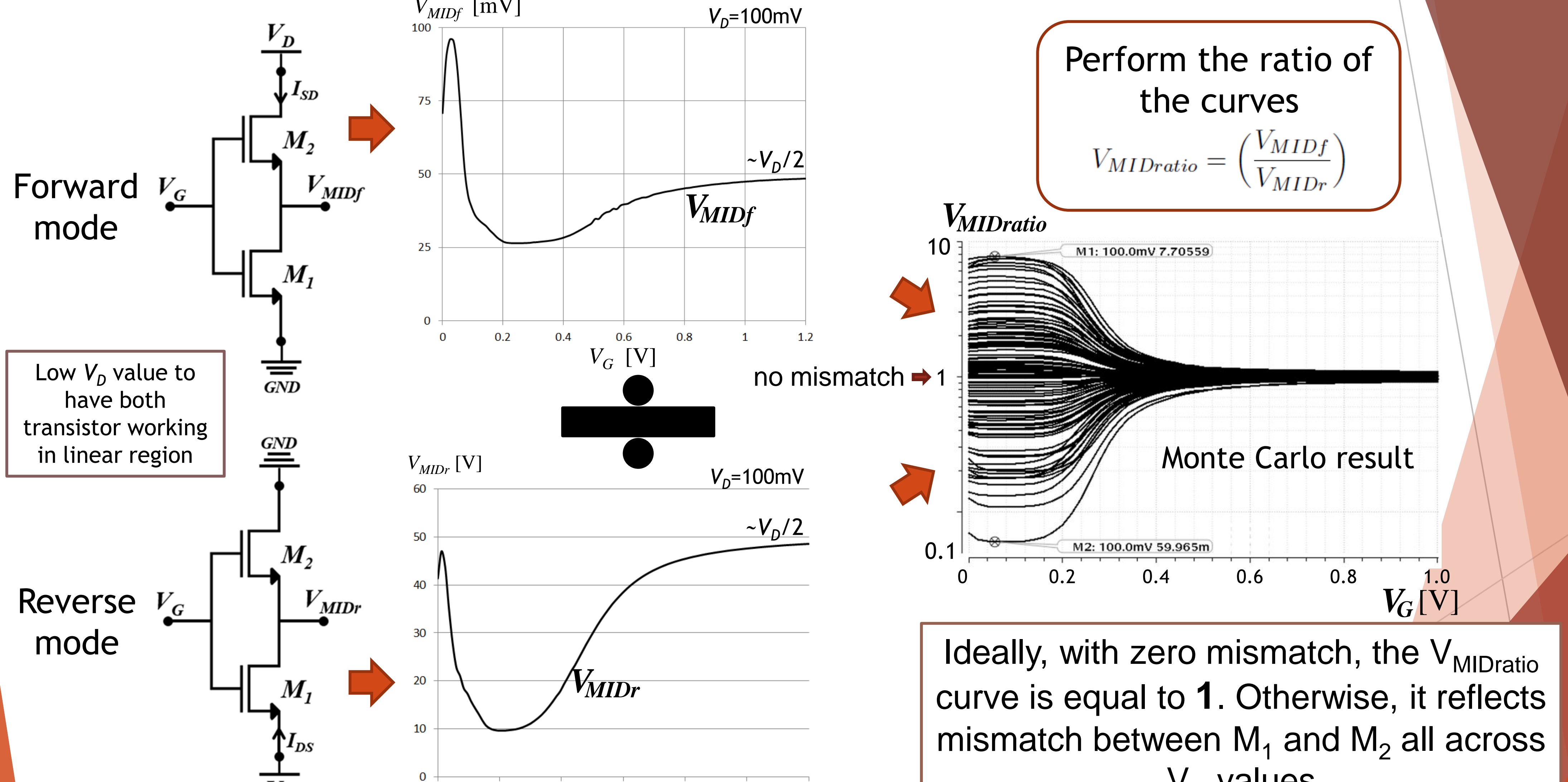


Fig. 1. Circuit diagram of test circuit composed of two MOSFETs (namely, M1 and M2) connected in series. These two MOSFETs have one body terminal in common to form the V_{BODY} terminal, with both gate terminals connected to each other to form the V_G terminal. The drain of M1 is connected to the source of M2, forming the V_{MID} terminal. The source of M1 is designated as the SD1 terminal while the drain of M2 is

Terauchi & Terada method



Ideally, with zero mismatch, the $V_{MIDratio}$ curve is equal to **1**. Otherwise, it reflects mismatch between M_1 and M_2 all across V_G values

EKV MOS Transistor Test Structure Modeling

from EKV model $I_D = I_S . e^{\frac{V_P}{U_T}} . \left[e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}} \right]$; $V_P \cong \frac{V_G - V_{TH}}{\eta}$; $I_S = 2\eta\beta U_T^2$

where η is the slope factor, $\beta = \mu_0 C_{ox} W/L$, V_P is the pinch-off voltage, V_{TH} is the threshold voltage.

Assuming that the current is the same in forward and reverse modes

$$I_{SD} = -I_{DS}$$

Weak Inversion

$$I_{S1} . e^{\frac{V_{P1}}{U_T}} . \left(1 - e^{\frac{-V_{MIDf}}{U_T}}\right) = I_{S2} . e^{\frac{V_{P2}}{U_T}} . \left(1 - e^{\frac{-V_{MIDr}}{U_T}}\right)$$

Taylor approx

$$\left(\frac{I_{S2}}{I_{S1}}\right) . e^{\left(\frac{V_{P2} - V_{P1}}{U_T}\right)} = \frac{\left(1 - e^{\frac{-V_{MIDf}}{U_T}}\right)}{\left(1 - e^{\frac{-V_{MIDr}}{U_T}}\right)} \cong \frac{V_{MIDf}}{V_{MIDr}} = V_{MIDratio}\Big|_{wi} = R_{wi}$$

$$ln(R_{wi}) = ln\left(\frac{\eta_2}{\eta_1}\right) + ln\left(\frac{\beta_2}{\beta_1}\right) + \frac{1}{U_T}\left[\frac{V_G(\eta_1 - \eta_2)}{\eta_1 . \eta_2} + \frac{\eta_2 V_{TH1} - \eta_1 V_{TH2}}{\eta_1 . \eta_2}\right]$$

IF $\eta_2 = \eta_1 = \eta$

$$ln(R_{wi}) = ln\left(\frac{\beta_2}{\beta_1}\right) + \left(\frac{\Delta V_{TH}}{\eta U_t}\right)$$

Can be approximated to $ln(R_{wi})n \approx \left(\frac{\Delta V_{TH}}{\eta U_T}\right)$

Strong Inversion

$$\eta_1 \beta_1 V_{P1} V_{MIDf} = \eta_2 \beta_2 V_{P2} V_{MIDr}$$

$$\frac{\eta_2 \beta_2 V_{P2}}{\eta_1 \beta_1 V_{P1}} = \frac{V_{MIDf}}{V_{MIDr}} = V_{MIDratio}\Big|_{si} = R_{si}$$

$$R_{si} = \frac{\eta_2 \beta_2}{\eta_1 \beta_1}\left(\frac{V_G - V_{TH2}}{\eta_2}\right)\left(\frac{\eta_1}{V_G - V_{TH1}}\right) = \frac{\beta_2 (V_G - V_{TH2})}{\beta_1 (V_G - V_{TH1})}$$

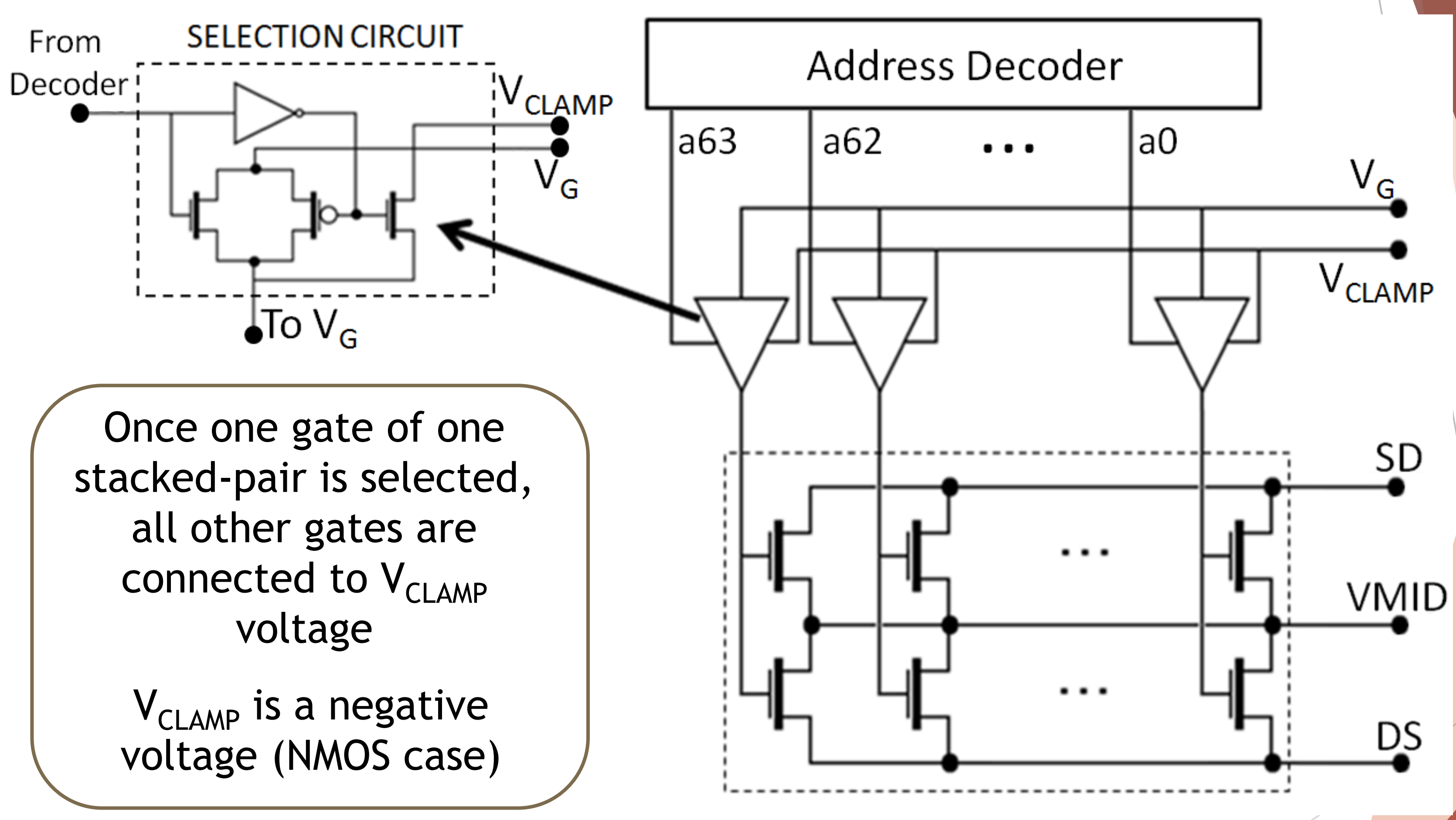
$$ln(R_{si}) = ln\left(\frac{\beta_2}{\beta_1}\right) + ln\left(\frac{V_G - V_{TH2}}{V_G - V_{TH1}}\right)$$

Must solved iteratively

V_G is the same for both transistors

Can be approximated to $ln(R_{si})n \approx ln\left(\frac{\beta_2}{\beta_1}\right)$

Addressable test structure circuit integration

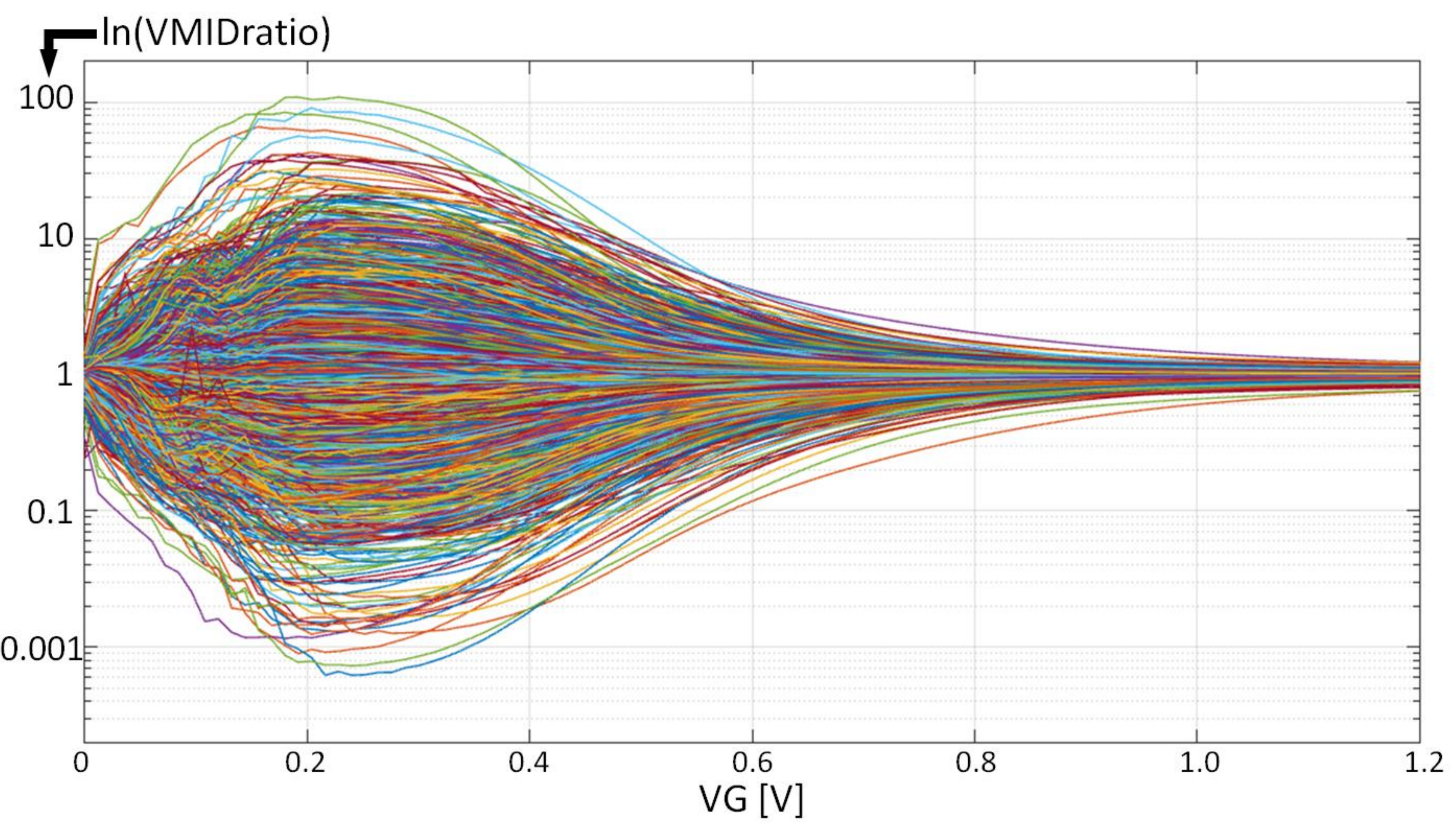


Once one gate of one stacked-pair is selected, all other gates are connected to V_{CLAMP} voltage

V_{CLAMP} is a negative voltage (NMOS case)

Same bias/switching scheme principle as used in :
(AGARWAL et al., VLSI Symp 2006)

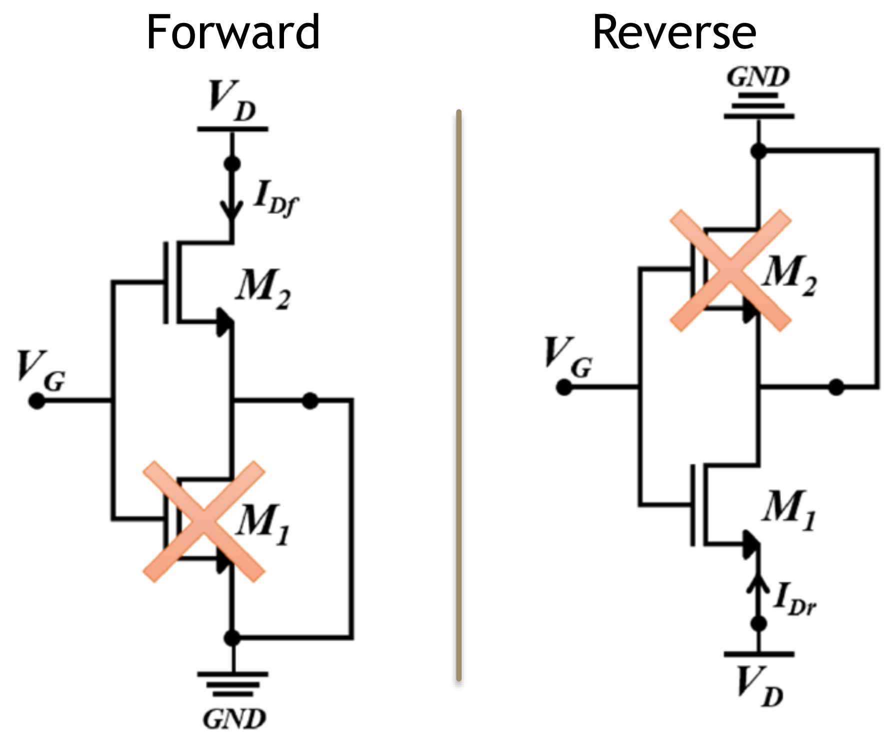
Measurements of ln($V_{MIDratio}$) versus V_G

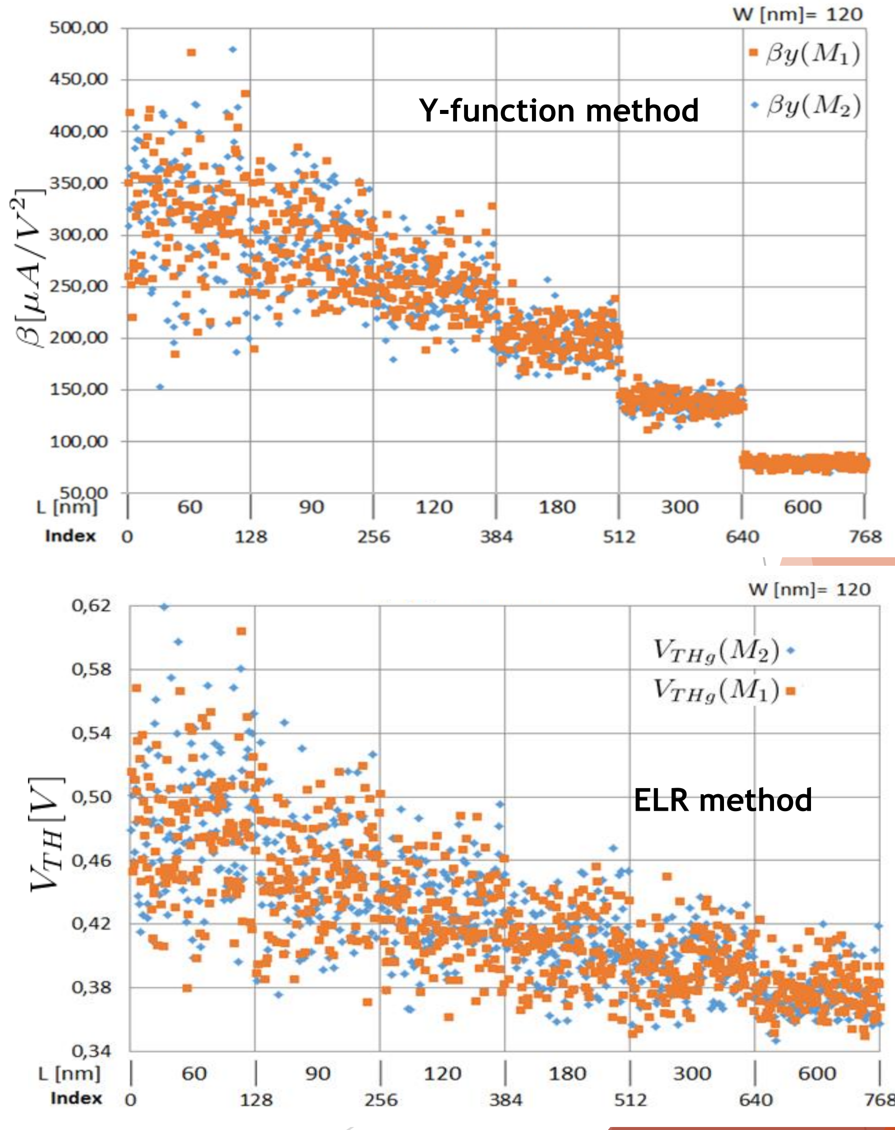


Can we extract ΔVth & ΔBeta variability separately from this curve?
Answer: **LINEAR REGRESSION ANALYSIS**

Single-Transistor Measurements

Before linear regression analysis...





Enables the evaluation of each transistor of the stacked-pair individually

TUINHOUT, Hans. **ICMTS 2000.**

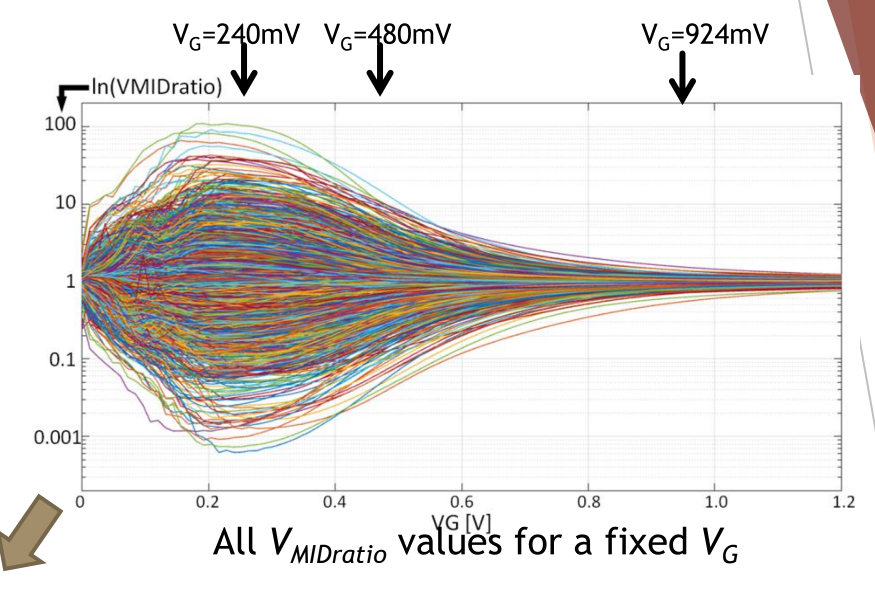
Linear Regression procedure

Model equation parameters can be extracted for a **single-transistor** configuration

$$ln(R_{wi}) = ln\left(\frac{\beta_2}{\beta_1}\right) + \left(\frac{\Delta V_{TH}}{\eta U_t}\right)$$

or

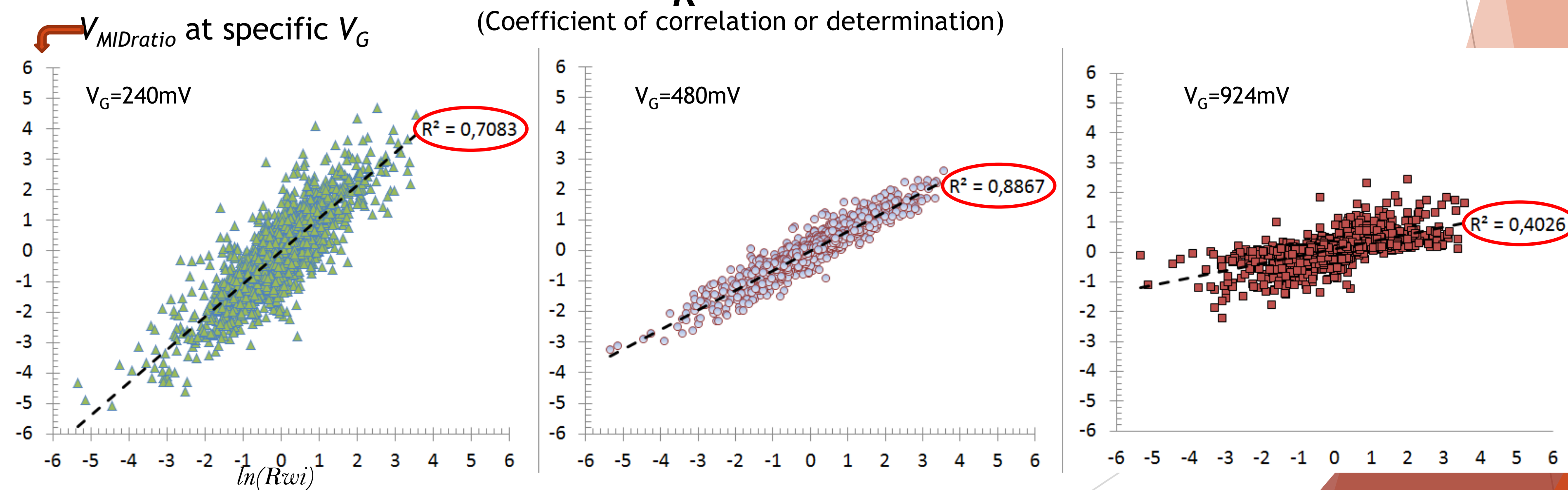
$$ln(R_{si}) = ln\left(\frac{\beta_2}{\beta_1}\right) + ln\left(\frac{V_G - V_{TH2}}{V_G - V_{TH1}}\right)$$



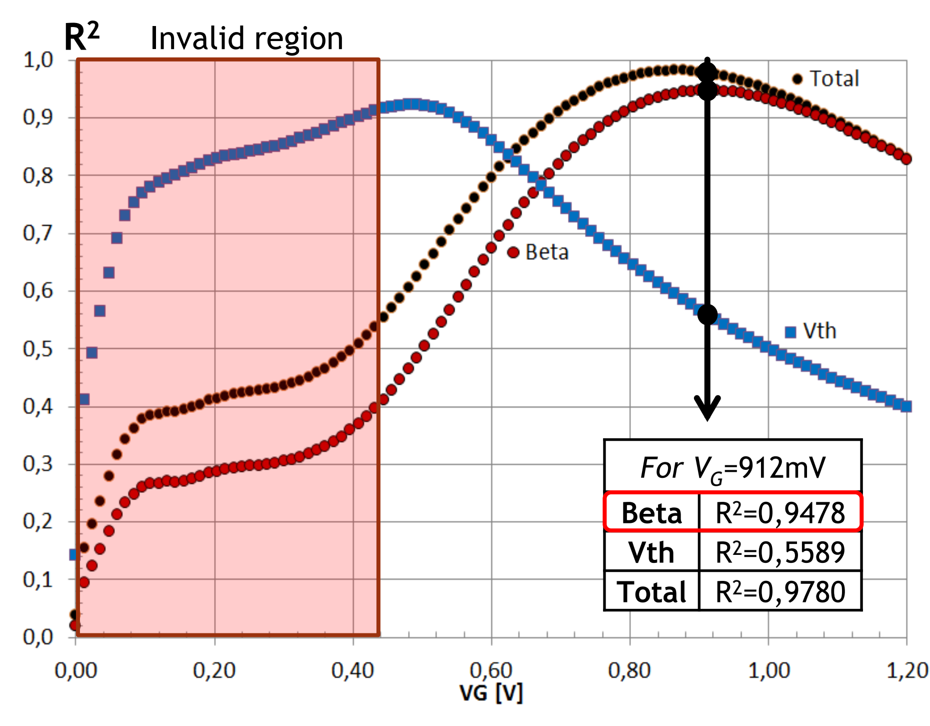
All $V_{MIDratio}$ values for a fixed V_G

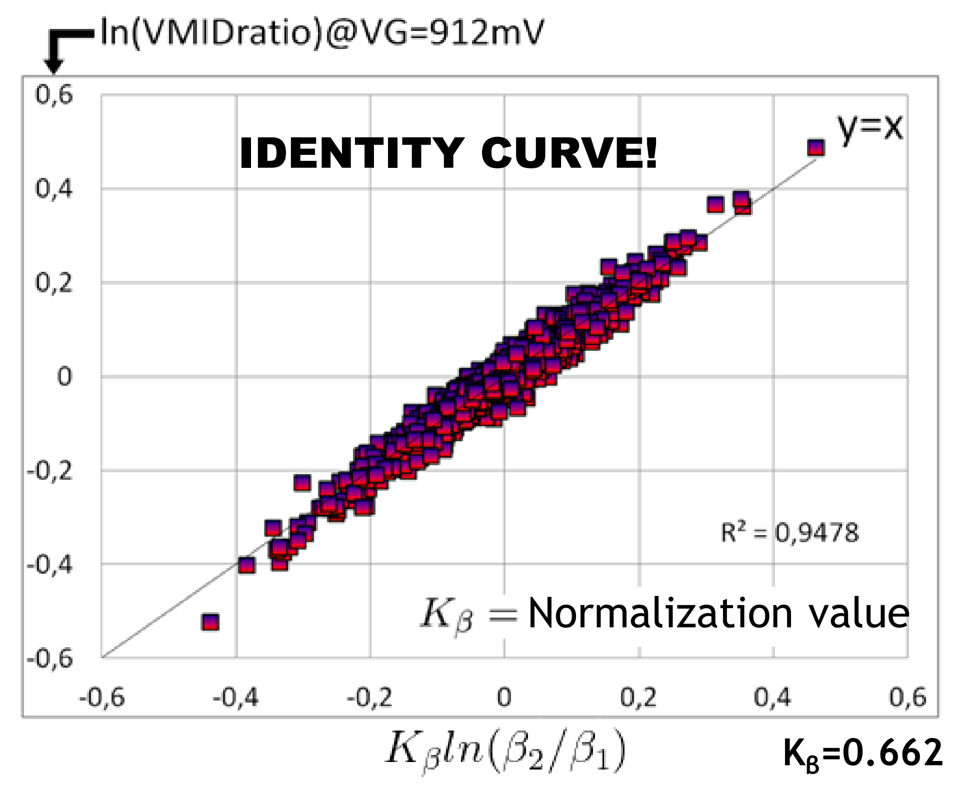
R^2
(Coefficient of correlation or determination)

$V_{MIDratio}$ at specific V_G



Correlation results – Strong Inversion



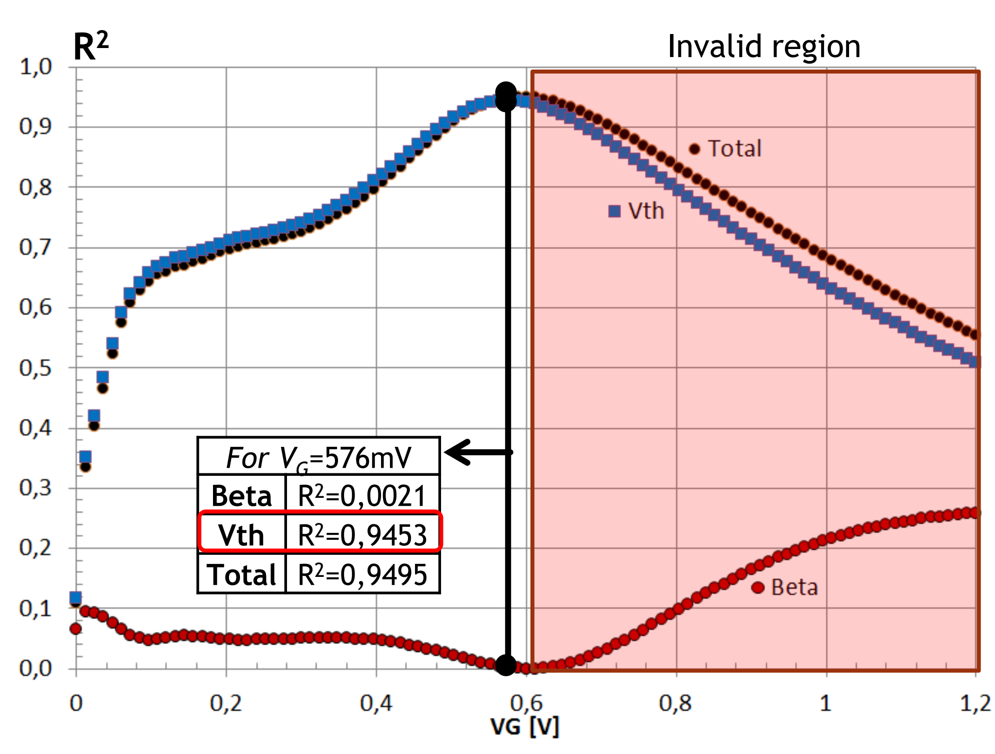


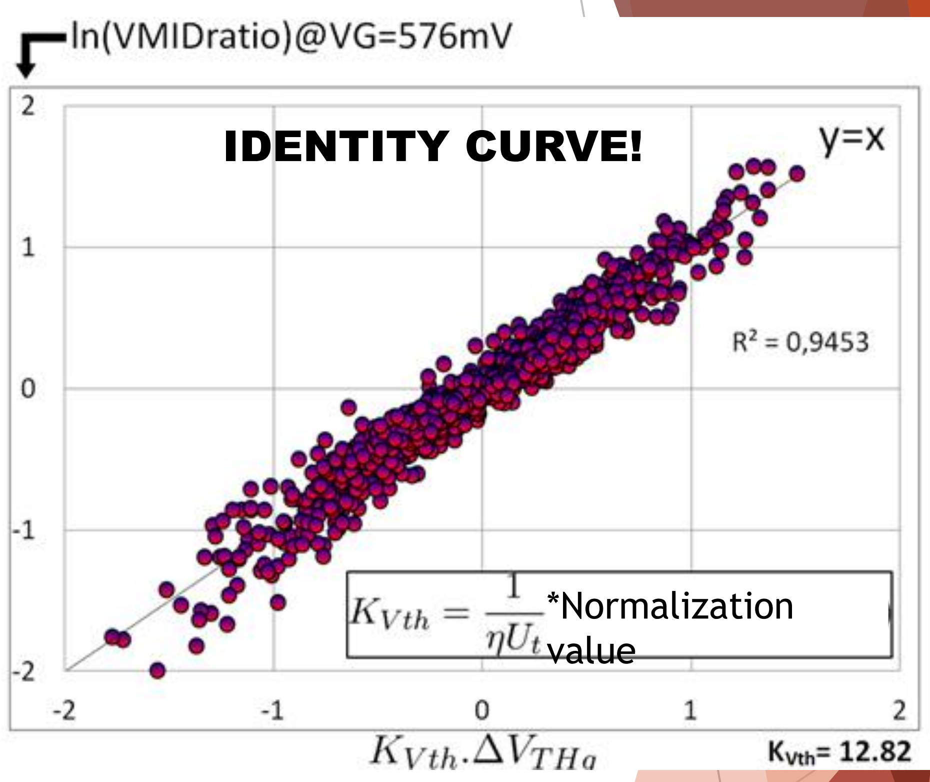
● Total ● Beta ■ Vth

$$ln(R_{si}) = ln\left(\frac{\beta_2}{\beta_1}\right) + ln\left(\frac{V_G - V_{TH2}}{V_G - V_{TH1}}\right) \xRightarrow{\text{approx}} ln(R_{si})n = ln\left(\frac{\beta_2}{\beta_1}\right) \; @V_G\text{=912mV}$$

$$\left(\frac{\Delta\beta}{\beta}\right) Eq = \frac{ln(V_{MIDratio})@V_{Gsi}}{\sqrt{2}.K_\beta}$$

Correlation results – Weak Inversion





$$K_{Vth} = \frac{1}{\eta U_t}$$

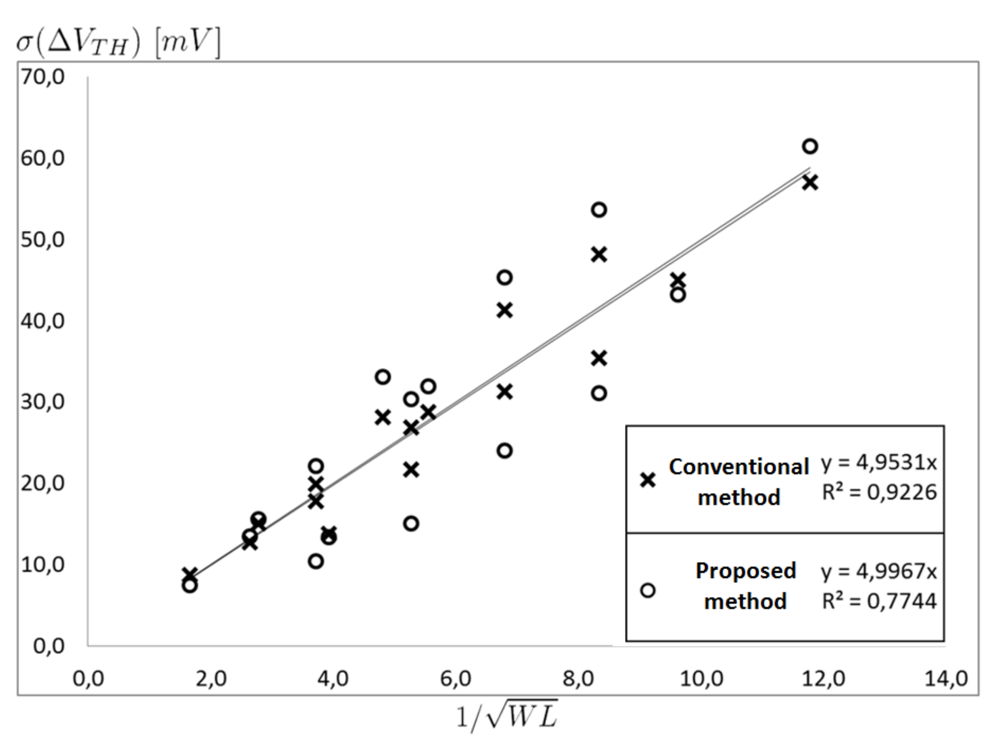
$$K_{Vth}.\Delta V_{THa}$$

● Total ● Beta ■ Vth

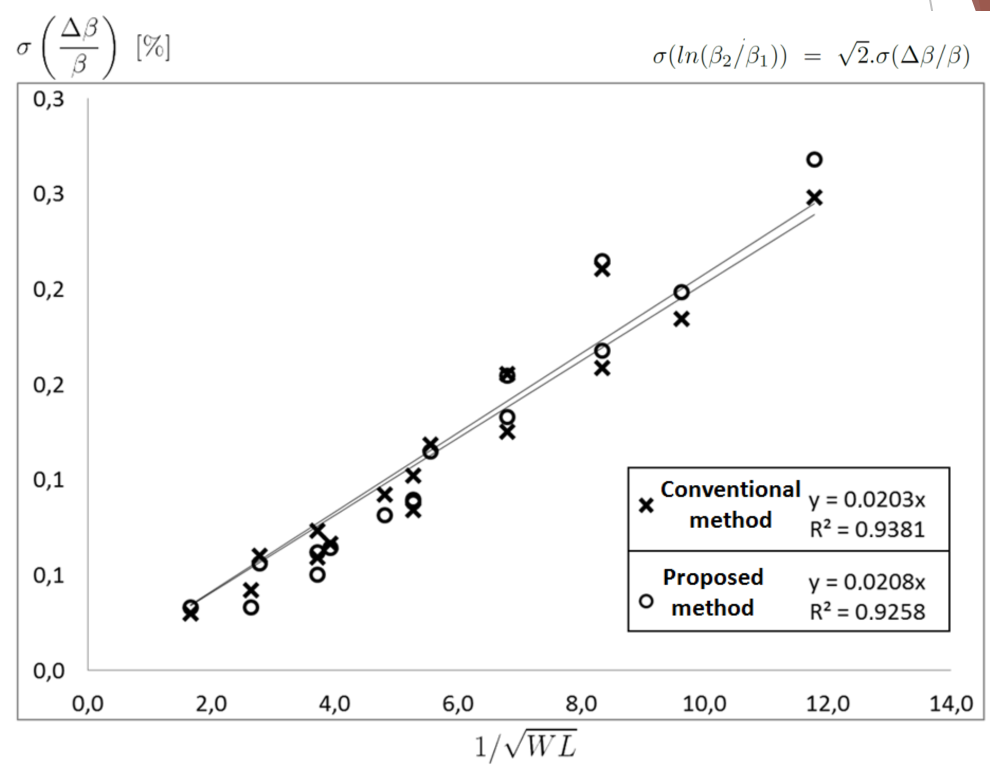
$$ln(R_{wi}) = ln\left(\frac{\beta_2}{\beta_1}\right) + \left(\frac{\Delta V_{TH}}{\eta U_T}\right) \xrightarrow{\text{approx}} ln(R_{wi})n = \left(\frac{\Delta V_{TH}}{\eta U_T}\right)$$ @V_G=576mV

$$\Delta V_{TH} Eq = \frac{ln(V_{MIDratio})@V_{Gwi}}{K_{Vth}}$$

Comparison of the $1/\sqrt{WL}$ plot



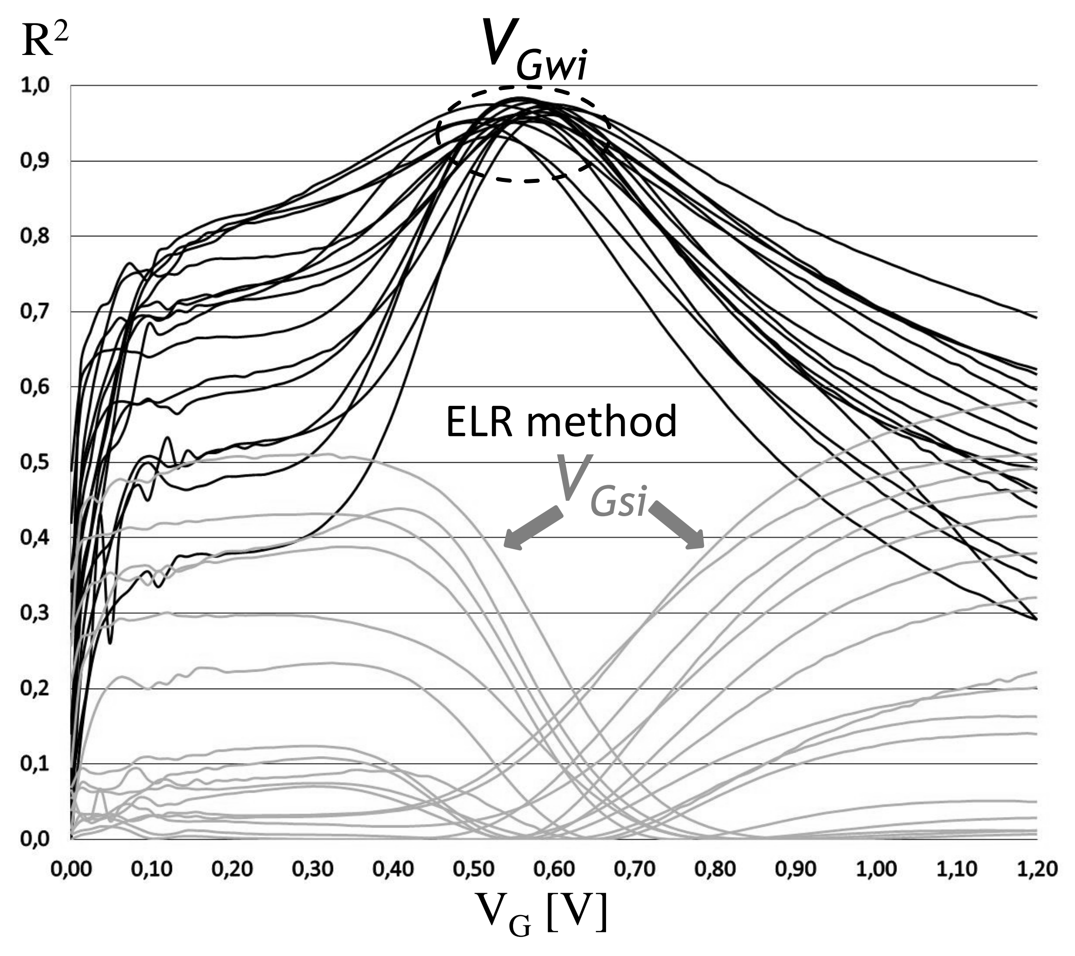
Slope A_{Vth} error is about 1%

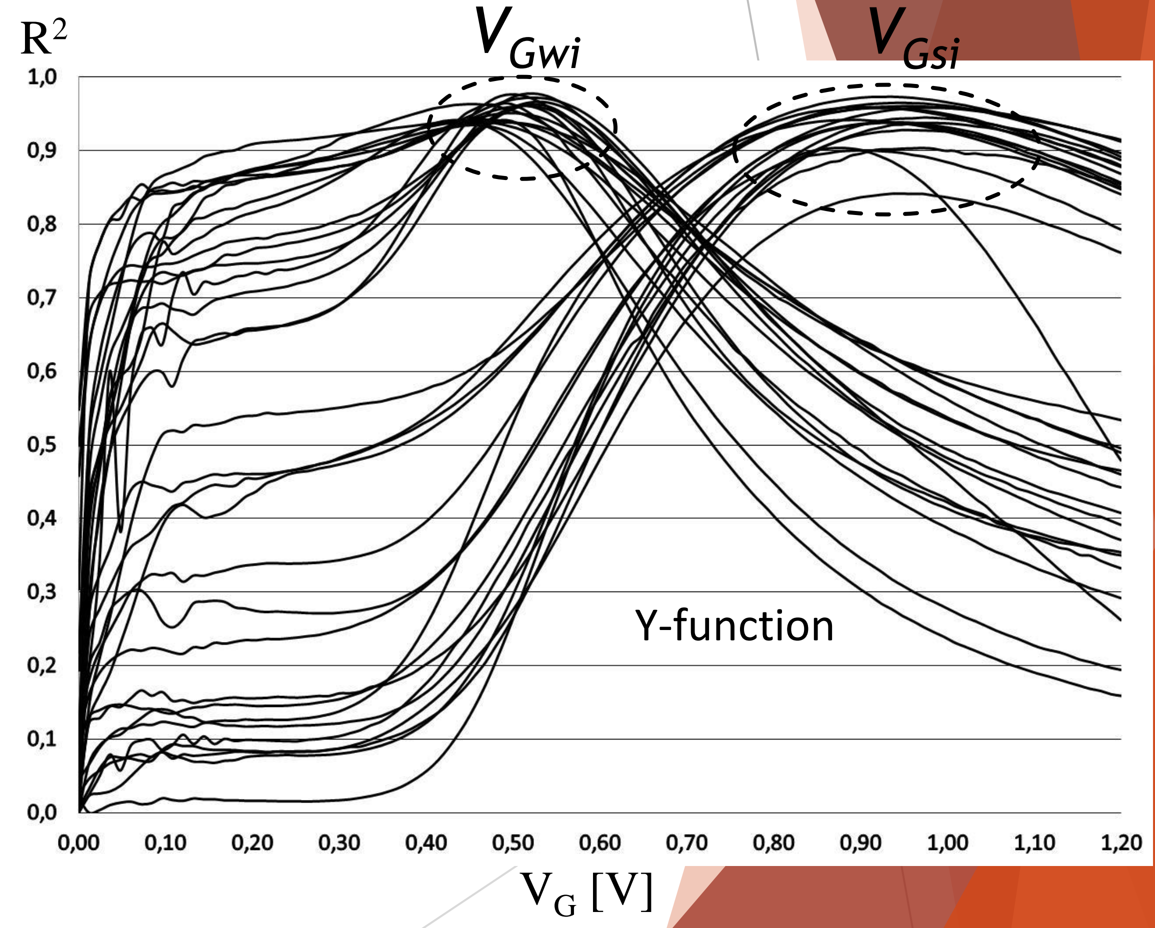


Slope A_β error is about 2%

Brito, Juan Pablo Martinez; Bampi, Sergio. Two-transistor voltage-measurement-based test structure for fast extraction of MOS mismatch design parameters. **In: 2019 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS). IEEE, 2019. p. 114-119.**

Linear regression determined separately for each same-size transistor matrix



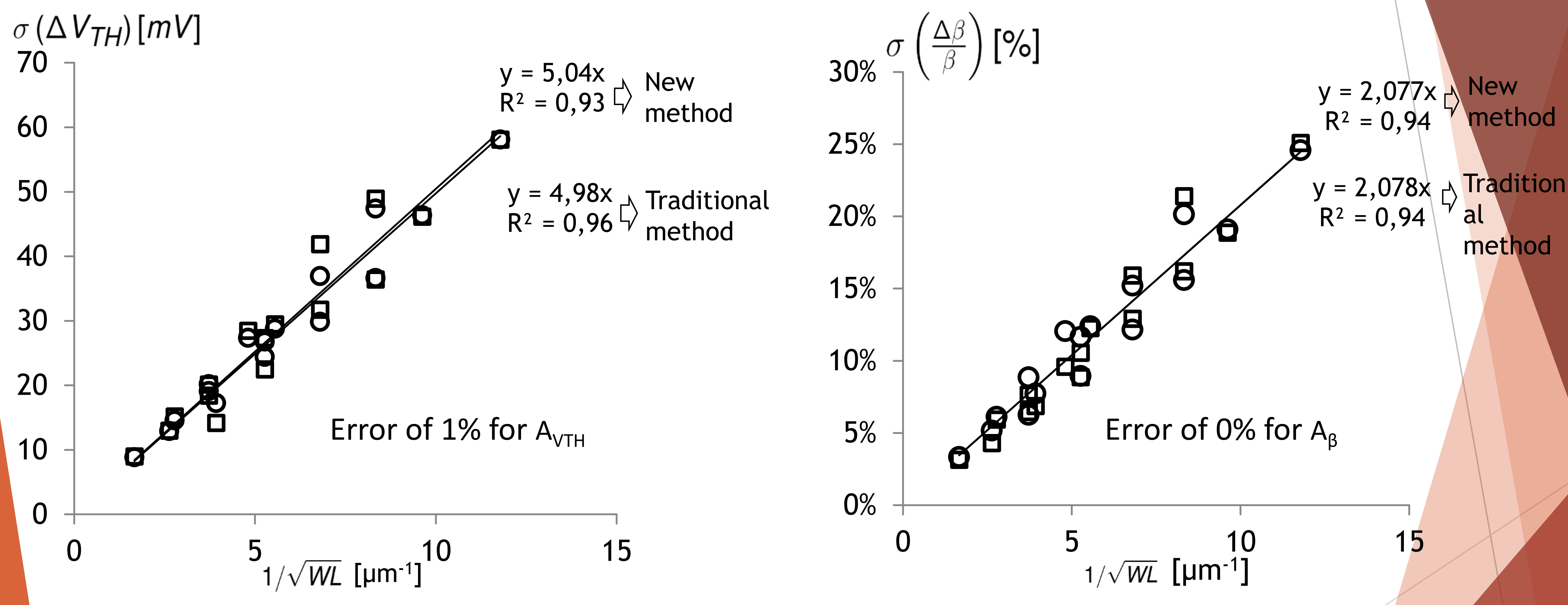


Linear regression determined separately for each same-size transistor matrix

matrix	W [nm]	L [nm]	Y-function		ELR method		Y-function		ELR method		$K_{V_{THy}}$	$K_{\beta y}$	$K_{V_{THg}}$	$K_{\beta g}$
			V_{Gwi} [mV]	V_{Gsi} [mV]	V_{Gwi} [mV]	V_{Gsi} [mV]	S_{wi}	S_{si}	S_{wi}	S_{si}				
1	600	60	528	972	576	336	1.511	0.423	0.465	-12.27	46.38	0.423	14.27	-12.27
2	240	60	492	948	600	1152	1.664	0.576	0.409	0.37	51.10	0.576	12.55	0.37
3	360	60	516	984	600	120	1.511	0.474	0.401	-10.36	46.40	0.474	12.31	-10.36
4	120	60	468	936	576	1200	1.735	0.652	0.442	0.54	53.27	0.652	13.57	0.54
5	720	60	516	972	576	288	1.730	0.425	0.486	-15.59	53.11	0.425	14.94	-15.59
6	1200	60	528	876	552	300	1.630	0.527	0.533	-13.60	50.03	0.527	16.37	-13.60
7	120	90	480	936	576	1200	1.487	0.650	0.392	0.62	45.67	0.650	12.03	0.62
8	120	120	456	912	516	1200	1.466	0.687	0.500	0.70	45.02	0.687	15.36	0.70
9	720	180	504	948	552	1200	1.484	0.555	0.495	0.41	45.57	0.555	15.20	0.41
10	600	600	492	972	552	1200	1.195	0.604	0.409	0.38	36.70	0.604	12.54	0.38
11	360	180	492	924	564	1188	1.388	0.599	0.422	0.48	42.60	0.599	12.94	0.48
12	360	90	516	924	600	324	1.537	0.593	0.397	-11.24	47.20	0.593	12.18	-11.24
13	1200	120	516	948	552	408	1.631	0.439	0.523	-13.82	50.09	0.439	16.06	-13.82
14	120	600	432	948	492	1200	1.070	0.593	0.413	0.45	32.85	0.593	12.68	0.45
15	120	300	456	900	528	1200	1.071	0.688	0.371	0.59	32.88	0.688	11.38	0.59
16	120	180	456	900	516	1200	1.257	0.704	0.445	0.72	38.60	0.704	13.66	0.72

FITTING CONSTANTS FOR EACH TRANSISTOR SIZE

Comparison of the 1/√*WL* plot



Brito, Juan Pablo Martinez; Bampi, Sergio. Two transistors voltage-measurement-based test structure for fast MOSFET device mismatch characterization. **IEEE Transactions on Semiconductor Manufacturing, v. 33, n. 2, p. 166-173, 2020.**

Heatmap comparison

Reproduces ΔV_{TH} and $\Delta\beta/\beta$ mismatch parameters separately and with the same geometrical space-distribution

Traditional Method

ΔV_{TH}

	8	7	6	5	4	3	2	1
8	1,70	-4,55	7,92	-7,76	7,40	-19,12	4,63	-6,84
7	-11,15	-12,54	-25,25	21,48	28,49	-1,70	-17,43	13,73
6	25,76	-4,17	4,96	7,26	-3,40	-15,56	-2,54	-10,12
5	24,17	2,55	13,73	6,00	12,70	7,45	-9,12	-4,01
4	6,47	1,42	-0,52	5,41	23,51	5,54	25,29	21,53
3	15,04	17,01	4,36	-9,51	-4,12	9,26	-8,92	-5,70
2	-2,07	4,47	-2,74	4,52	6,13	-7,61	1,86	16,56
1	7,47	-3,08	-4,36	-14,18	6,01	24,15	-9,36	-32,77

$(\Delta\beta/\beta)$

	8	7	6	5	4	3	2	1
8	0,7%	-1,0%	0,8%	-5,7%	-3,9%	-3,1%	-2,3%	-0,1%
7	0,6%	-1,7%	-1,6%	0,3%	2,0%	-2,4%	1,9%	1,3%
6	-0,5%	-2,4%	2,3%	2,9%	-0,5%	2,3%	1,5%	1,3%
5	-0,6%	1,4%	-3,3%	-0,5%	-2,6%	-1,3%	-3,4%	0,7%
4	-1,6%	-1,5%	-1,3%	-0,6%	1,0%	-0,8%	-0,2%	-1,4%
3	-1,2%	0,9%	0,5%	-1,7%	2,0%	3,1%	-0,8%	0,3%
2	-0,9%	-1,3%	0,7%	0,1%	-0,9%	-1,2%	-3,4%	0,9%
1	0,7%	1,2%	1,5%	0,6%	0,7%	-0,8%	3,6%	0,3%

Proposed Method

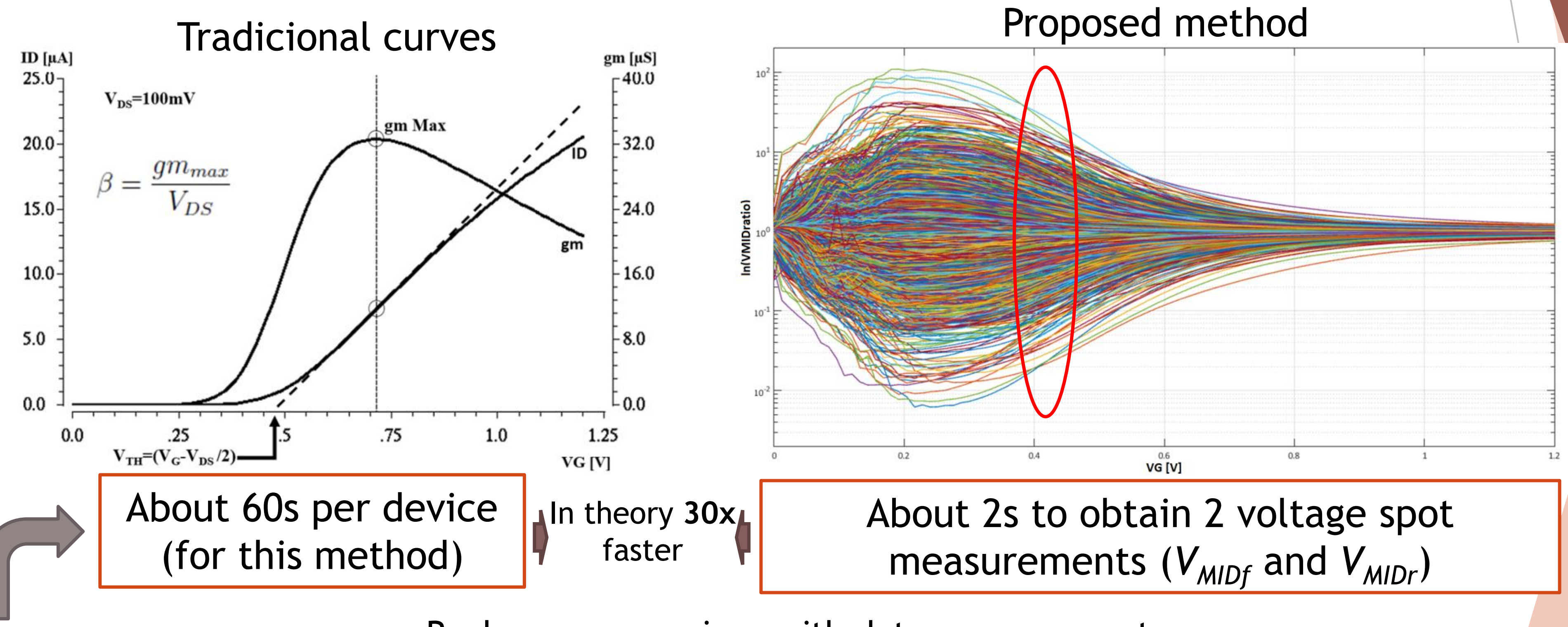
$ln(V_{Gwi})/K_{Vth}$

	8	7	6	5	4	3	2	1
8	3,99	-2,97	9,60	-11,42	3,31	-19,62	2,37	-7,94
7	-7,79	-16,36	-26,26	19,44	30,05	-2,74	-14,16	15,19
6	25,61	-2,65	7,73	9,84	-0,81	-13,30	-0,66	-11,85
5	25,70	2,51	9,13	5,52	10,70	4,20	-10,22	-3,08
4	6,32	-1,64	-2,02	6,11	27,68	4,18	26,18	20,29
3	13,99	18,01	3,21	-9,13	-0,50	8,41	-10,82	-4,48
2	-0,87	7,81	-0,26	3,62	6,64	-8,27	-3,26	18,13
1	12,62	-1,17	0,32	-9,80	6,10	26,55	-8,50	-33,98

$ln(V_{Gsi})/K_{\beta}$

	8	7	6	5	4	3	2	1
8	0,8%	-1,5%	2,3%	-4,8%	-3,4%	-4,2%	-1,4%	-2,2%
7	-0,2%	-2,1%	-2,0%	2,1%	5,6%	-1,3%	1,1%	2,5%
6	1,0%	-1,3%	4,3%	4,8%	-0,5%	0,4%	1,3%	0,3%
5	1,1%	3,3%	-1,2%	2,5%	0,4%	-0,7%	-3,4%	0,6%
4	0,0%	-0,1%	0,2%	-1,2%	2,1%	0,7%	2,7%	2,4%
3	1,7%	2,3%	2,1%	-1,6%	0,9%	3,2%	-2,2%	-0,7%
2	-1,6%	0,4%	0,9%	2,5%	-0,3%	0,0%	-4,0%	4,5%
1	2,9%	2,9%	2,7%	-1,3%	1,3%	3,4%	4,3%	-1,0%

Increase of Measurement Speed



Using the traditional ELR method Which is a built-in function in B1500A Semiconductor Device Parameter Analyzer from Keysight Technologies

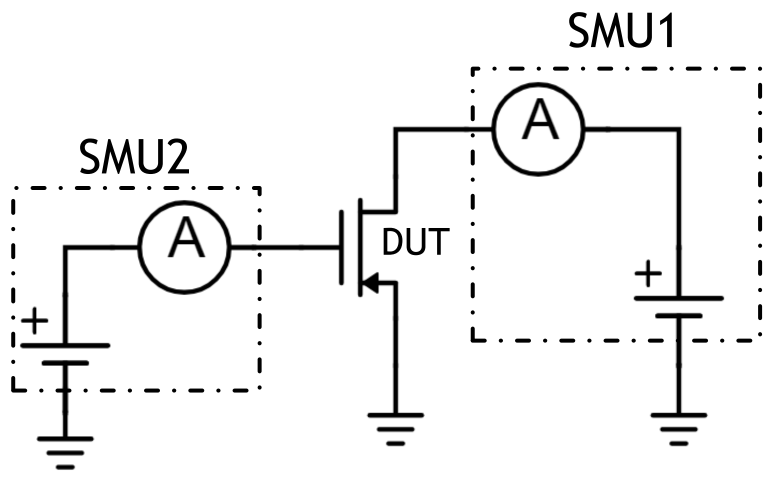
Real case comparison with data measurements

MOSFET Matrix	Start	End	Total	Seconds/Device
2304 MOS Devices I_D-V_G curves, 101 points	18:59:19 30/11/2016	04:39:23 01/12/2016	33h40min04s	52.6s
Stacked-Pairs Matrix	**Start**	**End**	**Total**	**Seconds/Device**
4096 Stacked-Pairs V_{MIDf} and V_{MIDr}, 2 points	16:44:10 26/08/2016	19:19:31 26/08/2016	02h35min21s	2.27s

$$\frac{52.6}{2.27} = 23.71\text{x}$$

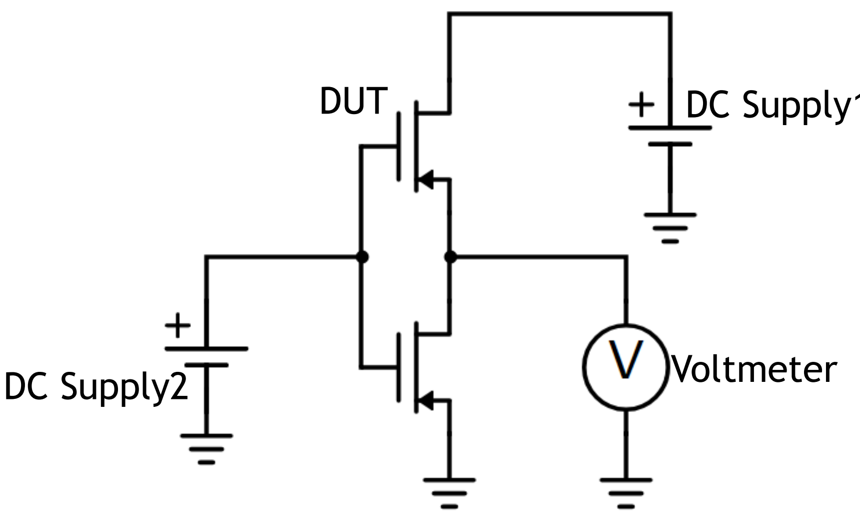
Reduction on the Measurement Setup

Traditional setup



Requires:
- At least 2 SMUs from a Parameter Analyzer.

Proposed method



Requires:
- 2 DC Voltage Supplies
- Voltmeter.

REDUCTION OF EQUIPMENT COST AND TESTING TIME

Comparison against related work

	This work	[3]	[4]	[6]	[7]	[8]
Speed Increase	30x	-	5x	-	-	-
Process	65nm	65nm	65nm	130nm	45nm	-
Parameters	$V_{TH}\&\beta$	V_{TH}	V_{TH}	V_{TH}	V_{TH}	$V_{TH}\&\beta$
Number of device	4096	800	1024	256	138	512
Transistor sizes	16	3	no	no	no	3
Regression analysis	yes	no	no	no	no	no

[3] K. Agarwal et al., "Fast characterization of threshold voltage fluctuation in mos devices," IEEE Transactions on Semiconductor Manufacturing, vol. 21, no. 4, pp. 526–533, 2008.

[4] T.-C. Luo et al., "Fast transistor threshold voltage measurement method for high-speed, high-accuracy advanced process characterization," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 5, pp. 1138–1149, 2014.

[6] S. Mukhopadhyay et al., "Statistical characterization and on-chip measurement methods for local random variability of a process using senseamplifier- based test structure," in 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, 2007, pp. 400–611.

[7] R. Rao et al., "A completely digital on-chip circuit for local-random variability measurement," in Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International. IEEE, 2008, pp. 412–623.

[8] C. C. McAndrew et al., "A self-amplifying four-transistor mosfet mismatch test structure," IEEE Transactions on Semiconductor Manufacturing, vol. 26, no. 3, pp. 273–280, 2013.

Conclusions

1. A two-transistor test structure and a simple measurement methodology demonstrates high confidence values in order to extract MOSFET mismatch parameters.
2. MOS transistor mismatch parameters such as A_{Vth} and A_{β} can be extracted with an error less than 2%, for the same test die.
3. Two great advantages of the method: an increase of **25x** in measurement speed and a simplified measurement setup.
4. The two-transistor test structure has been proven on its efficiency by linear regression analysis.
5. An improved version of the test structure has been proposed and tested in order to allow distance related mismatch evaluation.

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List of Author’s related publications

JOURNALS

1. Brito, Juan Pablo Martinez; Bampi, Sergio . Two Transistors Voltage-Measurement-Based Test Structure for Fast MOSFET Device Mismatch Characterization. IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, v. 33, p. 1-1, 2020.
2. Brito, Juan Pablo Martinez; Bampi, Sergio . Local Variability Evaluation on Effective Channel Length Extracted With Shift-and-Ratio Method. IEEE TRANSACTIONS ON ELECTRON DEVICES, v. 67, p. 4662-4666, 2020.

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1. Brito, Juan Pablo Martinez; Bampi, Sergio. Statistical Analysis of MOSFET extracted parameters for n-MOS mismatch modeling. 13th International MOS-AK Workshop; Silicon Valley, CA, Dec.10-11 2020
2. Brito, Juan Pablo Martinez; Bampi, Sergio. Two-transistor Voltage-Measurement- Based Test Structure for Fast Extraction of MOS Mismatch Design Parameters. In: 2019 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS), 2019, Kita-Kyushu City.
3. Martinez Brito, Juan Pablo; Lubaszewski, Marcelo ; Bampi, Sergio . Within-die and die-to-die variability on 65nm CMOS : oscillators experimental results. In: 2015 International Workshop on CMOS Variability (VARI), 2015, Salvador.
4. Martinez Brito, Juan Pablo; Lubaszewski, Marcelo ; Bampi, Sergio. MOSFET stacked-pair test structure for mismatch evaluation by estimating the on-resistance ratio. In: 2015 International Workshop on CMOS Variability (VARI), 2015, Salvador.
5. Brito, Juan Pablo Martinez; Bampi, Sergio. Estimation of Within-Die and Die-to-Die CMOS Variability Based on Ring Oscillators. IEEE/ACM ICCAD Workshop on Variability Modeling and Characterization (VMC). 2014. San Jose.

THANK YOU

Questions?

juanbrito@gmail.com