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On the Compact Modelling of Si Nanowire and Si Nanosheet MOSFETs

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Outline

Introduction

The Symmetric Doped Double-Gate Model - SDDGM

Application SDDGM model to nanowires and nanosheets

Model validation with: experimental transistor
simulated transistors

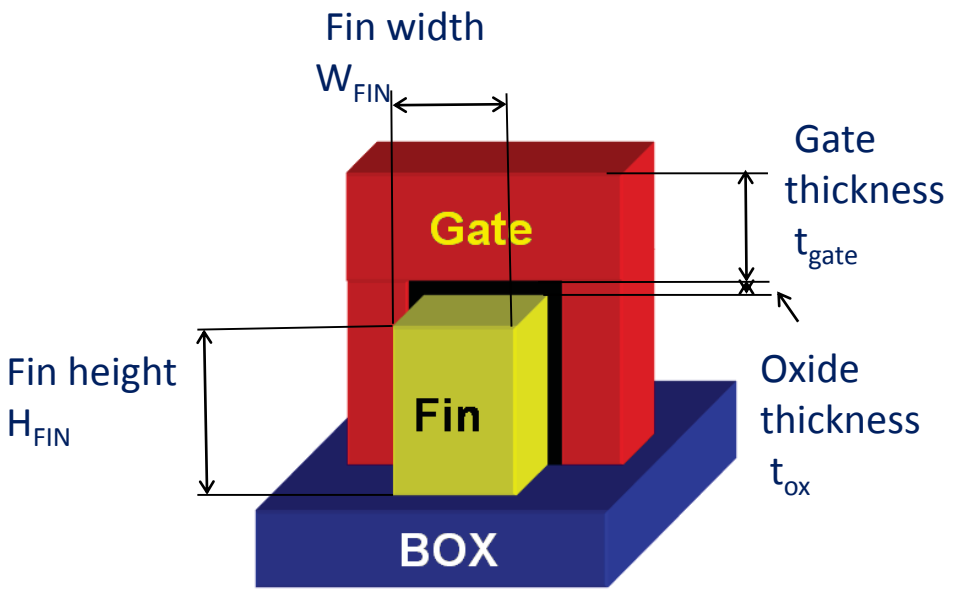
Conclusions

Introduction

Introduction

At present, the must advanced integrated circuits uses MOSFET structures know as FinFET, with is a typical 3D trigate structure with two lateral channels and one top channel.

SOI FinFET



Introduction

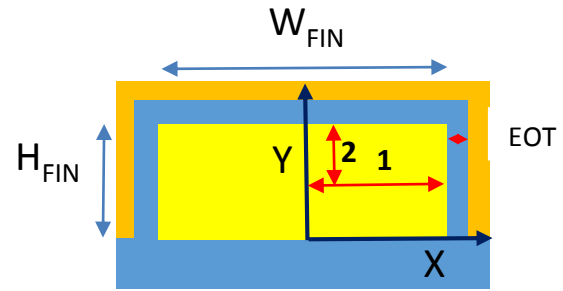
New types of FinFET transistors under development to be used in a new generation of Integrated Circuits, with very low dimensions:

1) NANOWIRE transistors:

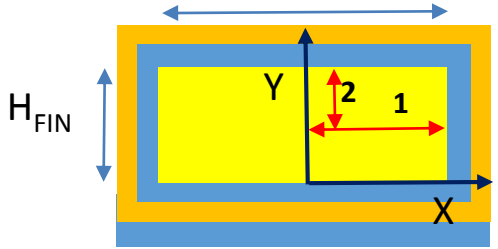
Trigate transistors, when W_{FIN} is equal or higher than H_{FIN}

2) NANOSHEET transistors:

When the channel surrounds the silicon Fin, also called Gate-All-Around (GAA) transistors.



NANOWIRE



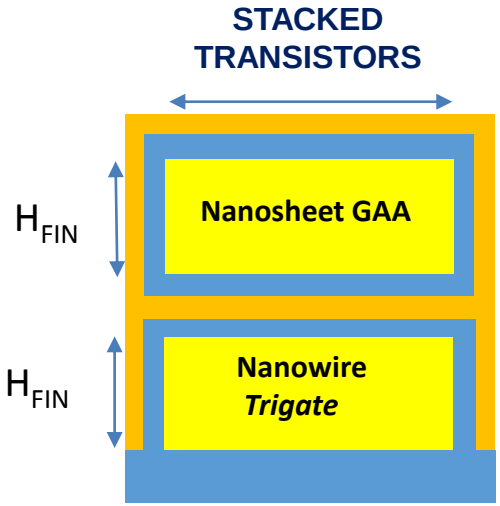
NANOSHEET

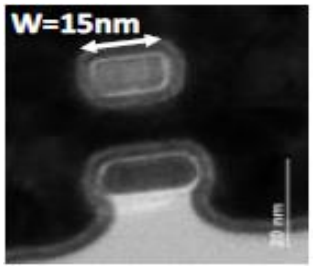
Introduction

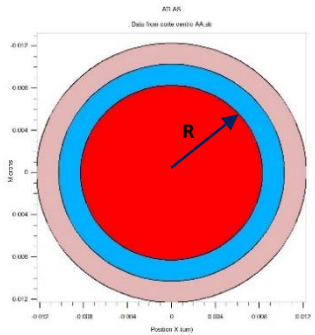
Above mentioned NANOWIRE and NANOSHEET transistors, located one over the other, are the most perspective structures for further IC development.

These structures are known as stacked transistors. The number of stacked transistors can be 2 or more.

Another transistor with a Gate-All-Around is the circular transistor.







CIRCULAR
NANOWIRE

Introduction

To design with these new types of MOSFETs, new compact models are required.

For nanowire transistors, several new models have been reported [1,2,3].

In this presentation we will show that our model ***SDDGM*** (***Symmetric Doped Double-Gate Model***) [4,5], already validated for Bulk and SOI types of FinFETs, can also be applied for modelling nanowires and nanosheets.

[1] Juan Pablo Duarte, et al. "A Universal Core Model for Multiple-Gate Field-Effect Transistors. Part I: Charge Model", IEEE Trans. On Electron Devices, 60, 2, 2013, 840-847

[2] Juan Pablo Duarte, et al. "A Universal Core Model for Multiple-Gate Field-Effect Transistors. Part II: Darin Current Model", IEEE Trans. On Electron Devices, 60, 2, 2013, 848-855.

[3] O. Rozeau, et al. "NSP: Physical compact model for stacked-planar and vertical Gate-All-Around MOSFETs" IEDM, 2016, 184-187

[4] A.Cerdeira, et al., "Modeling of potentials and threshold voltage for symmetric doped double-gate MOSFETs", *Solid-State Electronics*, vol. 52, pp. 830-837, 2008

[5] A.Cerdeira, et al., "Compact model for short channel symmetric doped double-gate MOSFETs", *Solid-State Electronics*, vol. 52, pp. 1064-1080, 2008

SDDGM and it application to nanowires and nanosheets

SDDGM model

Most important characteristics of the ***SDDGM*** model:

1. Includes the physical description of the device characteristics;

2. The currents and their derivatives are continuous in all the operating regions;

3. ***SDDGM*** model considers: H_{FIN} and W_{FIN} dimensions; doping concentration from undoped to highly doped; variable mobility; series resistances; short channel effects; temperature dependences; V_T roll-off; DIBL and channel length modulation.

SDDGM model

The drain current is expressed as a function of the normalized mobile charges at the source q_{ns} and drain q_{nd} as:

$$I_{DS} = \frac{2\frac{W}{L}C_{ox}\mu_s\left(\frac{k\,T}{q}\right)^2}{\left(1-\frac{\Delta L}{L}\right)} \frac{\frac{1}{2}\left(q_{ns}^2-q_{nd}^2\right)+\left[2(q_{ns}-q_{nd})-q_b ln\left(\frac{q_{ns}+q_b}{q_{nd}+q_b}\right)\right]^S}{\left[\sqrt{1+\left(\frac{\mu_s V_{Def}}{v_{sat}L}\right)^2}+2\frac{W}{L}C_{ox}\mu_s\ R\ \left(V_{GS}-V_T-\left(\frac{1}{2}+\frac{C_S}{C_S+C_{ox}}\right)V_{Def}\right)\right]}$$

$$\mu_s = \frac{\mu_o}{1+\left(\frac{\bar{E}}{E1}\right)^{P1}+\left(\frac{\bar{E}}{E20\left(1-E2V\ V_{Def}\right)}\right)^{P2}}$$

This model has only *12 model parameters.*

SDDGM model

Technological parameters, 8:

- N_a – doping concentration
- ϕ_{met} – metal workfunction
- EOT – equivalent oxide thickness
- Nss – interface charge density
- W_{FIN} – Fin width
- H_{FIN} – Fin height
- NU – number of parallel fins
- W – total transistor width, equal to the sum of all channel width

SDDGM model

Model parameters, 12:

- Mobility parameters (6) - μ_0, E1, E20, E2V, P1, P2
- Saturation velocity - v_{sat}
- Saturation voltage factor - τ
- Factor of conductance in saturation - λ
- Subthreshold slope - S
- DIBL factor - η
- Total series resistance - R

Application to nanowires and nanosheets

- In these transistors, the use of the SDDGM current expressions for the lateral, top and bottom surfaces is not trivial and must be demonstrated.
- $\mu_{TOP\ (or\ bottom)}$ and $\mu_{LATERAL}$ are different --> μ_{MED} a medium value is used.
- $I_{TOTAL} = I_{TOP} + I_{LATERAL} + I_{BOTTOM}$
- Doping concentration is equal to 10^{15} cm^{-3} --> No corner effects
- If dimensions are higher that 9 nm, the quantum effects can be neglected.

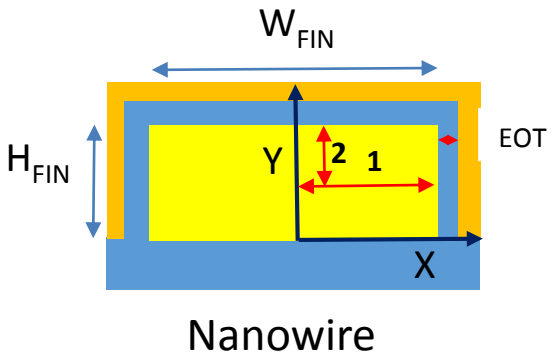
Application to nanowires and nanosheets

- Our previous work suggests that, if the total current in these transistors can be considered as the superposition of the current along the channel at the top, laterals and bottom interfaces, ***that is, as the current along the perimeter of the transistor,*** the model could also work for these devices.
- In order to prove this assumption, nanowire and nanosheet transistors were simulated with: H_{FIN}= 10 nm, W_{FIN}= 10 nm, N_a= 10^{15} cm^{-3} , EOT= 2 nm and V_G=V_D=1V.

We analyzed: The distribution of the electron concentration; current density and the electric field along cuts 1 and 2

CUT 1 – lateral surface to center

CUT 2 – top surface to center

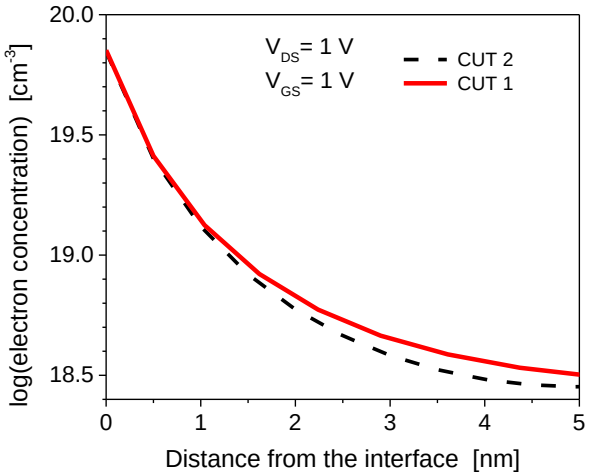


Nanowire

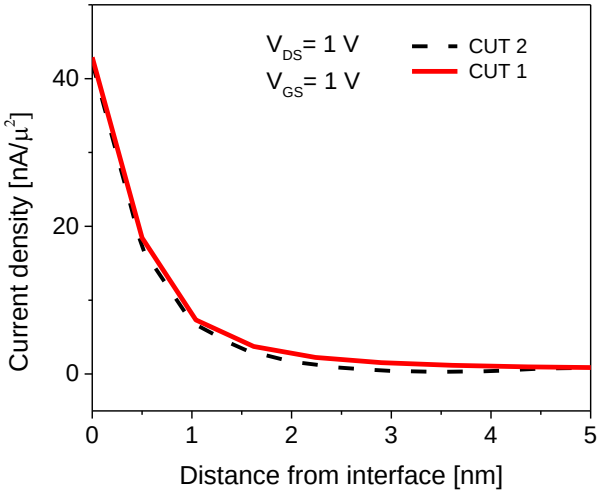
Application to nanowires and nanosheets

Simulated parameter distributions from top and lateral surfaces to center.

Electron concentration



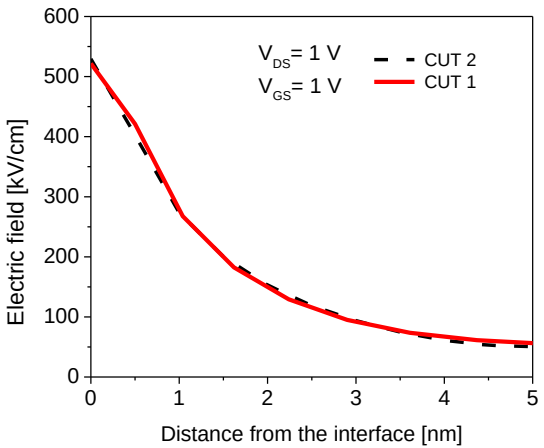
Current density



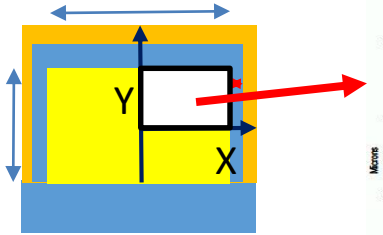
Application to nanowires and nanosheets

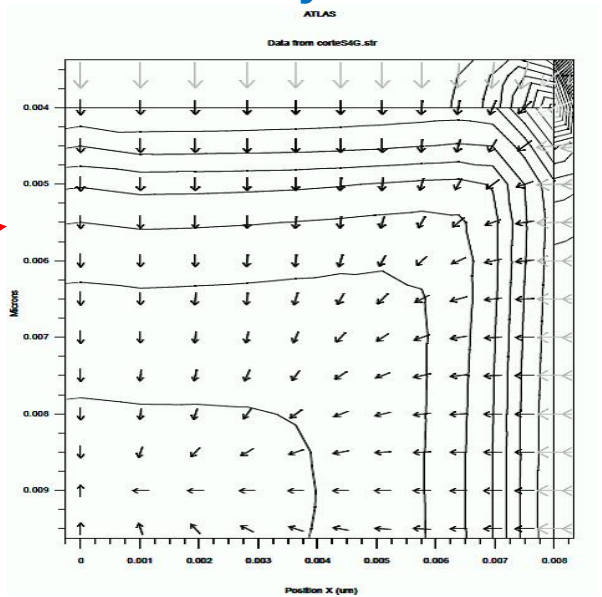
Simulated parameter distributions from top and lateral surfaces to center.

Electric field



Electric field inside the first quarter of the Si layer





Results of the simulations

- The distribution of electron concentration, current density and electric field, from the top and lateral interfaces to the center of the Si wire (cuts 1 and 2), are practically the same. Analyzed magnitudes change from the surface in 2-3 nm, that is at the surfaces.

- The distribution of the electric field inside the device is continuous, without corner effects.

Consequently

1) The drain current flows along the surface (channel) in the whole perimeter of the active channel;
2) SDDGM can be used for these devices, considering that the total channel width of the device, is equal to the perimeter of the transistor channels.

Results of the simulations

For modelling nanowires and nanosheets using the SDDGM model, the total channel width (*channel perimeter*) W_{tot} must be equal to:

For nanowires trigate -> $W_{tot} = W_{FIN} + 2\,H_{FIN}$

For nanosheet GAA -> $W_{tot} = 2\,W_{FIN} + 2\,H_{FIN}$

For circular GAA -> $W_{tot} = 2\,\pi\,R$ (R- radius)

For stacked transistors -> W_{tot}= Total perimeter of all stacked transistor channels [trigate and GAA]

The channel width W defined in the model is equal to $\boldsymbol{W_{mod} = W_{tot}/2}$

Model validation

Experimental transistors for validation

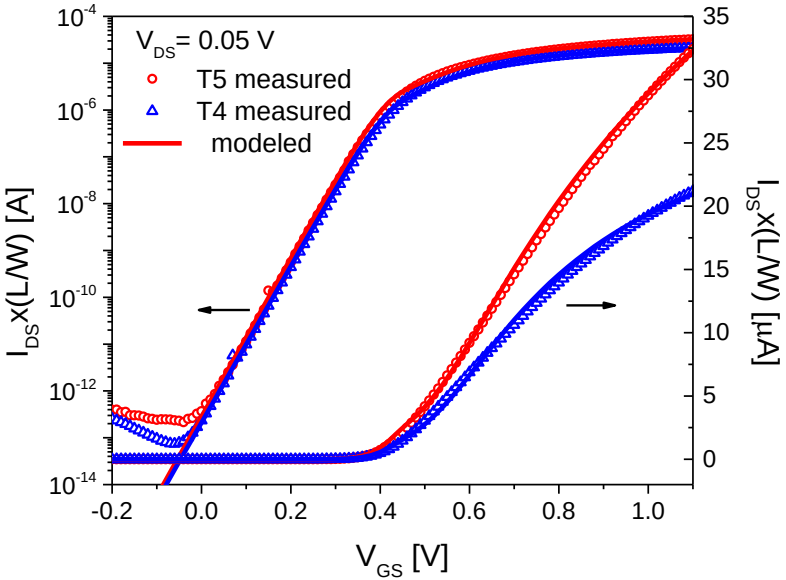
GROUP 1 – 7 EXPERIMENTAL TRANSISTORS

Symbol	Technological parameters	T1 NW	T2 NW	T3 NW	T4 NW	T5 NW	T6 NW	T7 NW+NS
L [nm]	Channel length	25	40	40	100	200	200	100
H_{FIN} [nm]	FIN height	10	10	10	10	10	10	9
W_{FIN} [nm]	FIN width	15	15	20	20	15	45	10
NU	Number of parallel FINS	1	10	10	10	1	1	1
W [nm]	Total channel width	35	350	400	400	35	65	66= 28+38

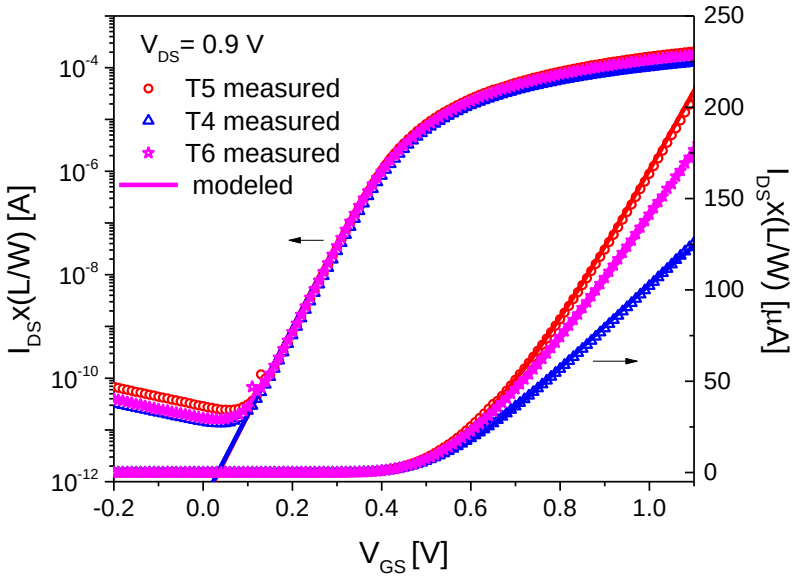
Experimental transistors

T4 T5 T6 **L≥ 100 nm**

Linear transfer characteristics



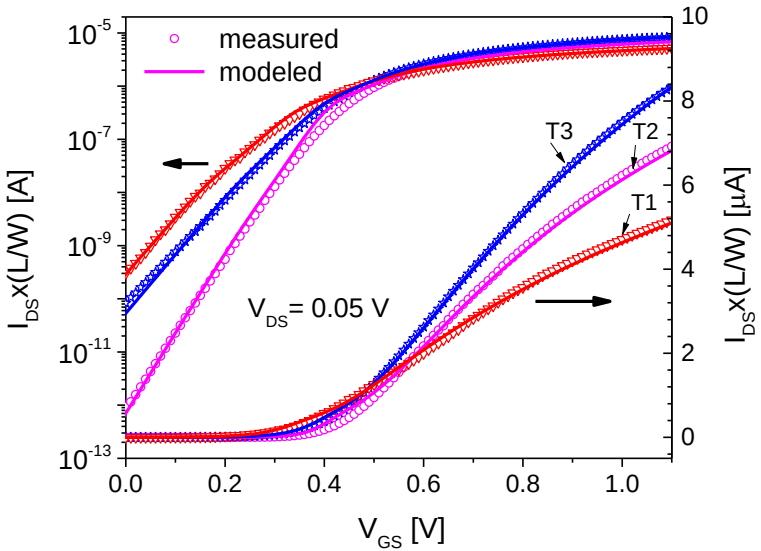
Saturation transfer characteristics



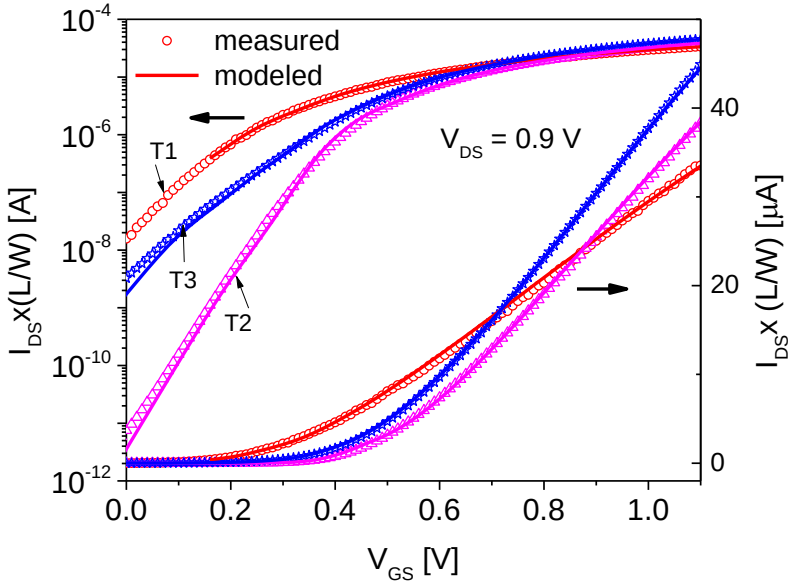
Experimental transistors

T1 T2 T3 **L = 25 and 40 nm**

Linear transfer characteristics



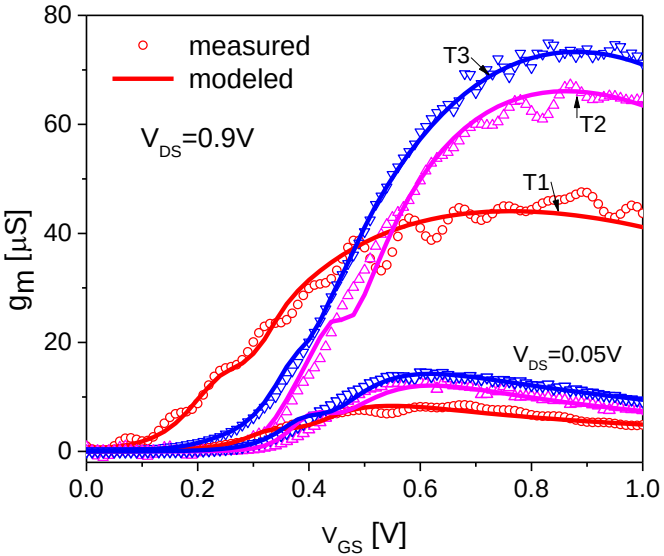
Saturation transfer characteristics



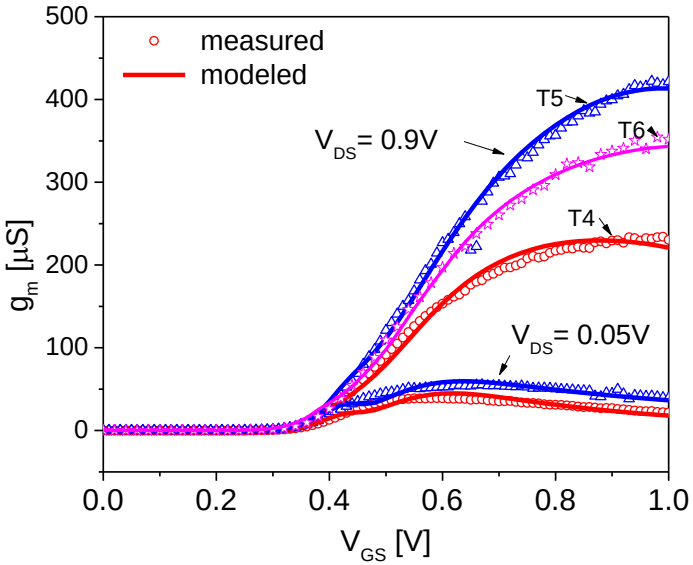
Experimental transistors

Transconductance in saturation

T1 T2 T3



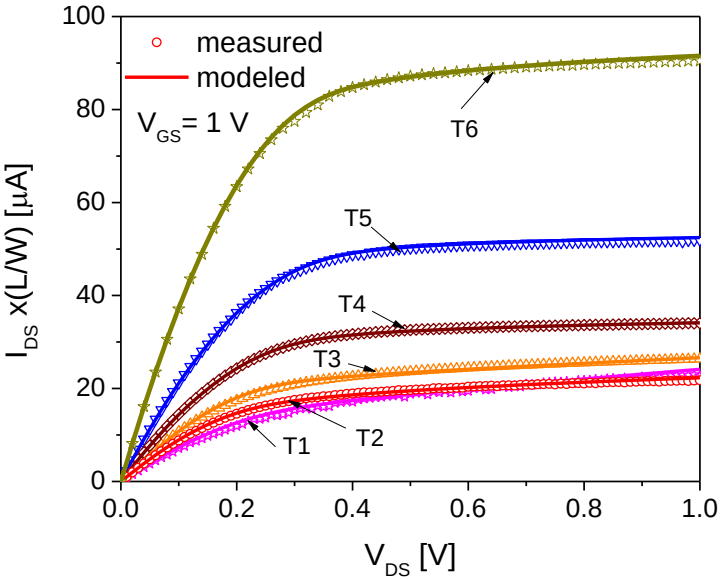
T4 T5 T6



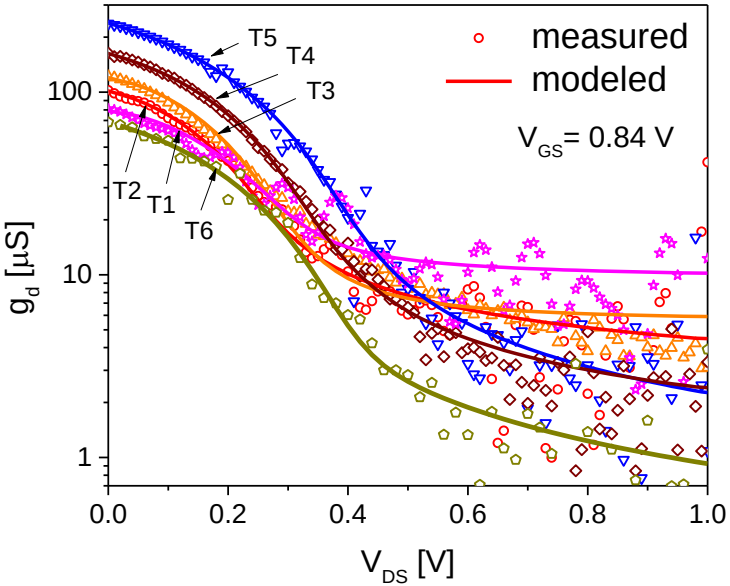
Experimental transistors

T1 T2 T3 T4 T5 T6

Output characteristics



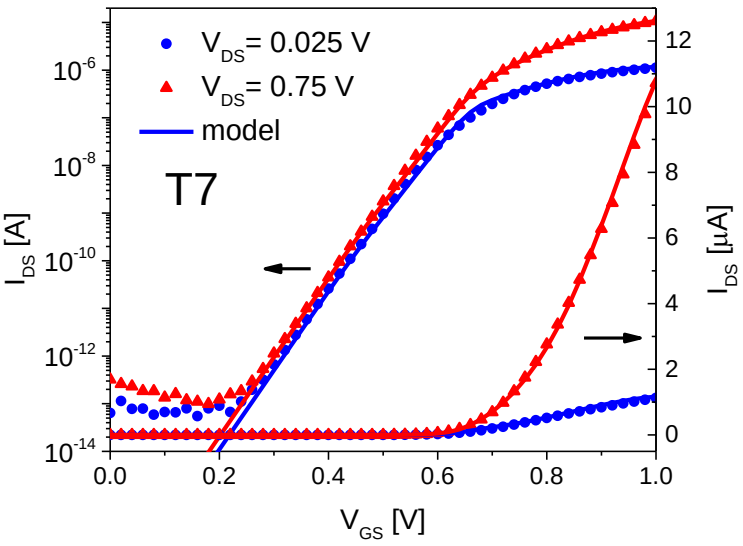
Output conductance



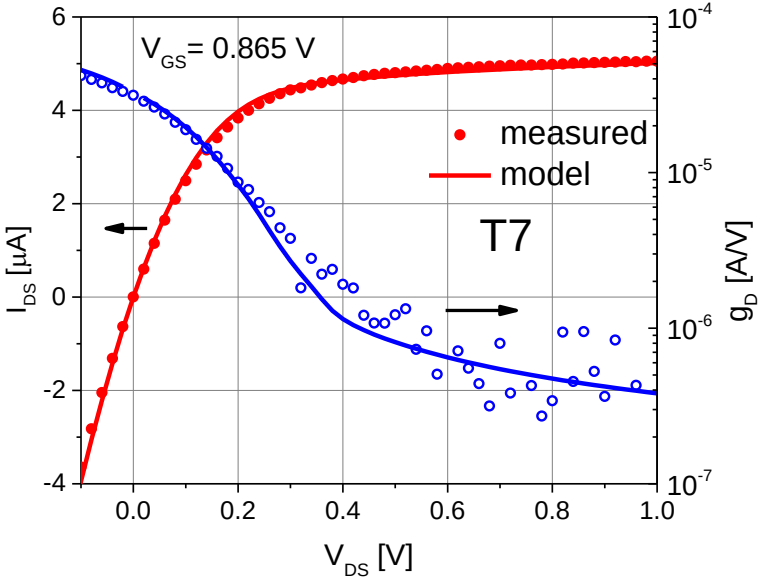
Experimental transistors

T7 - Stacked transistors - NW + NS

Transfer characteristics



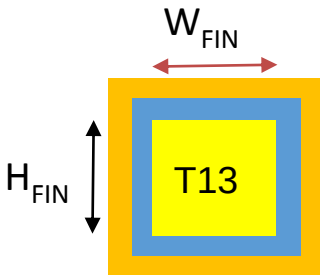
Output and conductance characteristics



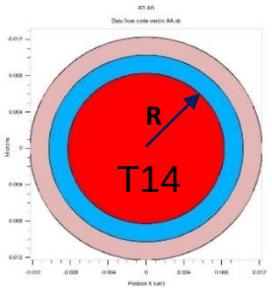
Simulated transistors for model validation

In order to validate the model with different dimensions, the following transistors were simulated and modelled:

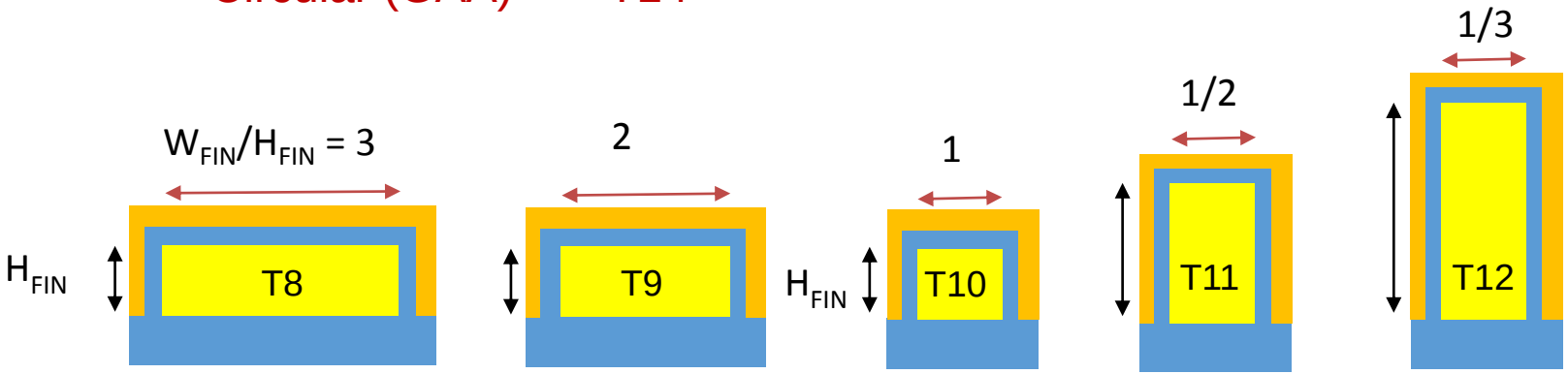
Nanowires	T8 – T12
Nanosheet (GAA)	T13
Circular (GAA)	T14



GAA



circular



Simulated transistors

GROUP 2 – 7 SIMULATED TRANSISTORS

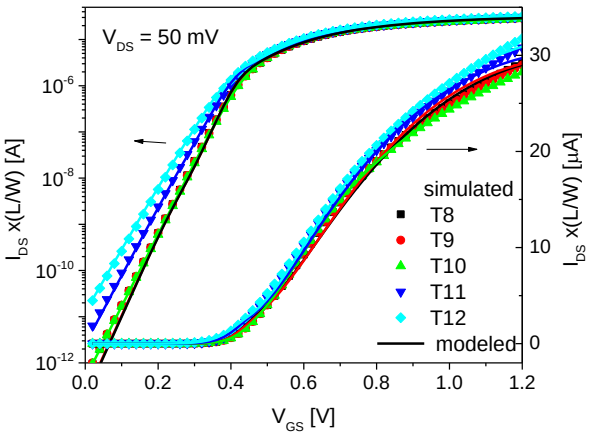
Symbol	Technological parameters	T8 NW	T9 NW	T10 NW	T11 NW	T12 NW	T13 NS-GAA	T14 Circular GAA
L [nm]	Channel length	50	50	50	50	50	50	50
H_{FIN} [nm]	FIN height	30	20	10	10	10	10	20 equiv.
W_{FIN} [nm]	FIN width	10	10	10	20	30	10	12.68 equiv.
W [nm]	Total channel width	70	50	30	40	50	40	40

T13 and T14 have the same perimeter = 40 nm

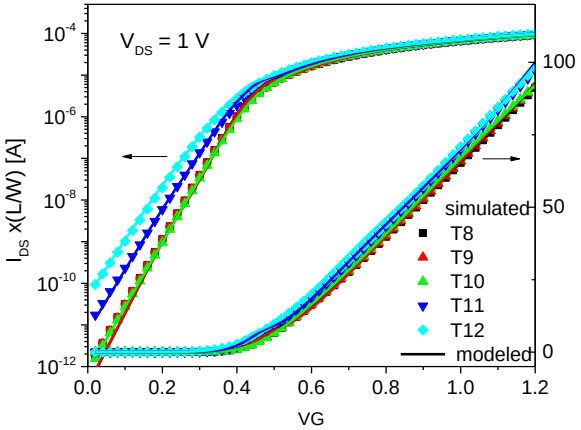
Simulated transistors

T8 – T12 NW **L = 50 nm**

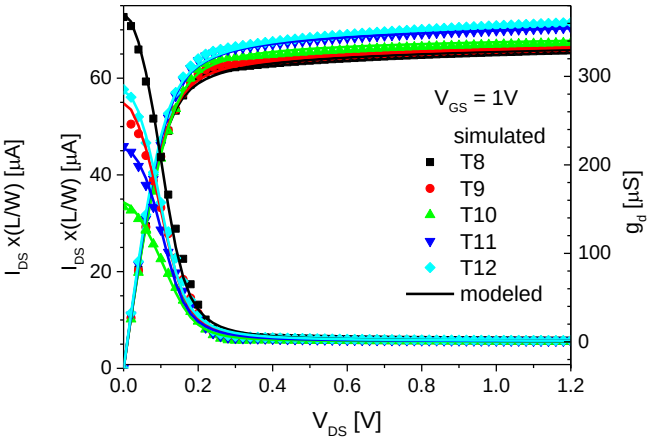
Linear transfer



Saturation transfer



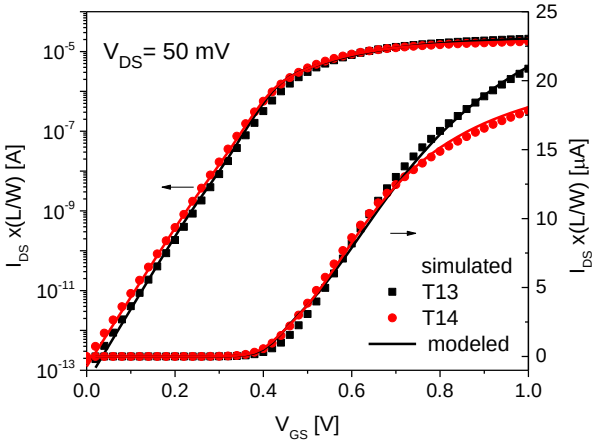
Output



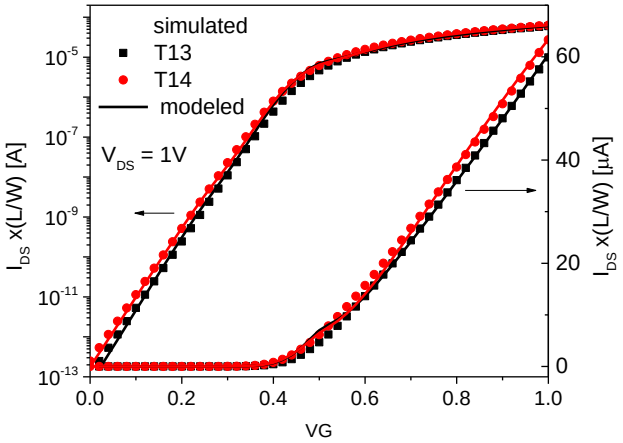
Simulated transistors

T13 – T14 GAA L = 50 nm

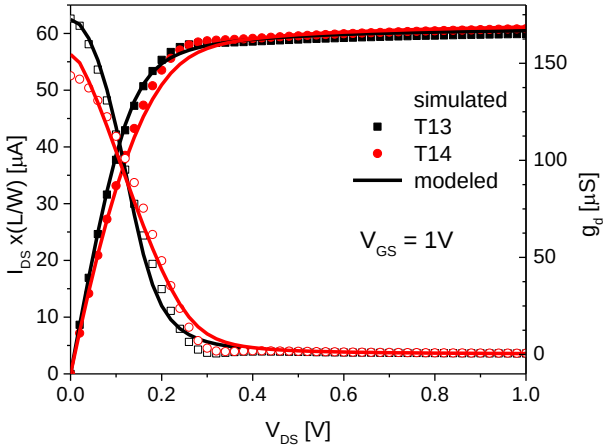
Linear transfer



Saturation transfer



Output



Conclusions

Conclusions

- It was shown that the distribution of electron concentration, current density and electric field, from the top and lateral interfaces to the center of the Si wire in **nanowire** or **nanosheet** transistors, are practically the same.

- The variation of these magnitudes are concentrated in less than 3 nm from the Si wire surface.

- For this reason, it is possible to consider that the total channel current is a superposition of the current along the lateral, top and bottom channels, considering an average value of mobility.

Conclusions

- For **nanowires** and **nanosheets** transistors, it can be considered that the effective channel width is equal to the perimeter of the transistor channels.

- The above characteristic allows to extend the use of the *SDDGM* model, not only to double-gate and trigate transistors, but also to **nanowires** and **nanosheets** multigate MOSFETs, with no need to include new parameters.

- The model is described in Verilog-A, and was validated with experimental and simulated devices, obtaining very good agreement.

Thanks for the attention

Technological parameters and extracted model parameters of these 14 transistors

Calculated threshold voltage V_T [V]

T1	T2	T3	T4	T5	T6	T7
0.36	0.42	0.42	0.43	0.42	0.43	0.66
T8	**T9**	**T10**	**T11**	**T12**	**T13**	**T14**
0.43	0.43	0.43	0.43	0.43	0.44	0.47

Model parameters extracted for experimental transistors

Symbol	Model parameters	T1	T2	T3	T4	T5	T6	T7
E1 [V/cm]	Mobility parameter	847	193	508	590	1.51×10^4	1.58×10^4	80
P1	Mobility parameter	0.33	0.21	0.24	0.169	0.198	0.292	0.215
E2 $\times 10^5$ [V/cm]	Mobility parameter	2.92	2.81	6.18	5.53	8.27	8.42	4.5
E2V [1/V]	Mobility parameter	1.06	1.06	1.16	0.8	0.72	0.95	0
P2	Mobility parameter	1	1	1.18	1.34	1.13	1	2
$v_{sat} \times 10^7$ [cm/s]	Saturation velocity	1.93	1.85	2.03	1.62	1.52	36	3.3
τ	Saturation voltage parameter	1.05	0.96	1.03	1.12	1.26	0.61	1.1
λ [1/V]	Factor of conductance in saturation	1.49	0.77	0.21	0.25	0.27	0.29	0.35
S [mV/dec]	Subthreshold slope parameter	0.95	1.03	0.89	1	1	1.03	0.98
η	DIBL factor	4.95	1.04	2.55	1	1	0.56	0.641
R [Ω]	Total series resistance	0	0	0	0	0	11	1361

Model parameters extracted for simulated transistors

Symbol	Model parameters	T8	T9	T10	T11	T12	T13	T14
E1 x10^7 [V/cm]	Mobility parameter	19.1	5.43	15	4.28	8	30	10
P1	Mobility parameter	0.17	0.178	0.18	0.658	0.93	0.2	1.26
E2 x10^5 [V/cm]	Mobility parameter	11.9	10.5	8	12.18	13	9	2
E2V [1/V]	Mobility parameter	0.243	0.725	1.5	0	0	0	1.065
P2	Mobility parameter	2.98	2.3	1.44	2.789	2.9	1.7	1
v_{sat} x10^7 [cm/s]	Saturation velocity	2.56	2.35	2.2	3.9	3.2	2.52	1.8
τ	Saturation voltage parameter	0.94	0.917	1	0.758	0.92	0.97	1.22
λ [1/V]	Factor of conductance in saturation	0.13	0.12	0.1	0.15	0.35	0.08	0.13
S [mV/dec]	Subthreshold slope parameter	1.05	1.04	1.03	1.04	1.26	1.1	1.07
η	DIBL factor	0.27	0.234	0.117	0.169	0.077	-0.29	-0.26
R [Ω]	Total series resistance	957	1090	1500	1865	1472	2100	100