

## Capacitance modelling of a transistor for RF Power Amplifiers in 5G applications.

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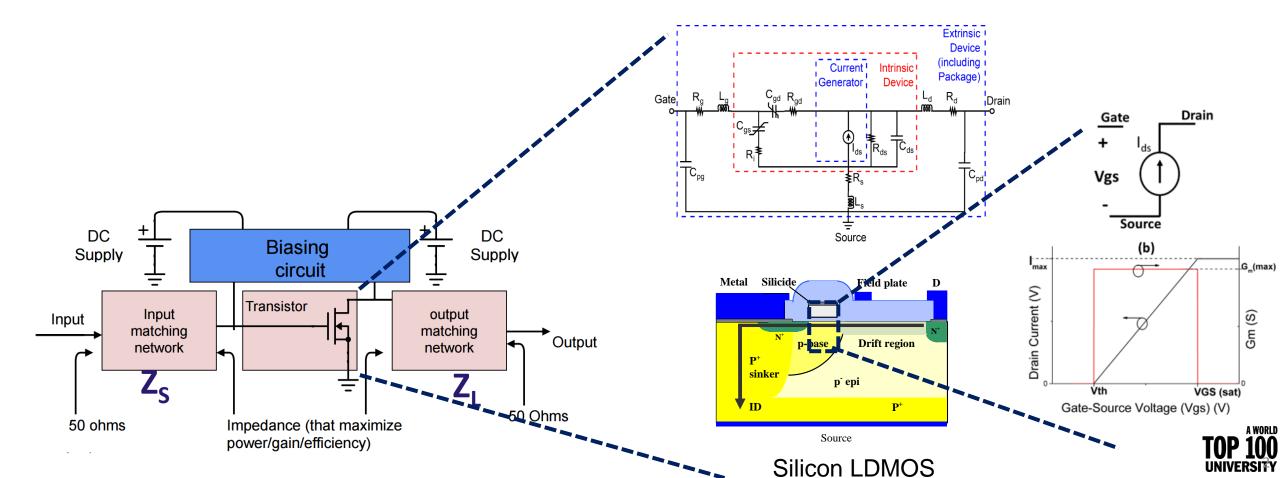
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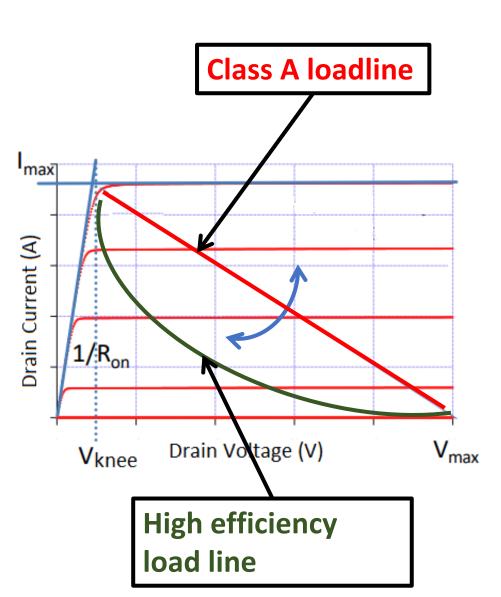


## The RFPA design process

- Identifying the optimal source ( $Z_{\rm S}$ ) and load ( $Z_{\rm L}$ ) impedances at fundamental and harmonic frequencies
- Requires an accurate model of the transistor, consisting of the intrinsic device corresponding to the gated channel, (~linear current generator) and extrinsic parameters







### Motivation

- High efficiency and linear amplifier are required to meet the stringent requirements of fifth generation mobile networks.
  - High efficiency modes such as continuum modes that rely on the harmonic manipulation
- The accuracy of circuit design relies heavily on the accuracy of the transistor model
  - requires accurate modelling of capacitances especially in the knee region.
  - for accurate distortion simulation up to N<sup>th</sup>-order requires models that have I-V and Q-V curves accurate up to Nth-order derivatives.
  - component-wise information about the dominant distortion sources helps to employ suppression techniques.

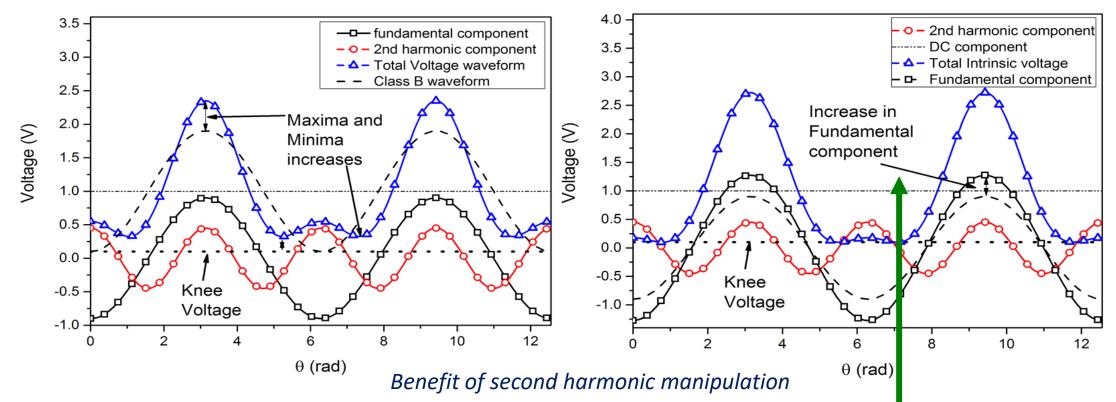




# High efficiency modes



## Principle of harmonic manipulation



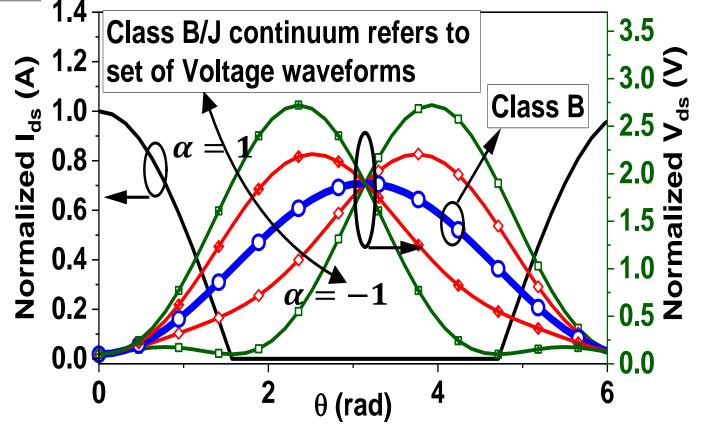
- The magnitude of the fundamental component increases by addition of the second harmonic component with an *appropriate* phase to the fundamental.
- This increase in voltage is often referred as "voltage gain" ( $\delta_{v}$ ).



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- Maximum of Voltage shifted to the left or right (Class J/J\*)
  - All these waveform result in efficiency 78.5 % (same as Class B)
- Result in an increase in design space

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# Impact of the Non-linear Caps on continuum modes

0.4  $I_{Cad}(\overline{\alpha=-1})$  $\alpha = -0.5$  $(\alpha = 0)$ 1.5  $C_{ad}(\alpha=1)$ <sub>Cad</sub>(α=0.5) 0.3 0.2 I<sub>cgd</sub> (A) l<sub>di(r)</sub> (Å) increasing 0.1 0.0 -0.1 0.0 -0.2 100p 200p 300p 400p 500p 600p 700p 0 Time (s) <del>---</del> α=-1 0.6 -<del>-</del> α=-0.5 **-** α=0 0.4 - α=0.5 **(**) 0.2 ,0.0 ,0.0 ,0.2 - α=1 increasing α -0.4 -0.6-100p 200p 300p 400p 500p 600p 700p 0 Time (s)

N. Poluri, MM De Souza, TCAS II, vol. 65, Issue 9, 2018

- Due to the variation of the phase of voltage in continuum mode, the phase of the current through Cgd changes.
  - Phase of Icgd varies relative the current from current generator (gm).
  - For some cases of α (such as -1), lcgd is out of phase with the current from current generator.
- This phase variation of lcgd result in an improvement/reduction fundamental component of the current.
  - Improves efficiency and P1dB over class B for some subset of  $\alpha$

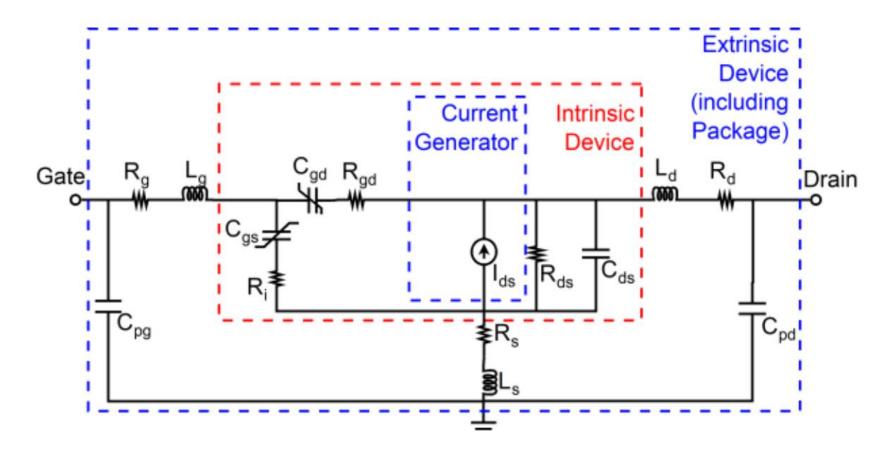




# Small Signal model



### Equivalent circuit model



- Extrinsic parasitics are extracted from cold-forward ( $V_{ds}=0 V, V_{gs}\approx 0$ ) and cold reverse conditions ( $V_{ds}=0 V, V_{gs}<V_{th}$ )
- Intrinsic parameters are extracted for each bias point

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### **Extraction of extrinsic capacitances**

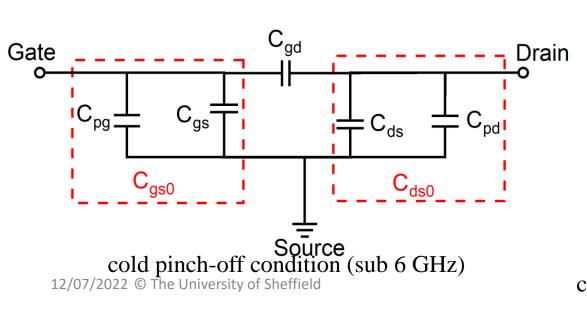
- $C_{gd}$  and branch capacitors ( $C_{gs0}$  and  $C_{ds0}$ )
  - can be extracted from the slope of the Y parameters of the device with frequency,  $\omega$ .

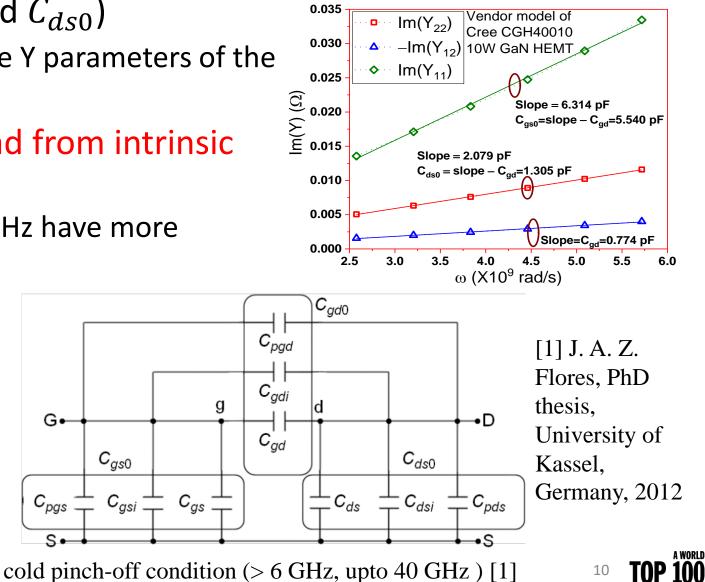
G•

C<sub>pgs</sub>

S.

- Need more relations to separate pad from intrinsic caps (Cgs and Cds).
  - Equivalent circuits for frequency >6 GHz have more capacitances.





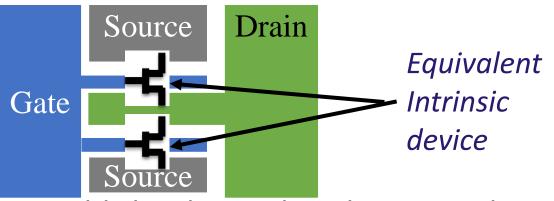
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### Extraction of pad capacitances

#### If the device structure is known

• 3-D electromagnetic (EM) simulations of the metallization layer [1].



- Establish relationships between the extrinsic and/or intrinsic capacitances by
  - Theoretical modelling of the capacitance (C) by assuming  $C \propto pad area$ . [2]

If device structure is unknown

- Optimization to minimize the modelling error
  - Guess values of pad capacitances [3] or
  - The ratio of pad/device capacitances can be optimized (referred as Technology-related Empirical Capacitance Ratios (TECR) [2])

[1] Davide Resca et. Al. IEEE MTT, vol. 58, no. 4, 2010 [2] J. A. Z. Flores, PhD thesis, University of Kassel, Germany, 2012 [3] F. Lin and G. Kompa, IEEE MTT, vol. 42, no. 7, 1994





## Modified TECR algorithm

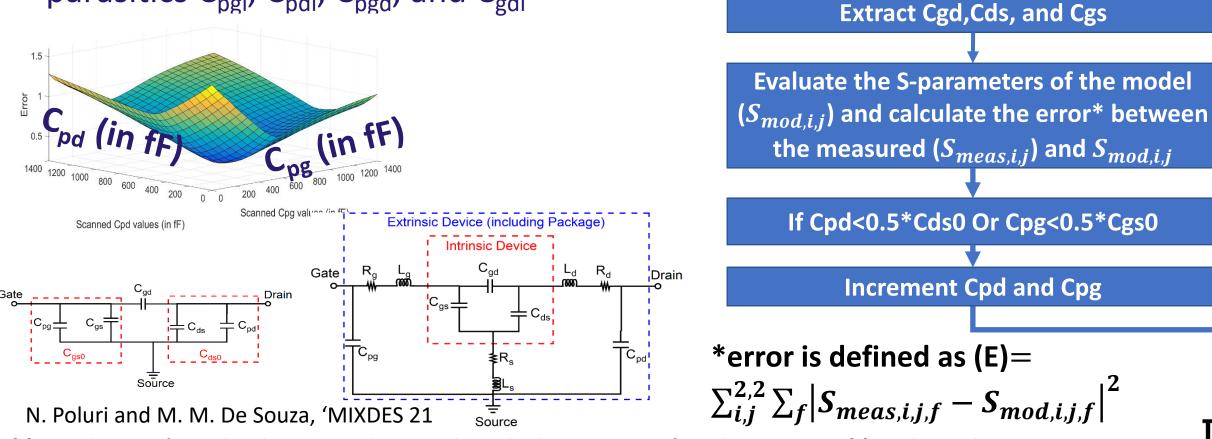
Cpd=0; Cpg=0

**De-embed Cpd and Cpg** 

Extract Rs, Rg, Ks, Ls, Ld, and Lg

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 Simplified version of TECR algorithm for extraction of C<sub>pd</sub> and C<sub>pg</sub> whereas the Original version includes additional parasitics C<sub>pgi</sub>, C<sub>pdi</sub>, C<sub>pgd</sub>, and C<sub>gdi</sub>

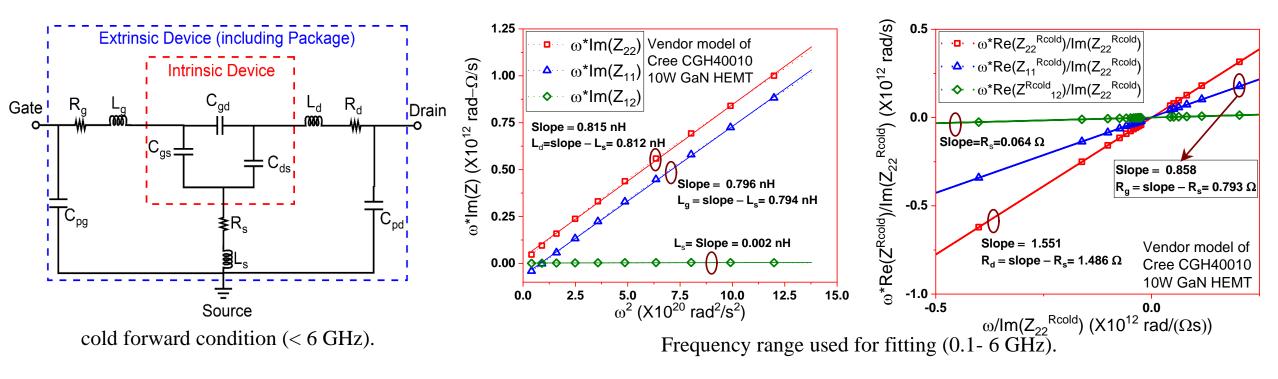


[1] Original version of TECR algorithm is proposed in J. A. Z. Flores, PhD thesis, University of Kassel, Germany, 2012 [2] N. Poluri et. Al., MIXDES, 2021



### Extraction of Extrinsic parameters

• Extrinsic resistances and inductances are extracted from cold forward condition (Vgs>Vth and Vds=0) [1].



[1] J. A. Z. Flores, PhD thesis, University of Kassel, Germany, 2012



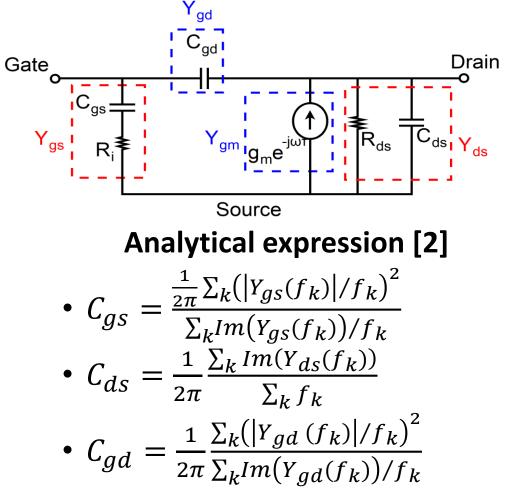


### Extraction of Intrinsic parameters

- De-embed extrinsic parameters.
- Related to Y parameters
- Analytical expressions are easier to program compared to curve fitting.

### **Relations for Curve/data fitting [1]**

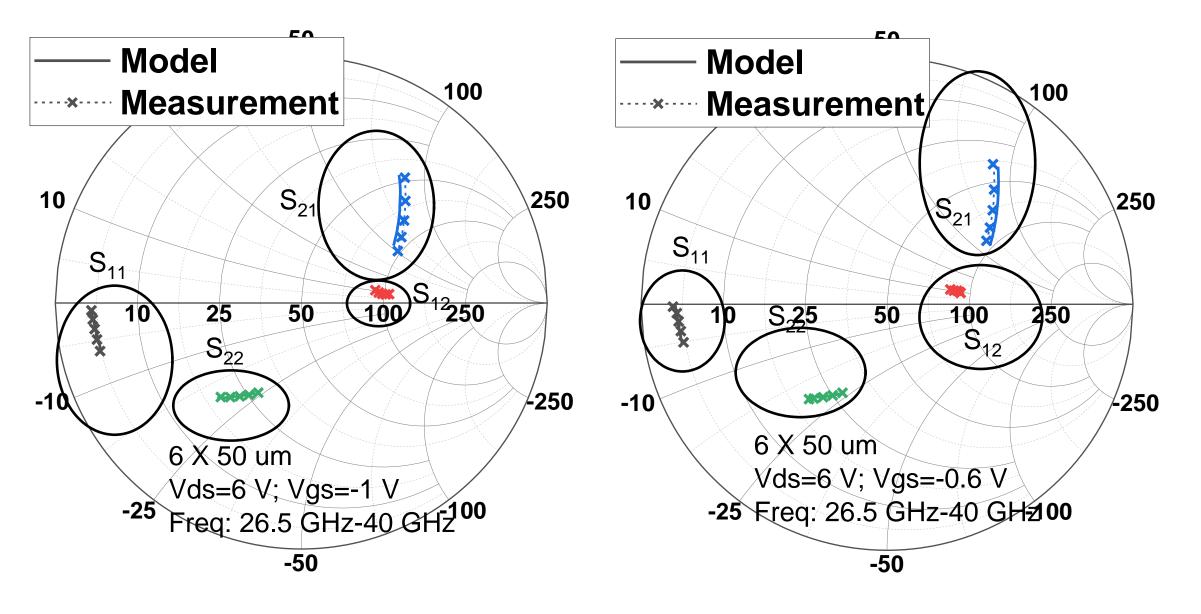
•  $\omega^2 C_{gd} = \omega |Y_{gd}|^2 / Im(Y_{gd});$ •  $\omega^2 C_{gs} = \omega |Y_{gs}|^2 / Im(Y_{gs});$ •  $\omega C_{ds} = Im(Y_{ds})$ 



[1] J. Lu, et. Al. *Solid. State. Electron.*, vol. 52, no. 1, pp. 115–120, 2008
[2] F. Lin and G. Kompa, IEEE MTT, vol. 42, no. 7, 1994



# Comparison of S-parameters (small signal model)





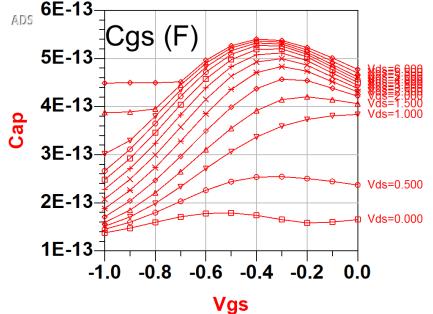


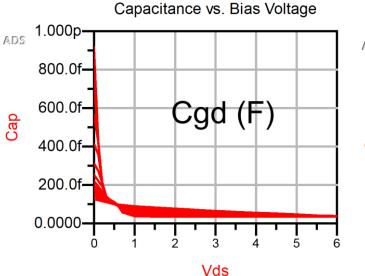
# Large signal model

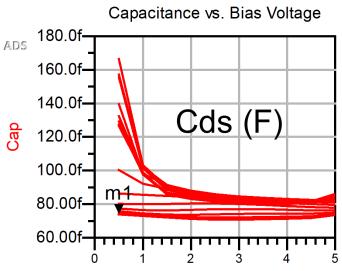




# Mapping voltages from the extrinsic to the intrinsic plane

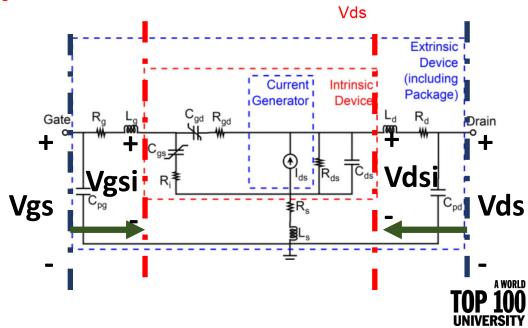






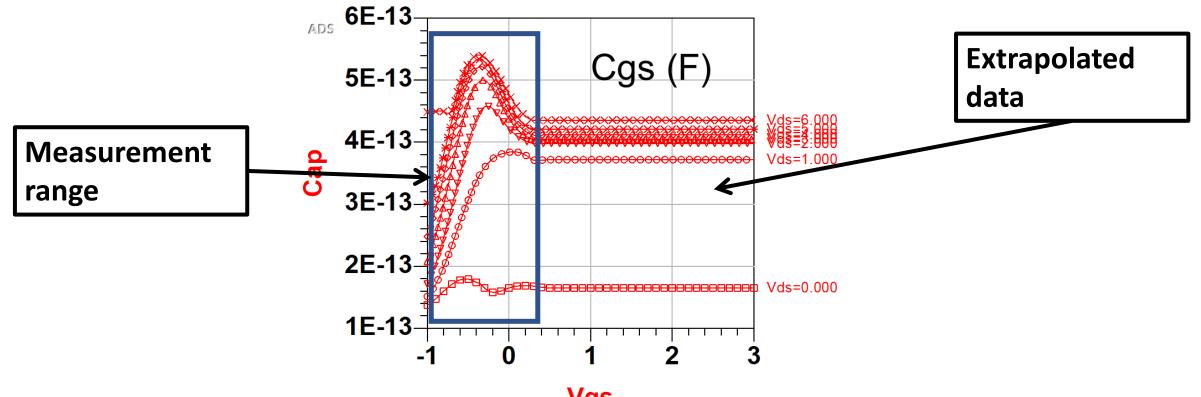
- Intrinsic capacitances obtained from extraction are a function of extrinsic voltages ( $V_{gs}$  and  $V_{ds}$ ).
- Intrinsic parasitics are "re-gridded" to intrinsic gate ( $V_{gsi}$ ) and drain ( $V_{dsi}$ ) voltages.

$$V_{dsi} = V_{ds} - (R_d + R_s)I_{ds} - R_sI_{gs}$$
  
 $V_{gsi} = V_{gs} - (R_g + R_s)I_{gs} - R_sI_{ds}$ 





### Extrapolation beyond measurement range



#### Vgs

- Device cannot be measured for all the gate and drain voltages because device might get damaged due to
  - device oscillations
  - thermal impact.





### Cgd and Cgs modelling [1]

### Division by charge

$$Q_g = Q_{gs} + Q_{gd}$$

• The reactive gate current  $(I_g)$  as

$$I_{g} = I_{s} + I_{d}$$

$$I_{s} = C_{gs} \frac{dV_{gsi}}{dt} + \frac{\partial Q_{gs}}{\partial V_{gdi}} \frac{dV_{gdi}}{dt}$$

$$I_{d} = \frac{\partial Q_{gd}}{\partial V_{gsi}} \frac{dV_{gsi}}{dt} + C_{gd} \frac{dV_{gdi}}{dt}$$

Where,  $\frac{\partial Q_{gd}}{\partial V_{gs}}$  and  $\frac{\partial Q_{gs}}{\partial V_{gd}}$  denote trans-capacitances

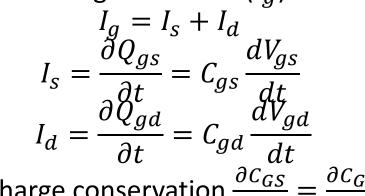
• The following is easy to implement in HB simulation

$$I_{s} = \frac{Q_{gs}(V_{gs} + dV_{gs}, V_{ds} + dV_{ds}) - Q_{gs}(V_{gs}, V_{ds})}{dt}$$

- Difficult to determine trans-caps.
- Could result in charge non-conservation  $\rightarrow$ periodic excitation that conserves  $Q_g$  could result in non periodic  $Q_{gs}$  and  $Q_{gd}$ .

### **Division by capacitance**

• The reactive gate current  $(I_{q})$  as

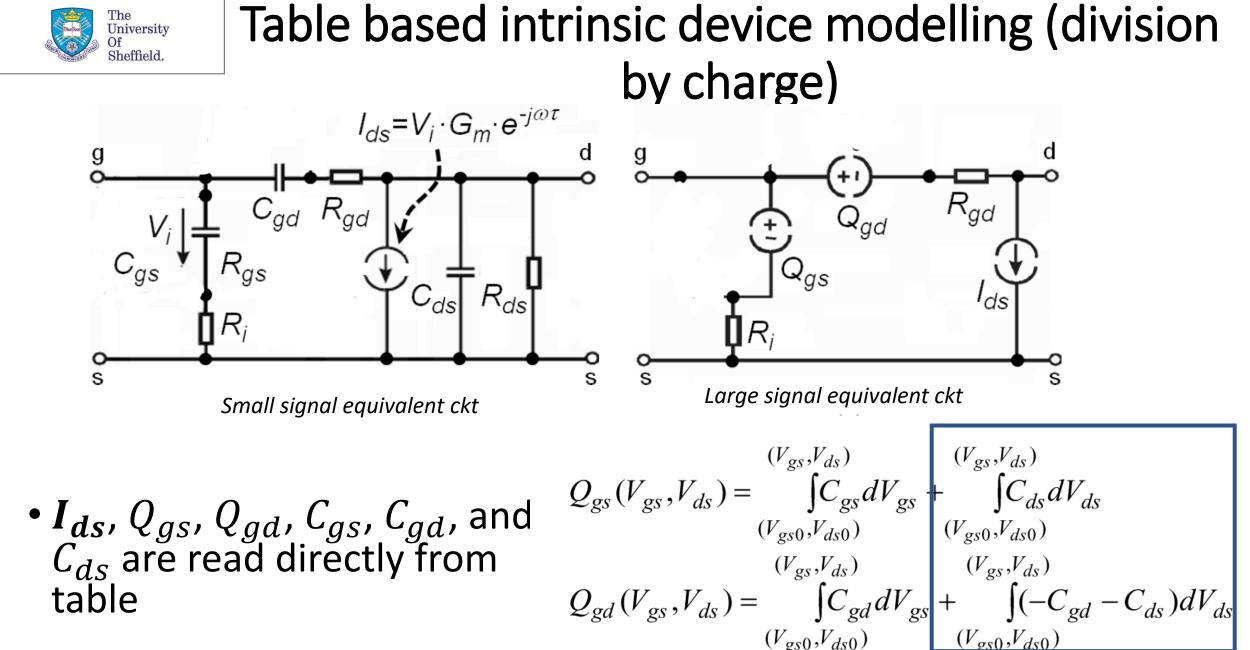


- For charge conservation  $\frac{\partial C_{GS}}{\partial V_{GD}} = \frac{\partial C_{GD}}{\partial V_{GS}}$
- Lack of trans capacitance simplifies modelling.
- Consistent with small signal model.

• Difficult to implement differential with only one variable in HB simulations  $I_{s} = \frac{Q_{gs}(V_{gs} + dV_{gs}, V_{ds}) - Q_{gs}(V_{gs}, V_{ds})}{dt}$ 

[1] S. Maas, Nonlinear Microwave and RF circuits, Artech House 2003 **TNP** 

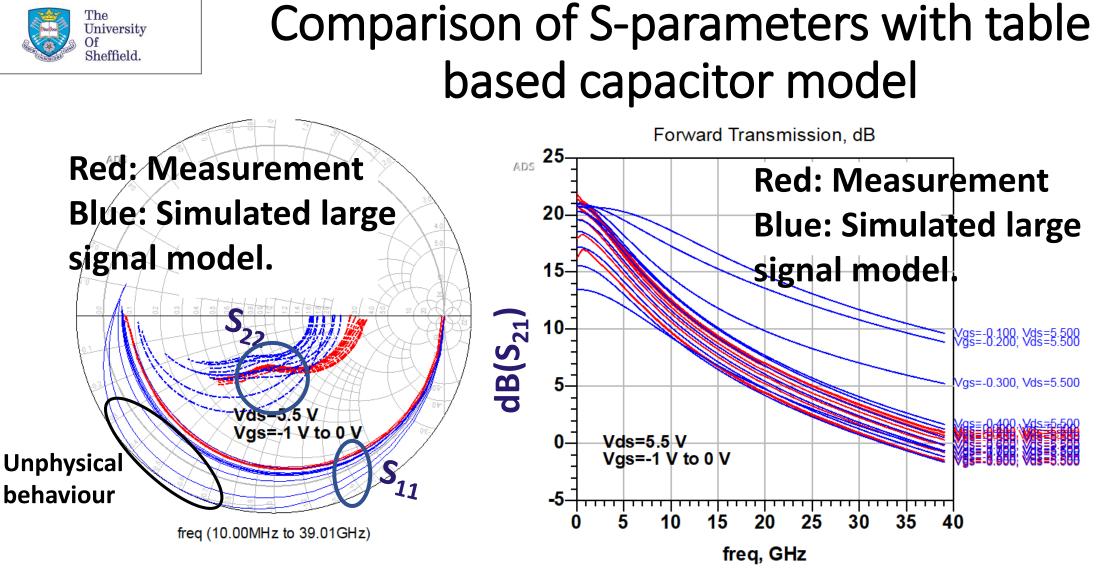
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Flores, PhD thesis, University of Kassel, Germany

Approximately models the trans capacitance





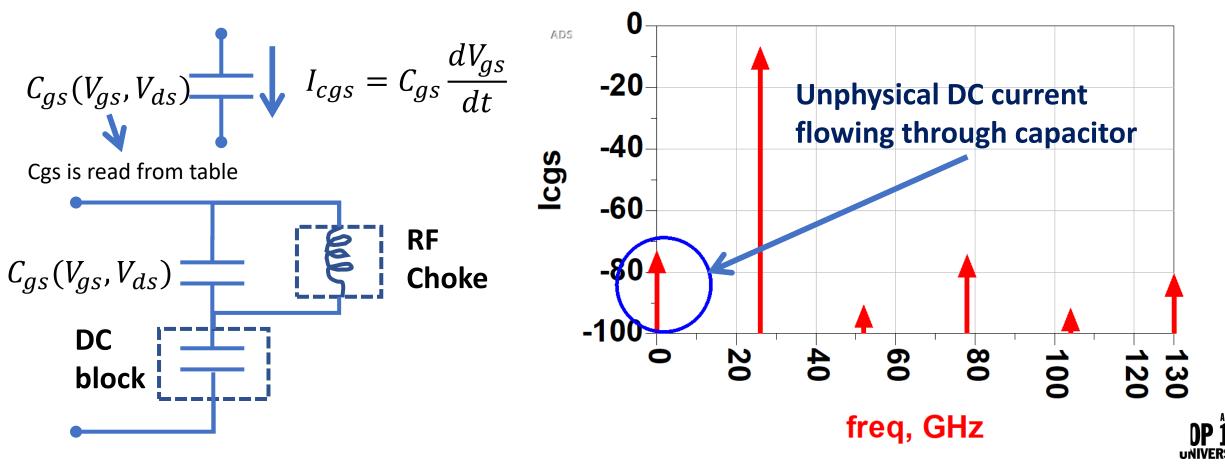
- Hard to debug as it is difficult to separate the impact of Qgs and Qgd
- We think the interpolating spline used to model the capacitor beyond its measured range causes oscillations between the data points, hence nonphysical fluctuations.





### Division by capacitance (issue with Cdv/dt)

- Implementation of a capacitor as  $C\left(\frac{dv}{dt}\right)$  results in unphysical DC current flowing through capacitor.
- A fix is to use a C block and RF choke to short the DC component → results in inaccurate harmonic

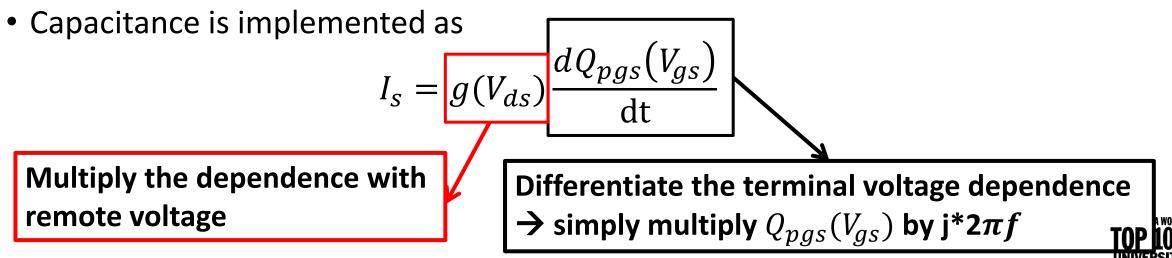




### Capacitance implementation in HB simulation

- How to implement of the differential with one variable in HB simulation?  $I_{s} = \frac{Q_{gs}(V_{gs} + dV_{gs}, V_{ds}) - Q_{gs}(V_{gs}, V_{ds})}{dt}$
- Capacitor is modelled as a product of functions of gate and drain voltage  $C_{\rm gs} \propto f(V_{gs})g(V_{ds})$
- Charge is calculated by integrating with terminal voltage

$$Q_{gs} = g(V_{ds}) \int f(V_{gs}) dV_{gs} = g(V_{ds}) Q_{pgs}(V_{gs})$$

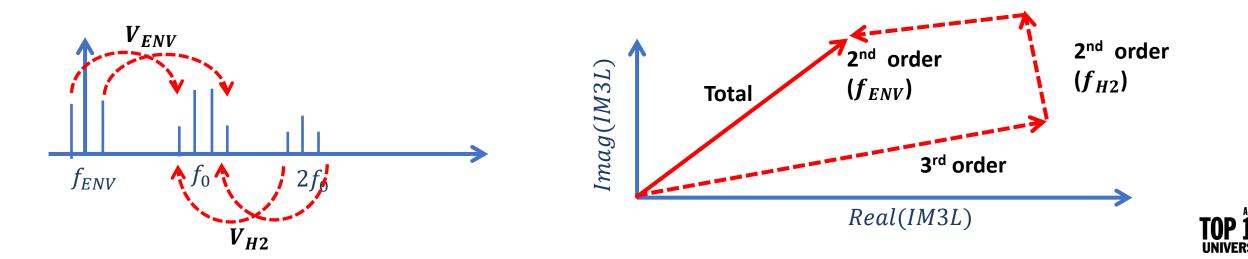




### Conventional Polynomial model (division by Capacitance)

 $\begin{aligned} C_{gs} &= C_{gs00} + C_{gs10} v_{gs} + C_{gs01} v_{ds} + C_{gs11} v_{gs} v_{ds} + \cdots \\ C_{gd} &= C_{gd00} + C_{gd10} v_{gs} + C_{gd01} v_{ds} + C_{gd11} v_{gs} v_{ds} + \cdots \end{aligned}$ 

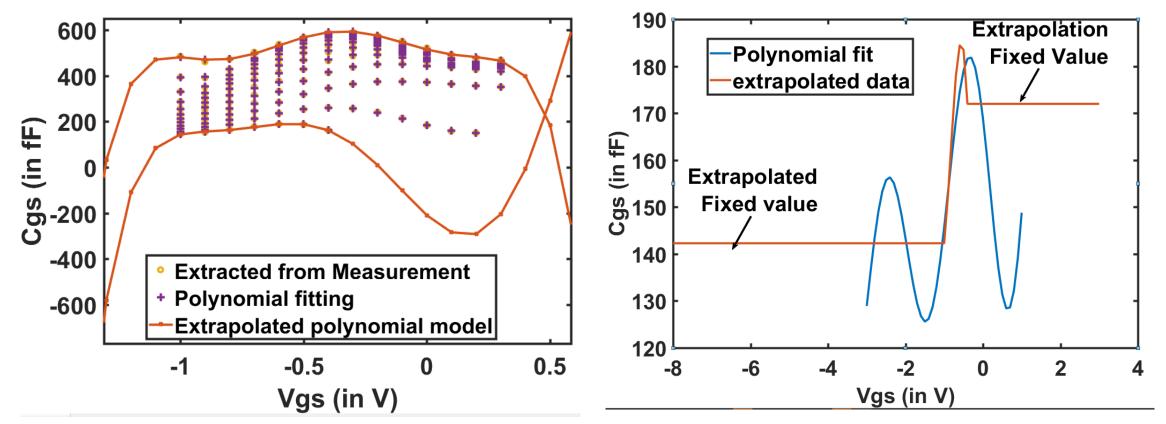
- Well-know numerical techniques are available and their derivatives are also devoid of discontinuities
- Suitable for Volterra analysis to understand multiple mixing mechanisms can also be recognized
  - which aids the design of harmonic terminal impedances.





### **Conventional Polynomial model**

- Outside the range of data used to generate the polynomial can result in undesirable behaviour.
- Small variation in the measured data due to noise may result in large changes in the polynomial coefficients → un-realisitic derivatives



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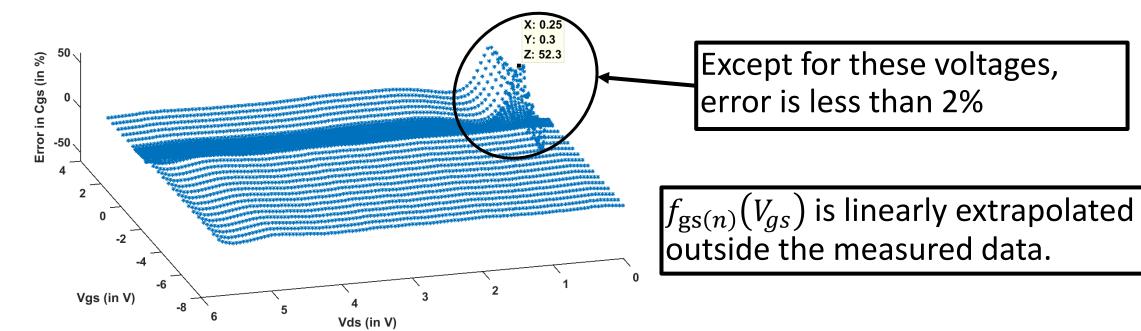
### UoS Capacitor Model (division by capacitance)

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- Capacitances are expressed as  $C_{gs}(V_{gs}, V_{ds}) = \sum_{n=0}^{N} f_{gs(n)}(V_{gs})g_{(n)}(V_{ds})$ and  $C_{gd}(V_{gs}, V_{gd}) = \sum_{n=0}^{N} -g_{gd(n)}(V_{gs})g_{(n)}(V_{gs} - V_{gd})$ • In our implementation,  $g_{(n)}(V_{ds}) = \begin{cases} (1 - V_{ds}/V_{dsq})^n & 0 < V_{ds} < V_{dsq} \\ 0 & V_{ds} > V_{dsq} \end{cases}$ 
  - $g_{(n)}(V_{ds})$  denoted the nth power of  $\hat{R}F$  component of the  $V_{ds}$ .

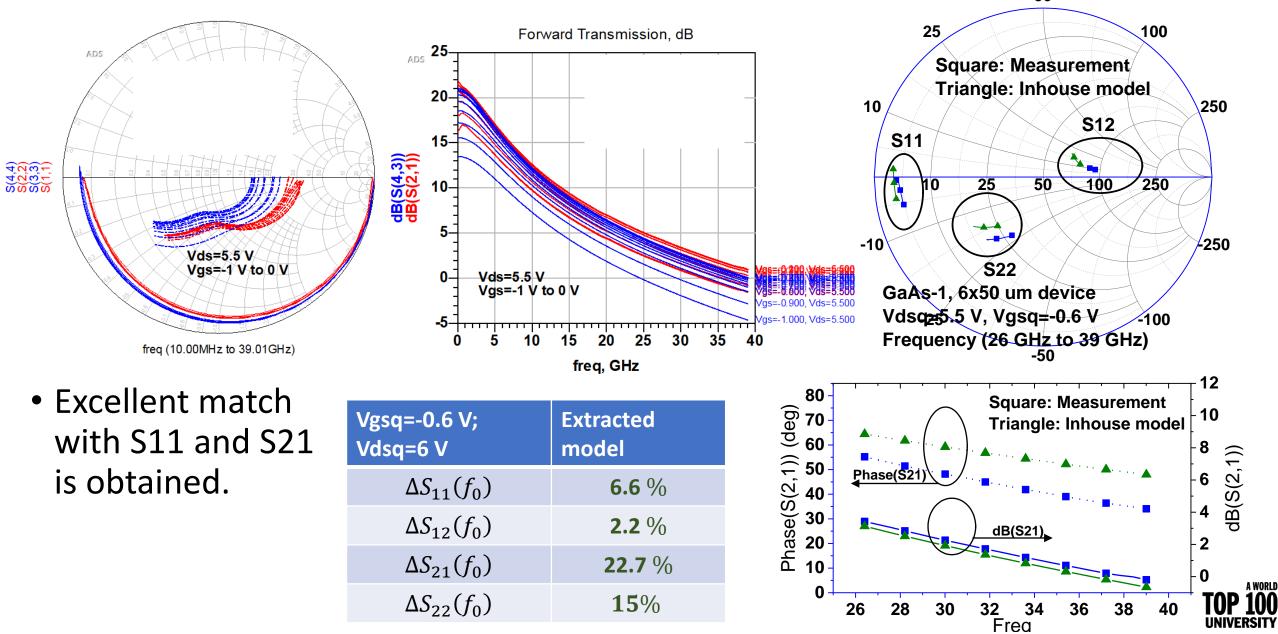
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•  $f_{gs(n)}(V_{gs})$  and  $g_{gd(n)}(V_{gs})$  is obtained from the curve fitting tool in matlab and read from a table in ADS.





### Accuracy of Large signal UoS Model





### Summary

- Each of the modelling techniques have deficiencies:
  - Table based Capacitor models
    - Easier to implement.
    - Accurately models within the measurement range.
    - However, interpolating spline can create oscillations between the data points and hence nonphysical fluctuation in the higher order derivatives.
  - Empirical model (The propose model)
    - Higher order derivatives are well defined.
    - Well defined beyond the measurement range.
    - Suitable for Volterra analysis.
    - less accurate than table based model.





# Thank you for your attention

