Ultra Low Power Dual-Gate 6T and 8T Stack Forced CNFET SRAM Cells

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Brief Outline

In this work two Carbon Nano Field effect transistors (CNFET) based SRAM cells are proposed to minimize the static power dissipation due to leakage.

One Cell has 6 dual gate CNFETs and the second cell has 8 transistors with stack forced technique.

The cells are designed with dual threshold voltages for N-type and P-type CNFETs by selecting dual chirality vectors of the carbon nano tubes.

We have analyzed the performance and the power dissipation of the cells through SPICE simulation at two different temperatures using the MOSFET like CNFET model from Stanford Nanoelectronics Group.

The proposed cells are effective in reducing the leakage power by more than 35% at 25°C and more than 60% at 110°C during standby mode of operation.

The static write leakage power and average write power are also minimized at the expense of minimal increase (less than 5%) in write delay.

Stack Forcing for Leakage Reduction

CNFET Invertor With and Without Stack Forcing

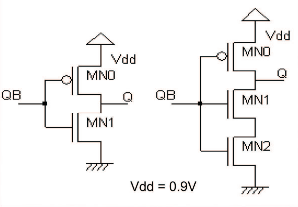


Table II. Device Parameters of CNFET Inverters shown above

CNFET	CNFET Inverter Without Stack Forcing		CNFET Inverter Without Stack Forcing	
	Parameter	Value	Parameter	Value
P-CNFET MN0	Gate Length	20nm	Gate Length	20nm
	Gate Width	40nm	Gate Width	40nm
	Chirality Vector	(16,0)	Chirality Vector	(16,0)
	No. of CNTs	1	No. of CNTs	1
N-CNFET MN1	Gate Length	20nm	Gate Length	20nm
	Gate Width	80nm	Gate Width	50nm
	Chirality Vector	(19,0)	Chirality Vector	(19,0)
	No. of CNTs	3	No. of CNTs	2
N-CNFET MN2	No transistor for inverter		Gate Length	20nm
			Gate Width	30nm
			Chirality Vector	(19,0)
			No. of CNTs	1

In CMOS technology, stack forcing involves replacement of pull down NMOS transistor with additional NMOS transistors connected in series to reduce leakage power by stack effect [13], [14] and the total gate area of all the NMOS of the stack is same as that of the non-stacked NMOS.

The condition for optimum iso loading condition for a two transistor stack [14] is given by

$$w/2 \le w_u,\ w_l \le w/2 \text{ and } w_u + w_l = w$$

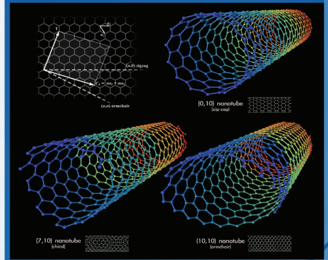
Where w is the width of NMOS before stacking, w_u is the width of upper transistor of stack and w_l is the width of the lower transistor of stack.
The leakage current flowing through the stack is dependent on number of off transistors in the stack and the technique is more effective in reducing sub-threshold leakage current for 45nm and 65nm CMOS nodes as explained in [14].

TABLE I. SUMMARY OF STATIC POWER OF CNFET INVERTERS WITH AND WITHOUT STACK FORCING UNDER VARIOUS INPUT CONDITIONS AND TEMPERATURES

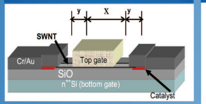
Inverter Schemes	Static Power at 25° C (pW)			Static Power at 110° C (pW)		
	Standby Mode	*Input '0' Mode*	*Input '1' Mode*	*Standby Mode*	*Input '0' Mode*	*Input '1' Mode*
Inverter without stack forcing	84.05	83.16	18.39	1091	1090	90.40
Inverter with stack forcing	38.82	34.47	14.37	250.9	245.4	86.38

CNFET Device Model and its Properties

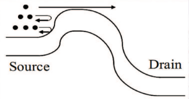
CNT Structure and Chirality Vectors



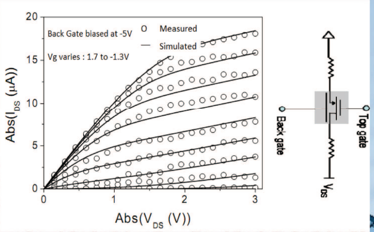
Dual Gate CNFET Structure



MOSFET-like CNFET Energy Band Diagram



Measured & Simulated DC Characteristics of a CNFET



CNFET consists of semiconducting single walled carbon nanotubes (CNTs) with high aspect ratio which constitute the conducting channel, bridging the source and drain contacts and gate controls the channel conduction electrostatically [2].

The SWCNFET can be considered as a sheet of graphene with a hexagonal lattice of carbon atoms rolled and connected by a connecting vector Ch = n1.ā1 + n2.ā2, where [ā1, ā2] are the lattice vectors and indices (n1, n2) are positive integers denoting chirality of tube [2]. Chirality determines whether the tube is metallic or semiconducting. In a MOSFET like CNFET model, applied gate voltage modulates the height of the non-tunneling potential barrier of the channel and causes variation in the electron density of the CNT channel, thereby varying the electrical conductivity of the channel [2],[11].

The CNFET I-V characteristics show that CNFET have higher Vds (drain to source voltage) and low channel on resistance compared to CMOS as explained in [2].

Threshold voltage of a CNFET varies inversely with CNT diameter [2] and can be approximated as

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}}$$

Where a denotes the distance between two carbon atoms, V_π is carbon π-π bond energy, e is unit electron charge and D_{CNT} is diameter of the CNT.

Threshold voltage of a CNFET can be varied for best device performance by altering tube's diameter through selection of chirality vectors.

Leakage current Ibtbt of a CNFET is caused due to band to band tunneling of majority carriers through the semiconducting sub-bands in sub-threshold region [2].

Band to band tunneling current can be approximated by the band to band tunneling probability (T_{btbt}) times the maximum current integrated from the conduction band at drain side up to the valance band at source side [2] as

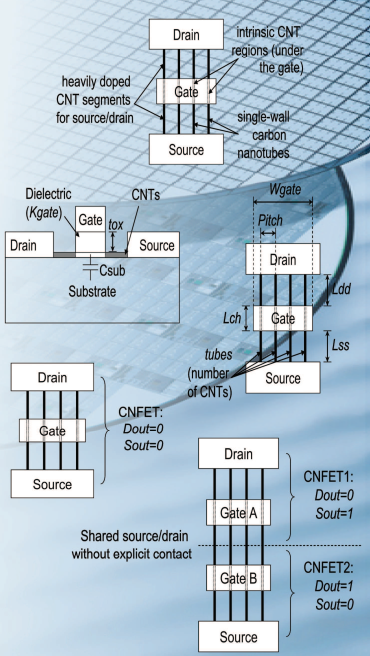
$$I_{btbt} \approx \sum_{\substack{k_m \\ m=1}}^{M} T_{btbt} \frac{4e}{h} \int_{E_{m,0}-E_f}^{V_{ch,DS}-E_{m,0}-E_f} \left(1 - f_{FD}(E)\right) \cdot dE$$

Where $V_{ch,DS}$ is the Fermi potential difference in channel near source side, h is planks constant, $E_{m,0}$ denotes half band gap of mth sub-band, k_m is wave number due to quantum confinement in the circumferential direction, E_f is the Fermi level of doped source/drain nanotube and is the Fermi Dirac function.

Dual-gate CNFET structure is found to have excellent sub-threshold properties and output characteristics without short channel effects and enables continued scaling of gate length [8].

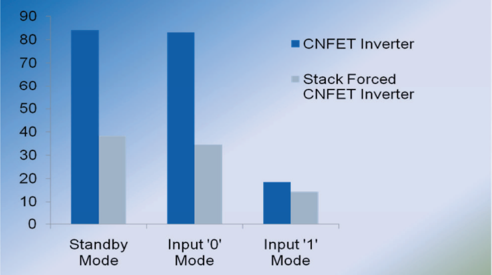
HSPICE model for a four terminal CNFET is presented in [12] and fourth terminal can also act as a back gate with applied reverse bias to enhance the electrostatic properties of CNFET. A high performance dual-gate CNFET with 40nm gate length is proposed in [8].

CNFET Structure and Model Parameters

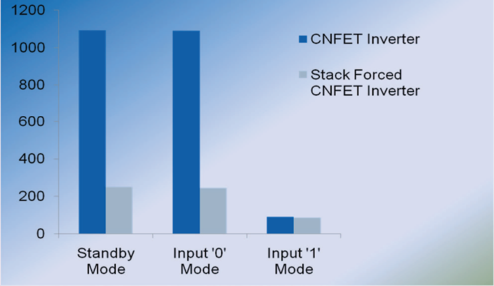


CNFET Stack Forced Inverter Simulation Results

Simulation Results for Static Power (in Pico Watt) at 25°C



Simulation Results for Static Power (in Pico Watt) at 110°C



The simulation results shows that the stack forcing is effective in reducing leakage power by

- * 53.81% in standby mode
- * 58.54% with bit '0' input
- * 21.85% with bit '1' input at room temperature.

At extreme temperature, the standby leakage power, input '0' leakage power and input '1' leakage power are reduced by 77%, 77.74% and 4.44% respectively.

Proposed CNFET SRAM Cells to Minimize Leakage

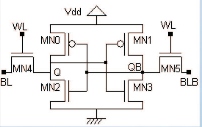
In this work two ultra low power CNFET SRAM cells are proposed, namely 6T cell with dual-gate N-type CNFETs and 8T stack forced cell to minimize leakage power dissipation.

The proposed cells are designed with dual chirality (different diameters for CNTs of N-CNFET and P-CNFET) for dual threshold voltages.

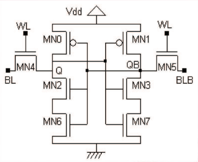
In [9], design of a high performance and stable dual chirality 6T SRAM is proposed and its performance is compared with that of a 32nm CMOS 6T SRAM cell.

In this work we have analyzed the leakage characteristics of CNFET SRAM cells and compared the performance of proposed low power cells with that of dual chirality based 6T SRAM cell given in [9].

6T SRAM Cell



8T Stack Forced SRAM Cell



6T SRAM with Dual Gate N-CNFETs

- In the 6T cell Shown in figure above, back gates of MN2, MN3, MN4 and MN5 are applied a reverse bias of -0.3V.

- The applied negative back gate bias improves the sub-threshold performance of the N-CNFETs [7] in the cell thereby minimizing the static power dissipation.

- The CNFET device dimensions were selected for optimized write operation and to prevent read upset problem as explained in [9].

- We have chosen the gate length to be 20nm in this work for comparison with the single gate dual-chirality 6T cell.

- Size ratio between the pull up transistor MN0 (with one CNT) and the access transistor MN4 (with 2 CNTs) is 0.5.

- Size ratio between the pull down transistor MN2 (with 3 CNTs) and access transistor MN4 (with 2 CNTs) is 1.5 to prevent read upset and for best write result.

- The dimensions of the cross-coupled inverters of the cell are similar to the inverter without stack forcing described earlier.

- The gate width, gate length and number of CNTs of access transistors (MN4 and MN5) are chosen as 60nm, 20nm and 2 respectively.

8T Stack Forced SRAM Cell

- An 8T CNFET SRAM cell shown in figure above consists of two cross coupled stack forced inverters.

- To maintain the optimum iso loading condition, gate widths of the N-CNFETs MN2, MN3, MN6 and MN7 were chosen to be 50nm, 50nm, 30nm and 30nm respectively.

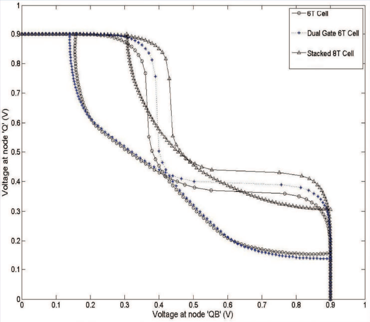
- Upper stack transistors MN2 and MN3 have two CNTs each

- Lower stack transistors MN6 and MN7 have one CNT each.

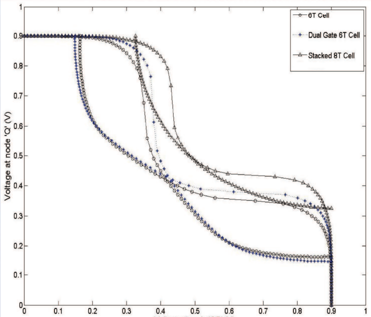
- The dimensions of other transistors of the cell are same as that of dual-gate SRAM cell explained above and the back gates of the N-CNFETs were tied to ground.

- The stack forcing is effective in reducing leakage current of the cell in standby mode as the current through the stack depends on number of off transistors in the stack.

SNM butterfly curves for 6T cell, 6T Dual Gate cell and 8T cell at 25°C



SNM butterfly curves for 6T cell, 6T Dual Gate cell and 8T cell at 110°C



Static noise margin (SNM) of the three cells is measured during read at two different temperatures. SNM is defined as the maximum value of DC noise voltage that the SRAM cell can tolerate without changing the stored bit [15] and SNM can be used as a metric for static stability of the cell [16].

TABLE III. SUMMARIZED SIMULATION RESULTS AT 0.9V POWER SUPPLY AND 25°C TEMPERATURE

	SRAM Cells		
	Single Gate dual-chirality 6Tcell	***6T cell with dual gate N-CNFETs***	***Stack forced Single Gate 8T cell***
Leakage Power in hold 0 Mode (pW)	108.40	70.26	60.78
Leakage Power in hold 1 Mode (pW)	105.40	65.59	53.83
Write 0 Lekage power (pW)	114.01	62.82	66.93
Write 1 Lekage power (pW)	113.20	68.91	68.55
Average read power (micro Watt)	4.53	4.52	4.52
Average write power (nW)	770.70	5.46	412
Write delay (ps)	9.23	9.61	9.49
SNM (mV)	163	173	108

TABLE IV. SUMMARIZED SIMULATION RESULTS AT 0.9V POWER SUPPLY AND 110°C TEMPERATURE

	SRAM Cells		
	Single Gate dual-chirality 6T cell	***6T cell with dual gate N-CNFETs***	***Stack forced Single Gate 8T cell***
Leakage Power in hold 0 Mode (pW)	1189	469	348
Leakage Power in hold 1 Mode (pW)	1192	466.1	331.9
Write 0 Lekage power (pW)	1196	459.9	350.1
Write 1 Lekage power (pW)	1190	467	349.5
Average read power (micro Watt)	4.62	4.61	4.60
Average write power (nW)	1070	6.88	578
Write delay (ps)	8.92	9.14	9.012
SNM (mV)	143	159	92

Conclusion

* This work has investigated the impact of leakage power in an optimised dual chirality 6T CNFET SRAM cell and two low power cells are proposed to minimize leakage during hold and active modes of operation.

* In the first proposed dual gate 6T cell, back gates of N-CNFETs are reverse biased and in the second 8T cell, stack forcing was employed to minimize leakage in sub-threshold region of operation.

* The proposed cells are effective in reducing the leakage power by more than 35% at room temperature and more than 60% at 110°C.

* Write power shows a significant reduction in the 6T dual-gate cell compared to the 8T cell.

* Static Noise Margin (SNM) of the 6T dual gate cell shows that the cell is more stable compared to 8T and 6T single-gate dual chirality based cell.

* Proposed cells can be used in design of CNFET based ultra-low power and high speed SRAM memories.

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