ANALOG SCALING CHALLENGES AND COMPACT MODELS

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imec

OUTLINE

Device scaling roadmap

Analog scaling induced by logic

Compact modeling at IMEC

Extrinsic parasitics

Conclusions

FUTURE APPLICATION REQUIREMENTS

HIGH-PERFORMANCE COMPUTING

- Increased performance at constant power density
- Constraints = Thermal and energy budget
- Device: low-Vt, mobility boosters

HIGH-PERFORMANCE MOBILE

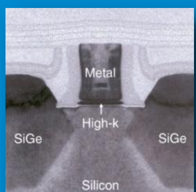
- Increased performance at constant leakage
- Constraints = Battery, Leakage in multi-cores
- Device: Strong SCE control

IMEC LOGIC SCALING ROADMAP

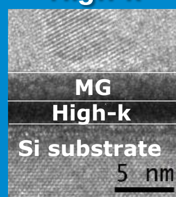
V_{dd} 1.0-1.1V 0.9-1.0V 0.8-0.9V 0.7-0.8V 0.6-0.7V 0.5-0.6V < 0.5V

Strain & Advanced Gate Stack Engineering

SD/stressors

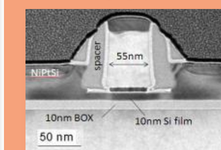


Metal Gate +High-k



Fully-depleted Channel for Improved Electrostatics

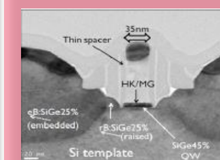
Ultra-Thin SOI



Multi-gate FETs

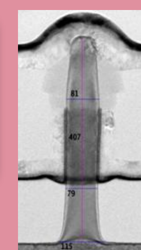
Band-Engineered Channel for Enhanced Transport

High-Mobility Channels



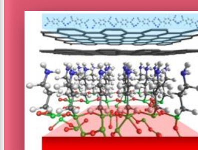
(SiGe, Ge IIIV)

Nanowires/ Tunnel FETs



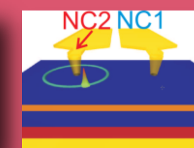
Novel Materials/ New Transport/ Extreme Electrostatics

2D Materials



(Bi-layer Graphene)

Quantum/ Spin Devices



Tech Node

32/28nm — *14nm* — *7nm* — ...

45nm — *22/20nm* — *10nm* — *5nm*

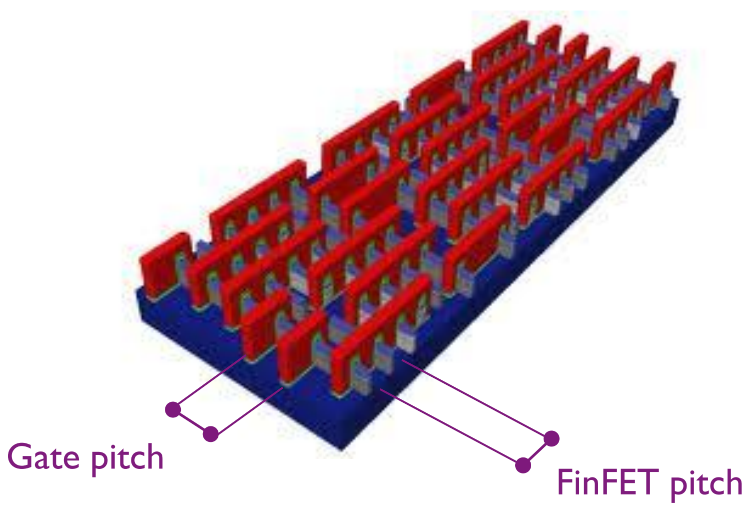
- **Feature Dimension & Voltage Scaling** are concurrent drivers
- **Material & Device Architecture Innovations Enablers** of continual scaling

SYSTEM SCALING DRIVERS = PPAC

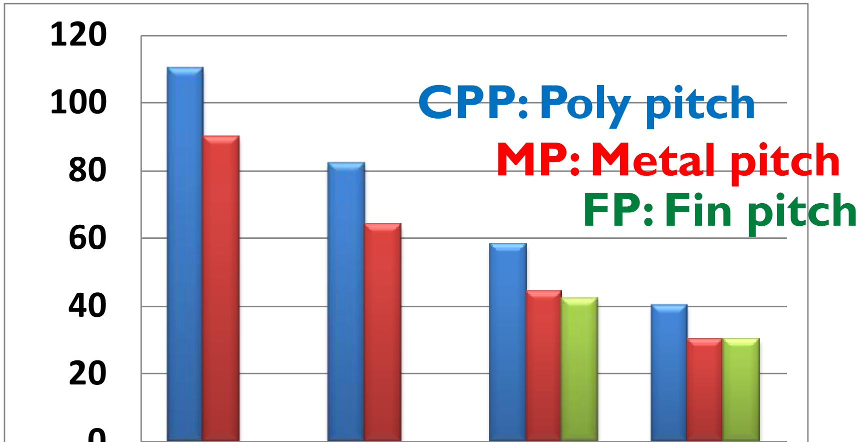
Node-to-node scaling targets

- >50% area downscaling node-to-node
- >30% more fmax node-to-node at constant power
- >20% more fmax at constant leakage
- >35% more fmax at constant energy
- <15% process cost

Pitch scaling to ensure 50% area downscaling



IMEC pitch targets – [nm]



	28	20	14	10
CPP	110	82	58	40
MP	90	64	44	30
FP	0	0	42	30

Technology node – [nm]

CPP=Contacted Poly Pitch (Gate); MP=Metal1 Pitch; FP=FinFET pitch

DOES DIGITAL-CENTRIC SCALING ENABLE ANALOG SCALING?

Digital

Short-channel Devices

Reduce delay (CV/I)
Reduce power (Vdd)
Increase Ion/Ioff
Reduce area
Improve matching (AVt)
Reduce cost / Mgates

↔

Scaling Drivers
of advanced nodes

Analog

Short/Long-channel devices

Higher frequency (fT, fmax)
Higher intrinsic gain (gm/gds)
Higher linearity (IIP3~gm/Id)
Lower noise (1/f)
Higher matching (AVt)
Higher Cratio with high Q

Passives (add-ons? + existing?)

Higher density (R,L,C)
Higher matching (R, C)
Higher quality factor (L, C)
Higher linearity (R,C)
Lower leakage (C)
Better temperature behavior (R)

ANALOG CO-EXISTS WITH DIGITAL

MPU/SoC is a system with logic, memory, and analog

- PLLs for clock generation
- Bandgap based temperature sensors
- DLLs for the logic and memory interface
- SERDES for high-speed IOs
- Linear DACs for the video display
- Power supply regulators
- IO circuits

More-or-more convergence of RF front-end with digital

- LNA
- Mixers
- LC-VCOs
- ADC
- Power amplifier

SCALING IMPACT ON ANALOG FOMS: ASSUMING AN IDEAL LONG-CHANNEL DEVICE

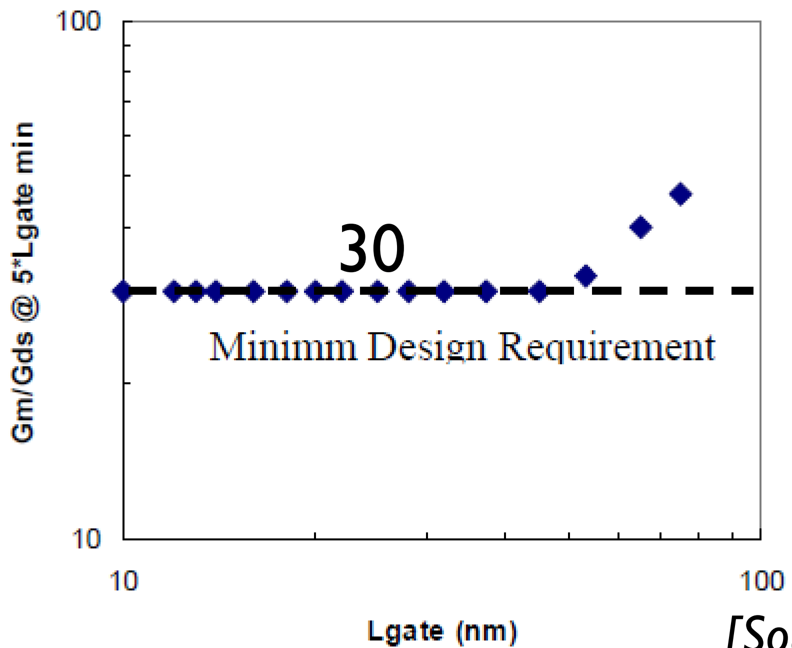
Technology	Quasi-Static	Fixed Vdd
Supply voltage	$K^{-1/2}$	1
Lateral dimensions	K^{-1}	K^{-1}
Vertical dimensions - t_{ox}	K^{-1}	$K^{-1/2}$
Doping concentration	K	K
Id,sat	1	$K^{1/2}$
Transconductance (gm)	$K^{1/2}$	$K^{1/2}$
Out. conductance (gds)	$K^{3/4}$	K
Cd/Co	$K^{-1/4}$	1
SS	>1	1
1/f noise	1	$K^{1/2}$
Long channel index	$K^{-1/6}$	$K^{-1/3}$

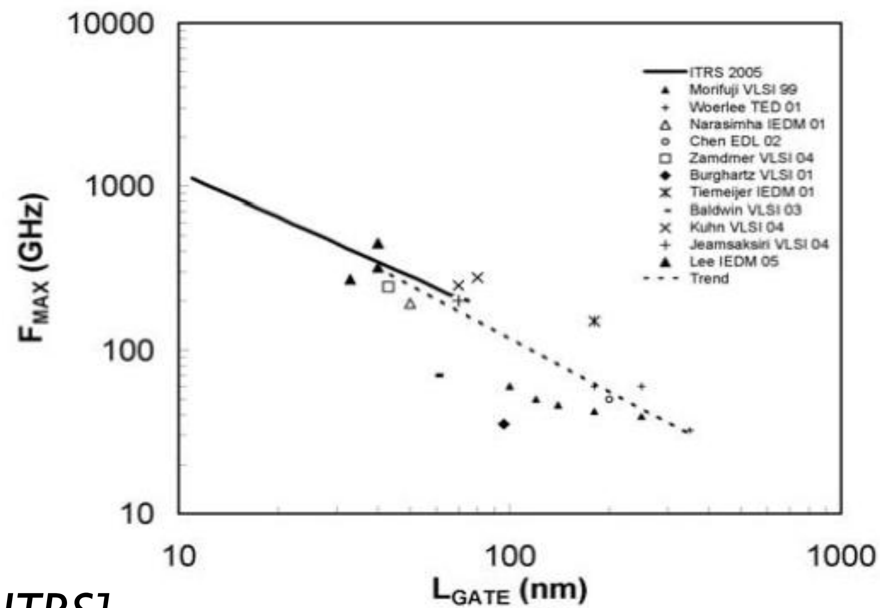
Circuit parameter	Quasi-Static	Fixed Vdd
Voltage gain – gm/gds	$K^{-1/4}$	$K^{-1/2}$
Voltage gain – 2 stage opamp	$K^{-1/2}$	K^{-1}
Power density	$K^{3/2}$	$K^{5/2}$
Miller capacitance - Cc	K^{-1}	$K^{-3/2}$
Gain bandwidth – gm/Cc	$K^{3/2}$	K^{2}
Slew rate (Id,sat / (Vdd.Cc)	$K^{3/2}$	K^{2}
SNR – low-frequency apps	$K^{-1/2}$	$K^{-1/2}$

[Source: Wong, IEEE JSSC 1983]

How about non-idealities: short channel, advanced devices, novel layout strategies, ...?

IMPACT OF SCALING ON DEVICE FOMS



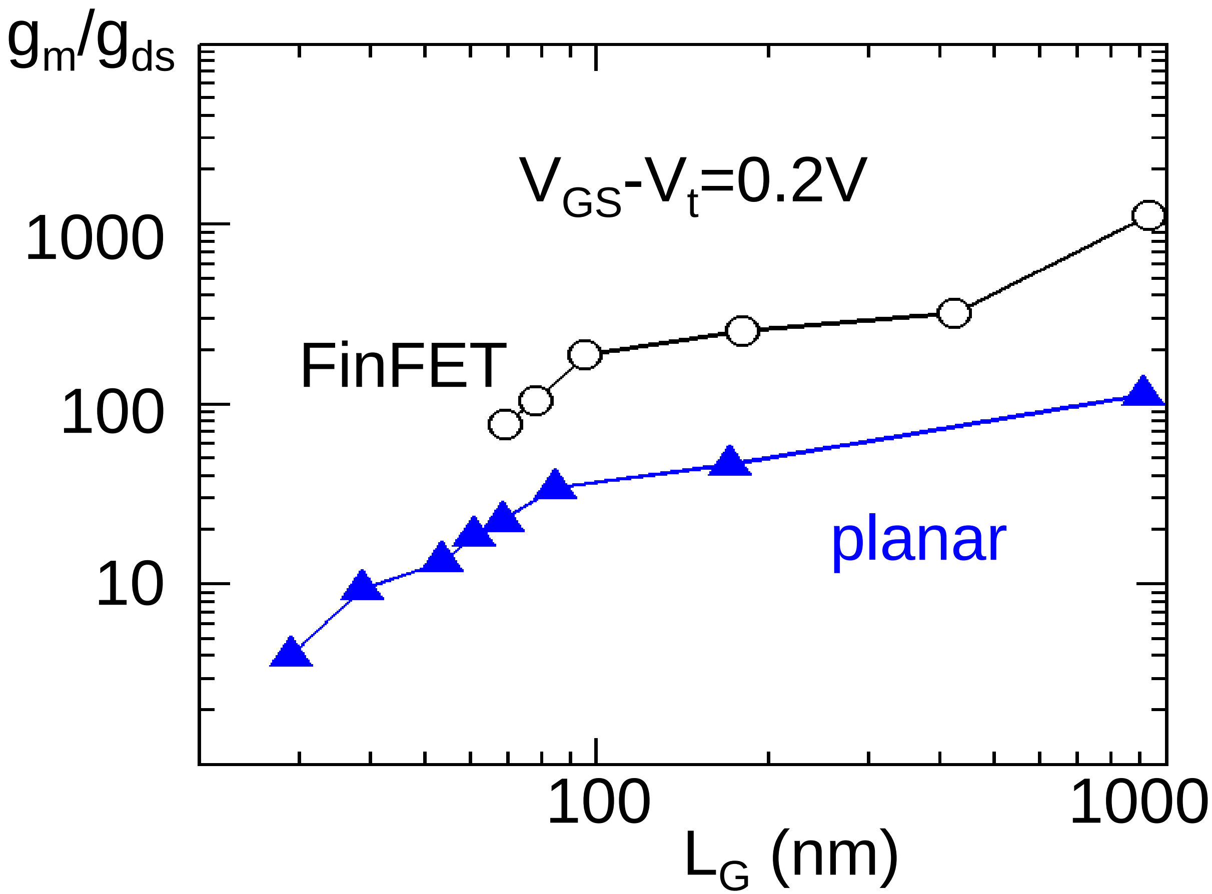


[Source: ITRS]

Lgate versux tox scaling
Doping control
Workfunction tuning
Advanced devices

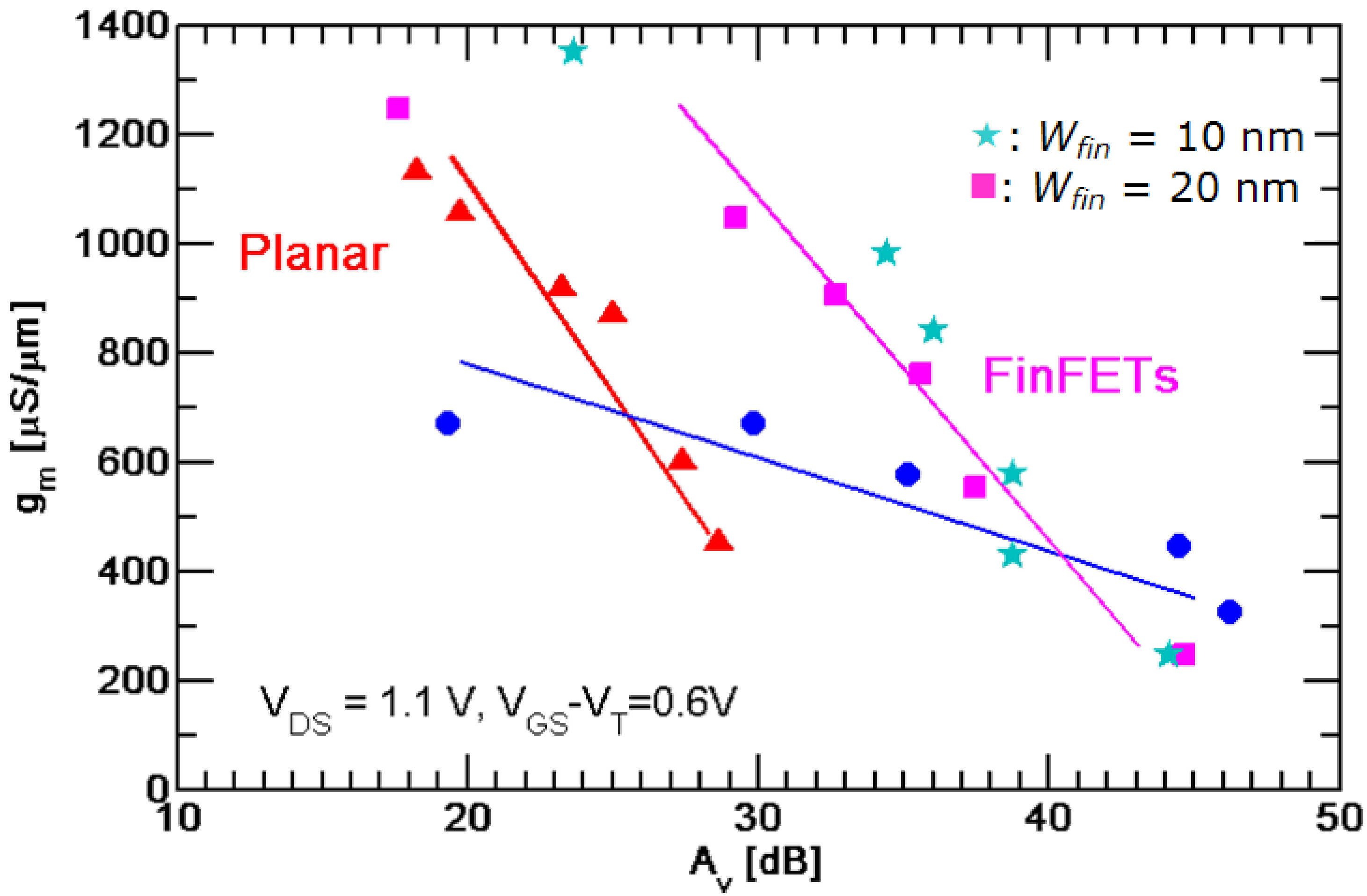
Careful layout
Reduced capacitance
Reduced gate and S/D resistance

NEW DEVICE ARCHITECTURES IMPROVE GM/GDS



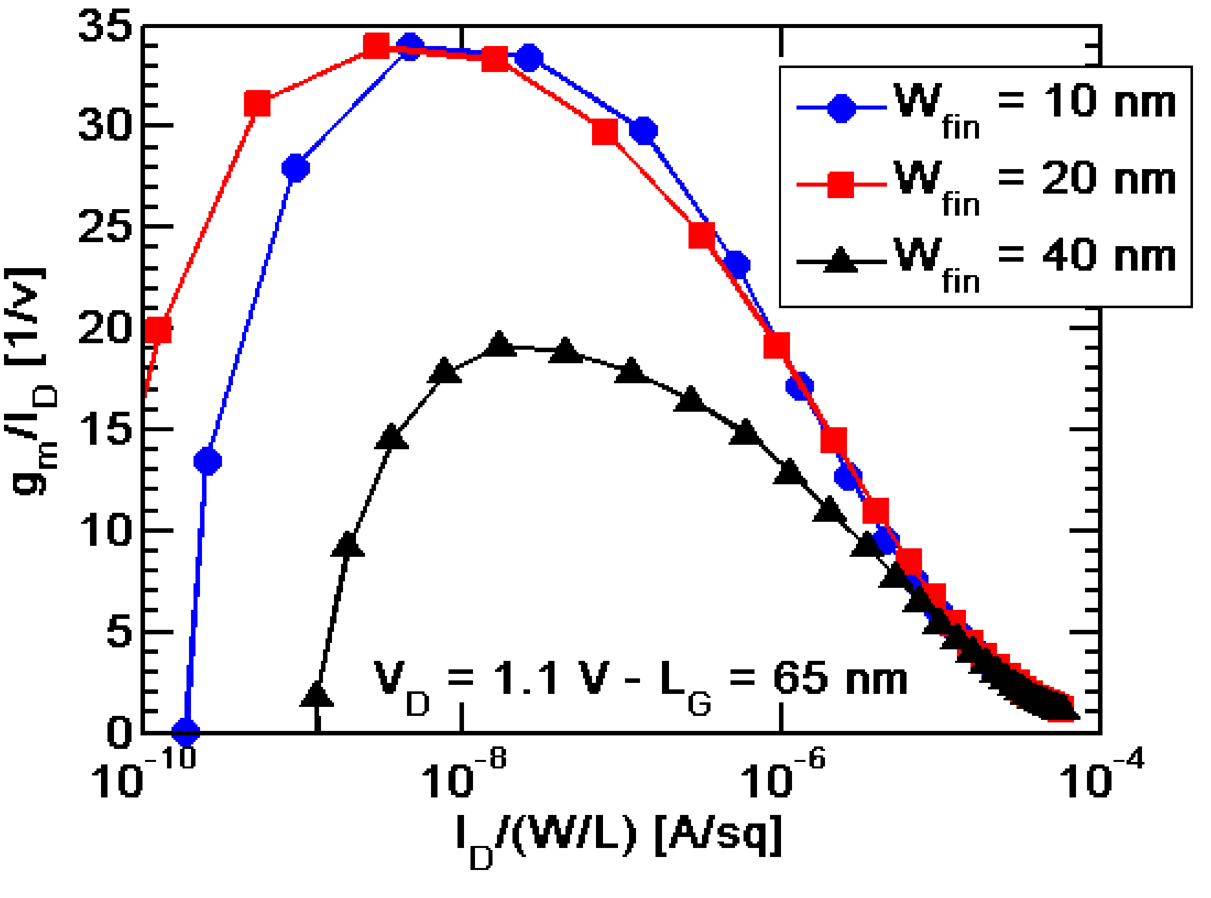
less short-channel effect → higher intrinsic gain (gm/gds)

FINFETS GIVE A BETTER TRADE OFF BETWEEN SPEED AND GAIN WRT PLANAR

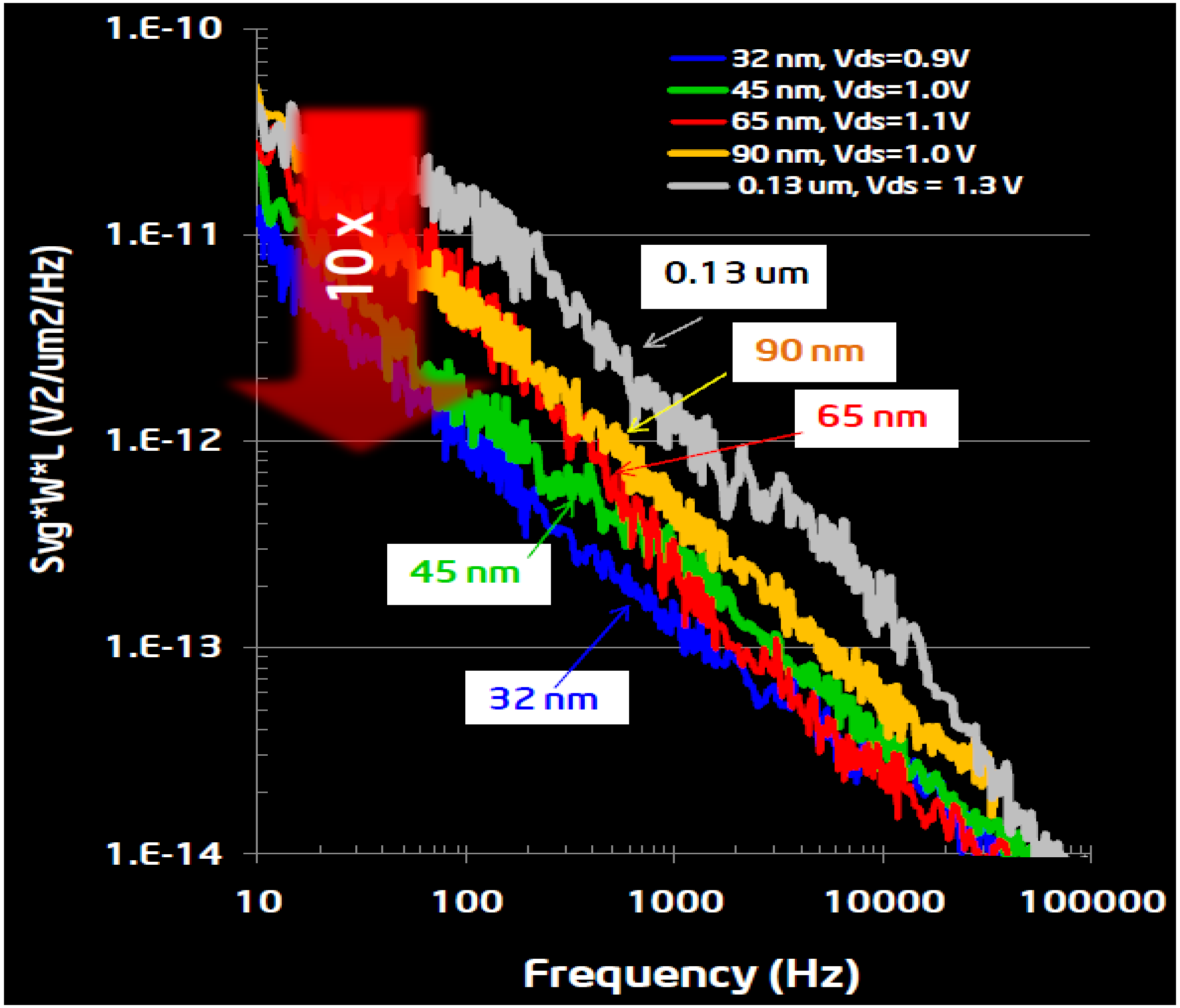


FinFETs offer a serious alternative to planar Devices for digital and low frequency analog applications...

A BETTER SCE IMPROVES ALSO THE CURRENT EFFICIENCY – NARROW FIN BRINGS BETTER LINEARITY



I/F NOISE GETS BETTER WITH TECHNOLOGY SCALING



[source: IEDM '10 C.H. Jan]

COMPACT MODEL IS DETRIMENTAL IN DESIGN-TECHNOLOGY ASSESSMENT

Process assumptions

PDK

Design rules

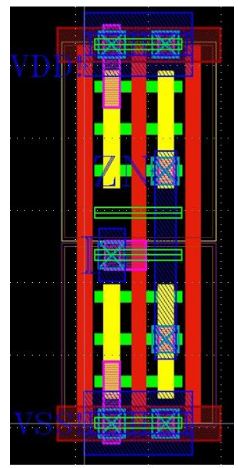
Compact models

Parasitics

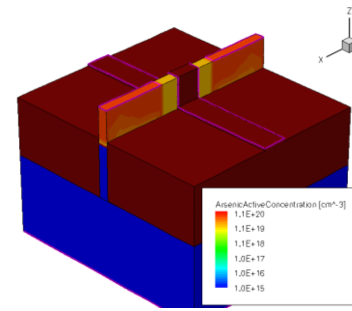
Standard cell

SRAM

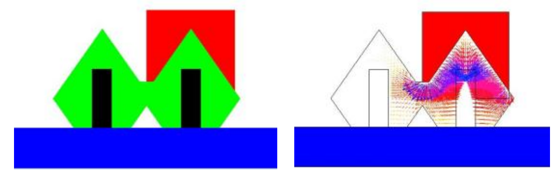
SoC PPA-C



CELL



TCAD → CM



EXTRINSIC PARASITICS

IMEC PRE SILICON ROADMAP

Technology definition

System assessment

Process / technology assumptions

Experimental vehicles

TCAD results

Reference data

Compact models

PPAC

Performance
Power
Area
Cost

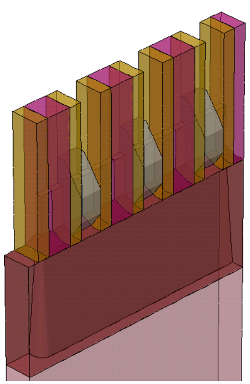
ring oscillators to system level

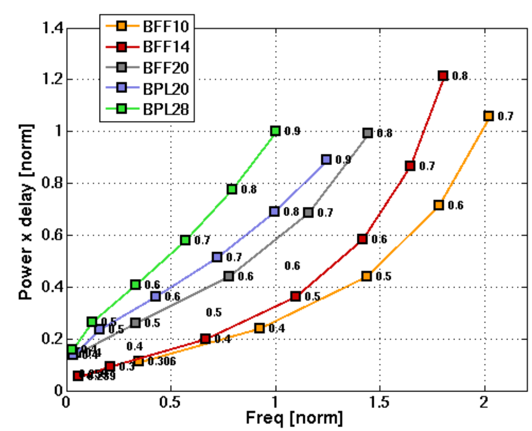
Change assumptions and process flow

Change parameters

Change layout

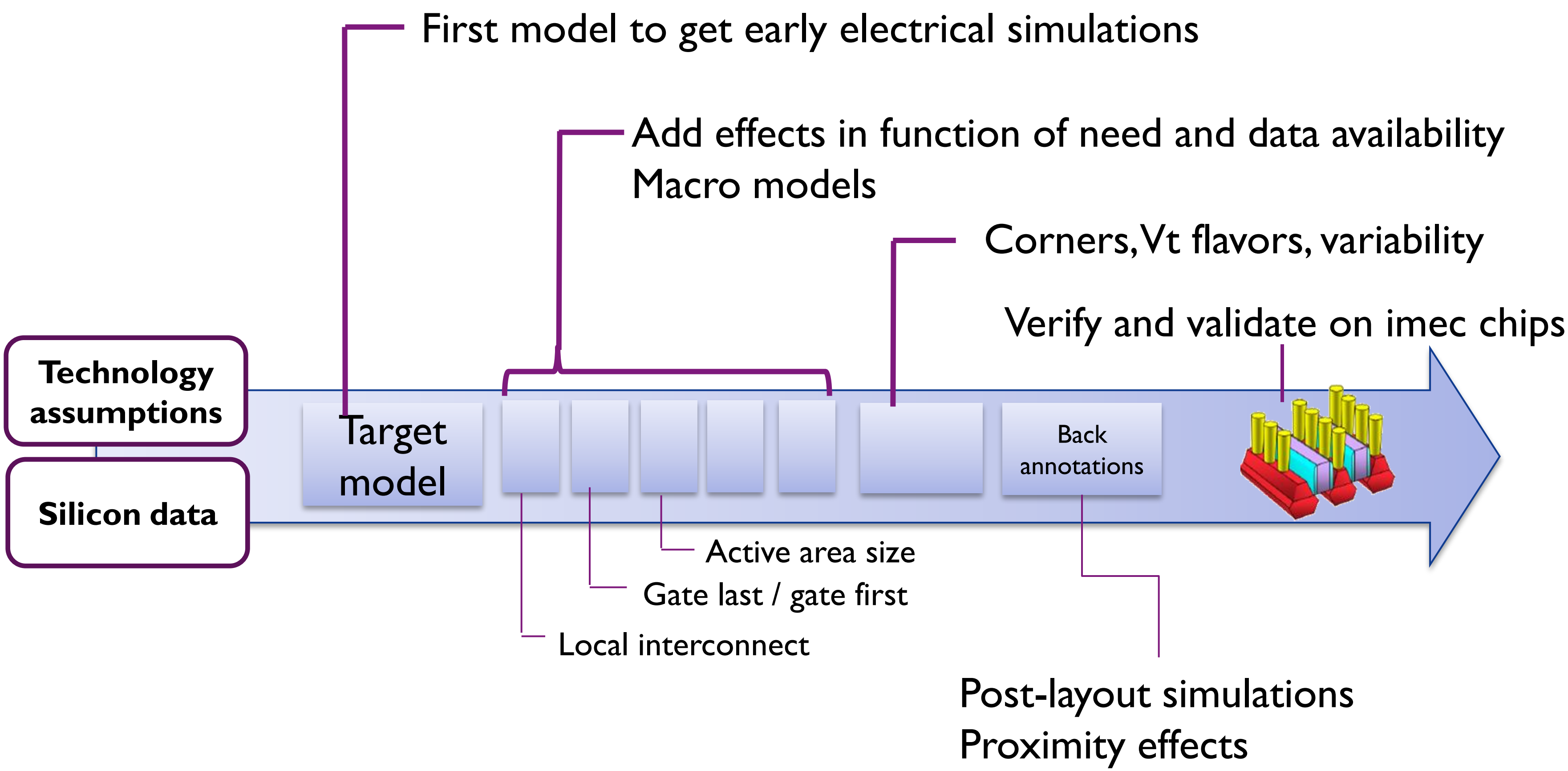
Applications targets met?





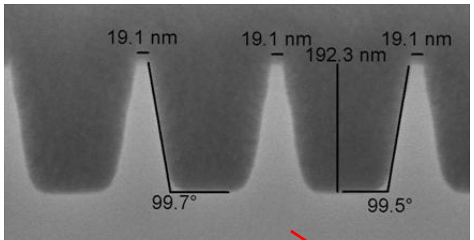
COMPACT MODELLING APPROACH

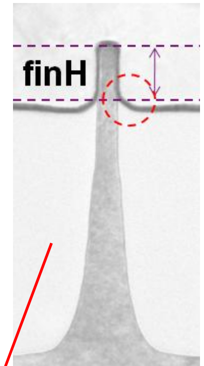
- Follow compact models industry standards
- Develop ad hoc macro models
- Silicon validation

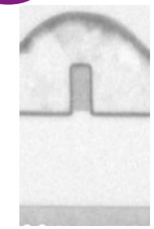


EXAMPLE : FINFET SCALING @ IMEC

Fin Shape & Surface Orientations

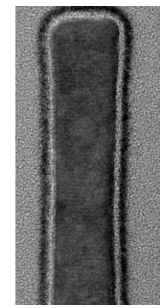


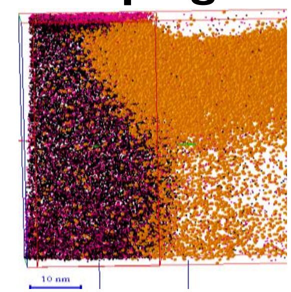




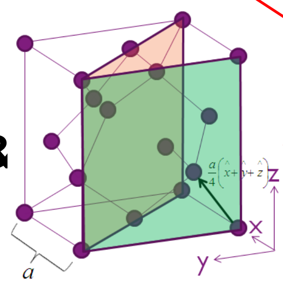
Variability Bulk Vs. SOI

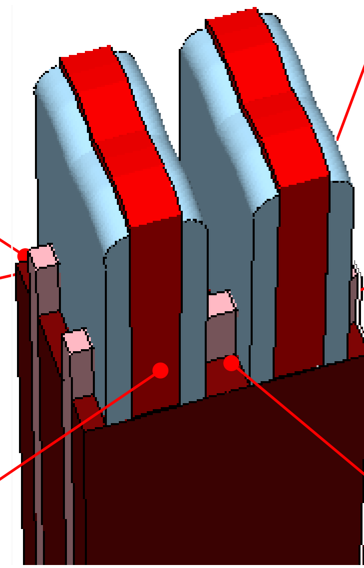
Special Implants & Doping



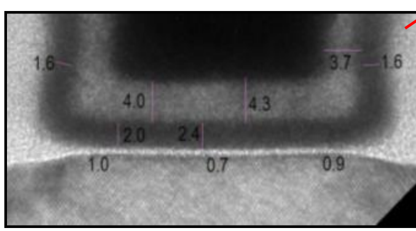


Unique FinFET Reliability & RTN

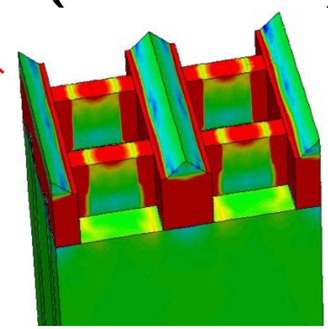


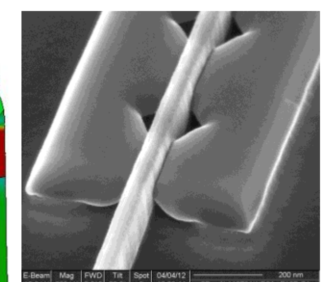


Advanced Gatestack for FinFETs



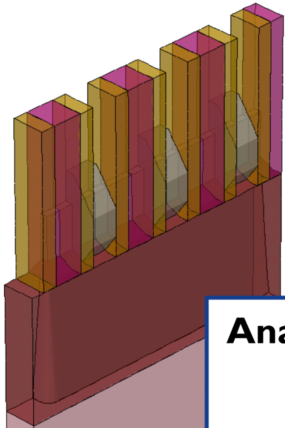
S/D Epi stressors (SiGe & Si:C)





- Enabling of aggressive 14nm FEOL+BEOL platform
- Scaling platform to accelerate 10nm & beyond R&D

EXAMPLE: INCLUDING LDE IN BFF14 MODEL



TCAD stress simulations

Analytical stress profiles

stress = f(sa, sb)

Stress to electrical parameters

Compact model imec macro

Compact model BSIM CMG

Experimental data BFF14

Structures for Layout dependent effects

calibration

2013

Physics based compact model

Inclusion of layout dependent effects in macro

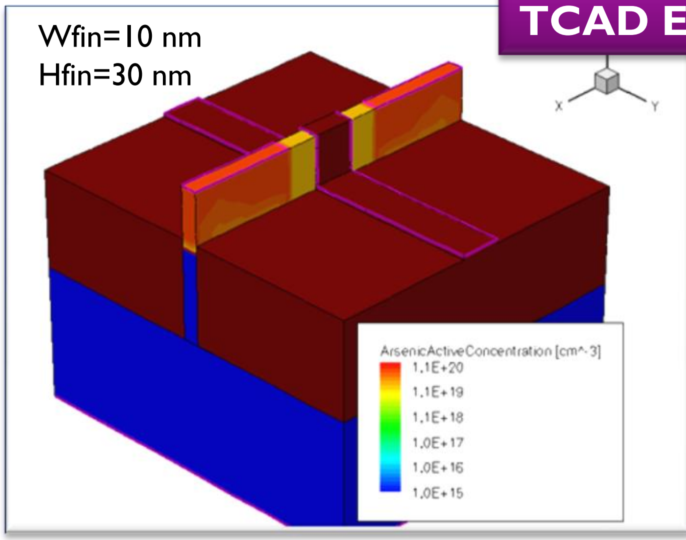
Considering stress from

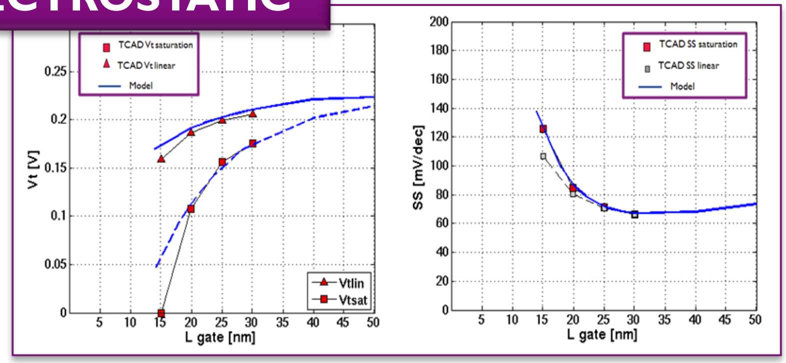
- EPI Source/Drain
- STI
- Replacement Metal Gate
- Local interconnect
- …

BUILDING COMPACT MODEL

TCAD ELECTROSTATIC

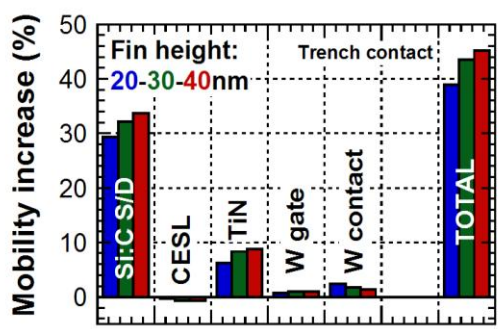
Wfin=10 nm
Hfin=30 nm





+ PERFORMANCE / STRAIN

Breakdown per stressor



Si:C S/D is the also main effective stressor, 30-35% mobility increase for scaled fin and gate pitch.

Physical parameter inputs for BSIM CMG physical MODEL:

- ✓FW FH
- ✓Lg
- ✓Tox
- ✓ channel doping
- ✓Gate work function
- ✓geometry and doping for parasitic capacitances and resistances

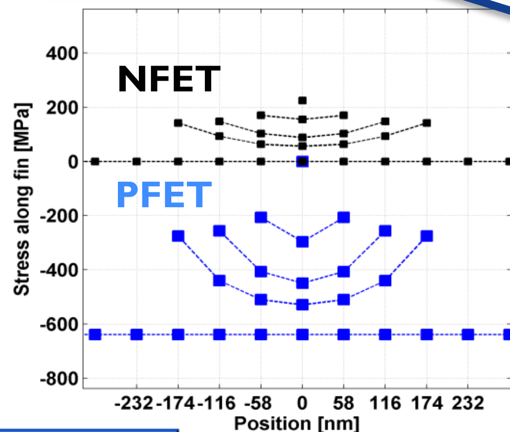
EXAMPLE: INCLUDING LDE IN BFF14 MODEL

From layout dependent stress to RO performance

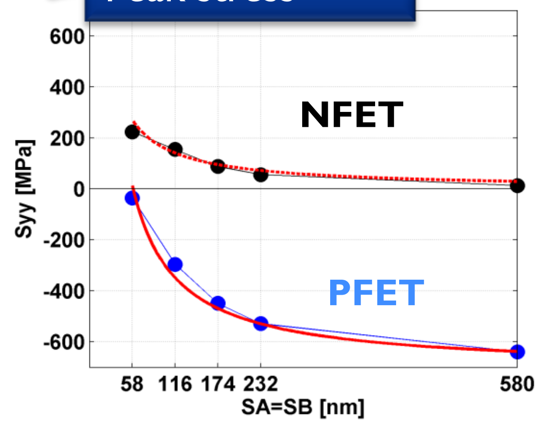
NFET
STI tensile 1 GPa

PFET
SiGe no recess 3Pa
STI tensile 1 GPa

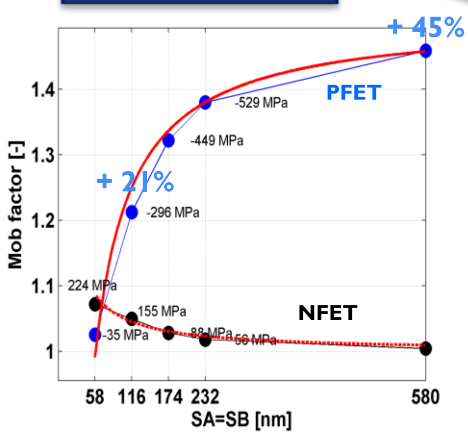
TCAD stress along fin



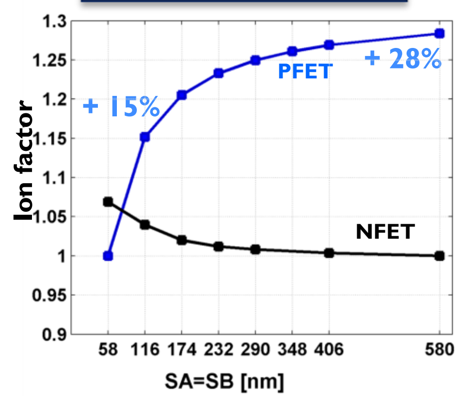
Peak stress



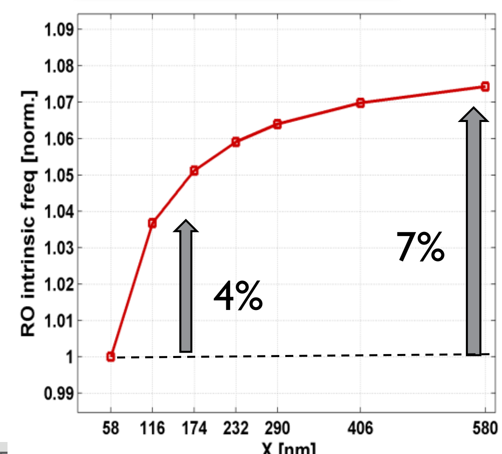
Mobility



Ion currents



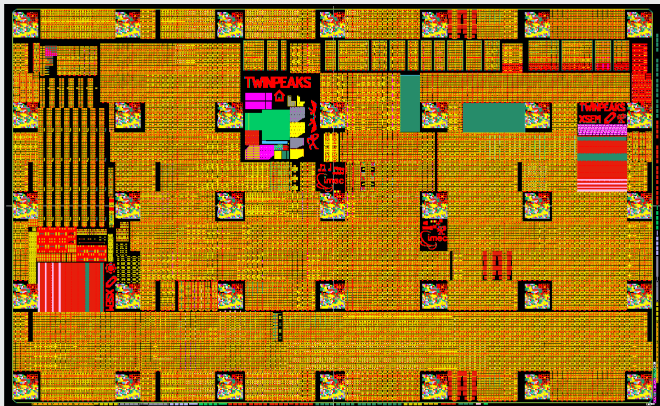
RO frequency



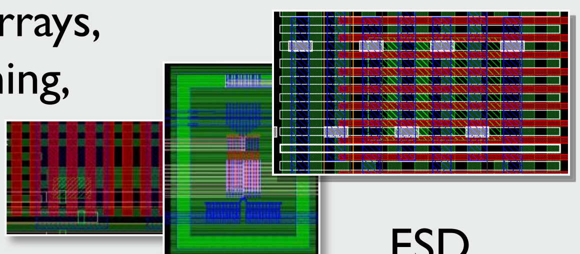
SILICON VALIDATION - DESIGN EXPLORATION

TwinPeaks test-site T/O

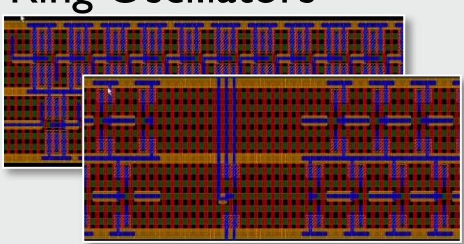
- 14nm CPP58/62, FP45
- 10nm CPP40/45/50, FP30



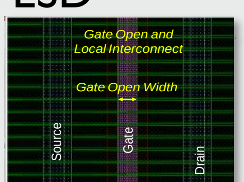
FET arrays,
Matching,
LDE



Ring Oscillators



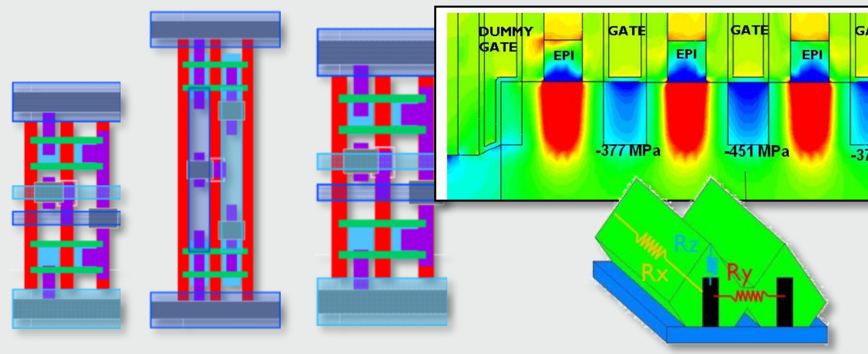
ESD



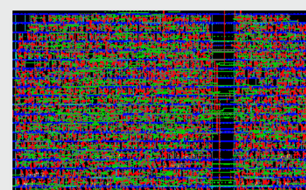
…

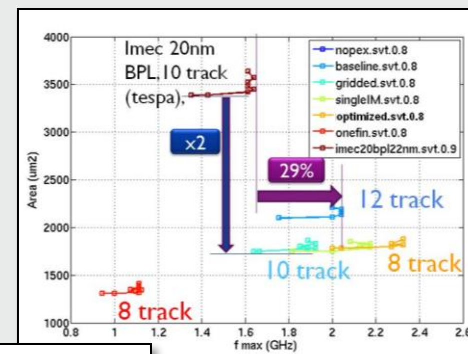
14nm design exploration

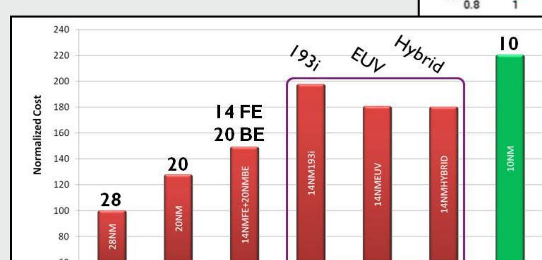
- Standard cell architecture
- Technology options (PDK)



- PPA-C



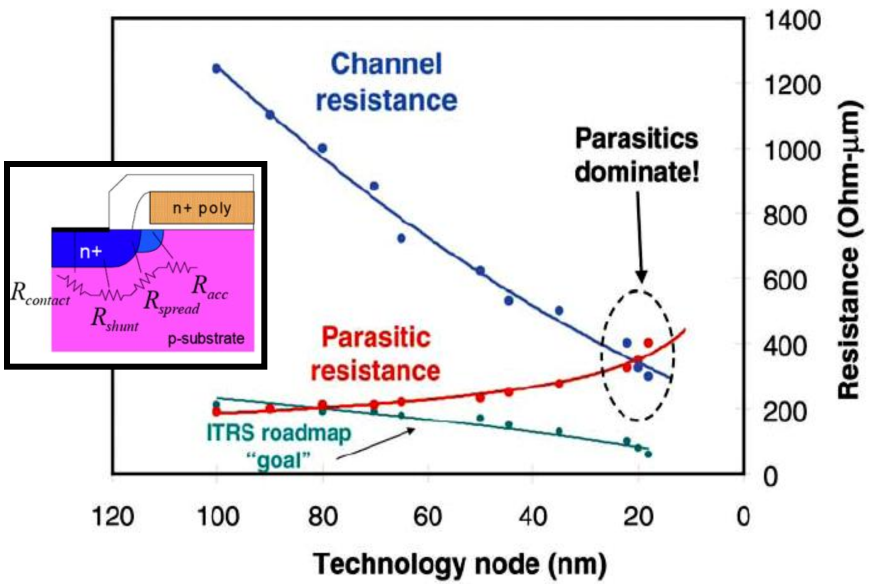


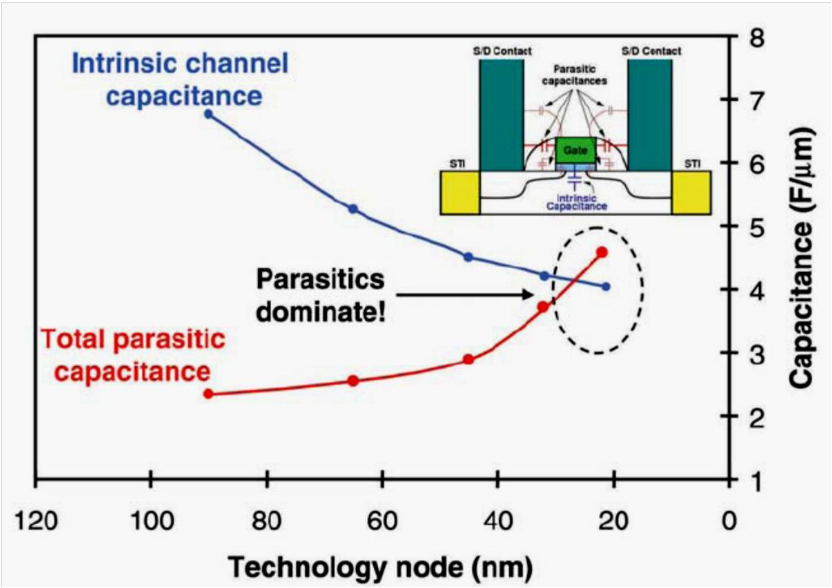


DEVICE ARCHITECTURE INFLUENCES EXTRINSIC PARASITICS

Parasitic resistances might become larger than the channel resistance

Parasitic capacitance might become larger than the one of intrinsic gate capacitance





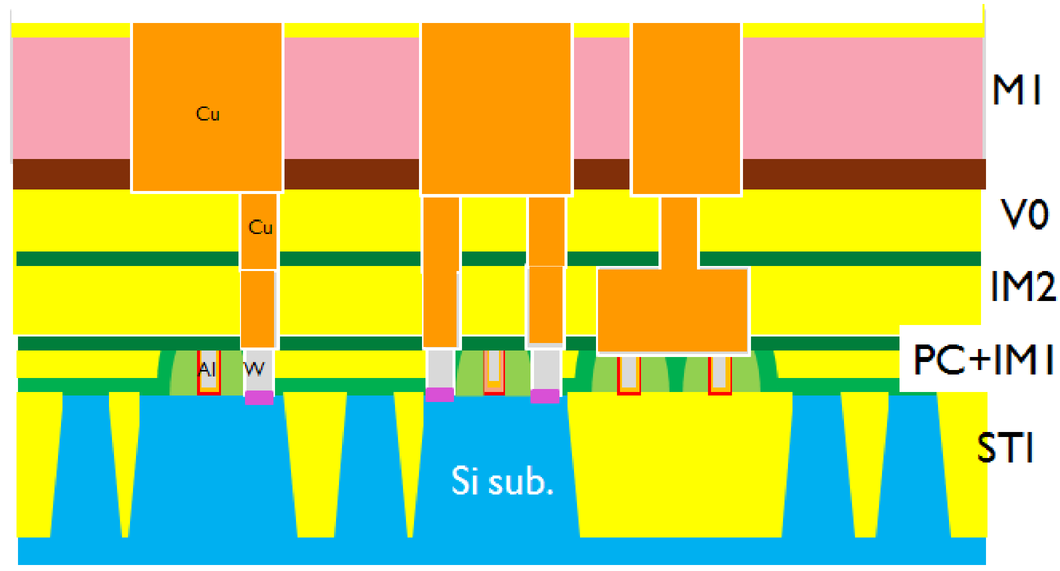
20NM DEVICE OPTIONS: BULK PLANAR / UTB SOI / BULK FINFET

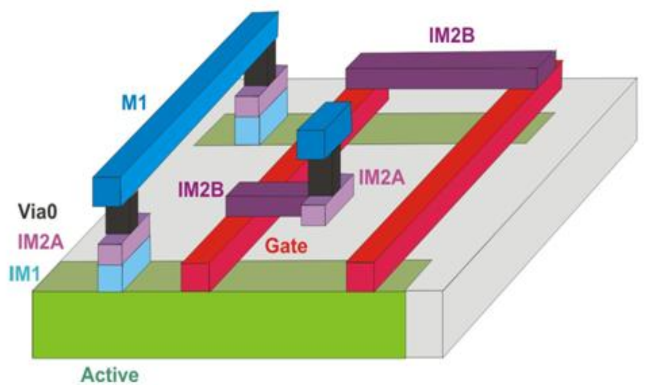
20nm BPL/UTB/BFF (193i DP)

Dimensions	nm
FF width	16
FF height	35
FF pitch	64
Mgate width	22
Mgate pitch	82
Mgate cut	50
Mgate-active extension	30
IM1 bottom width	22
IM1 pitch	82
IM2 bottom width	24
IM2 pitch	82
Via0 size*	50x40
Via0 pitch_horz	82
Via0 pitch_vert	64
M1 width	32
M1 pitch	64
M1 tip-to-tip (same/split)	80 / 40

*physical Via0 is generated with a Boolean (AND) operation from the drawn via0 & metal gds layers – based on dual damascene Cu process assumption

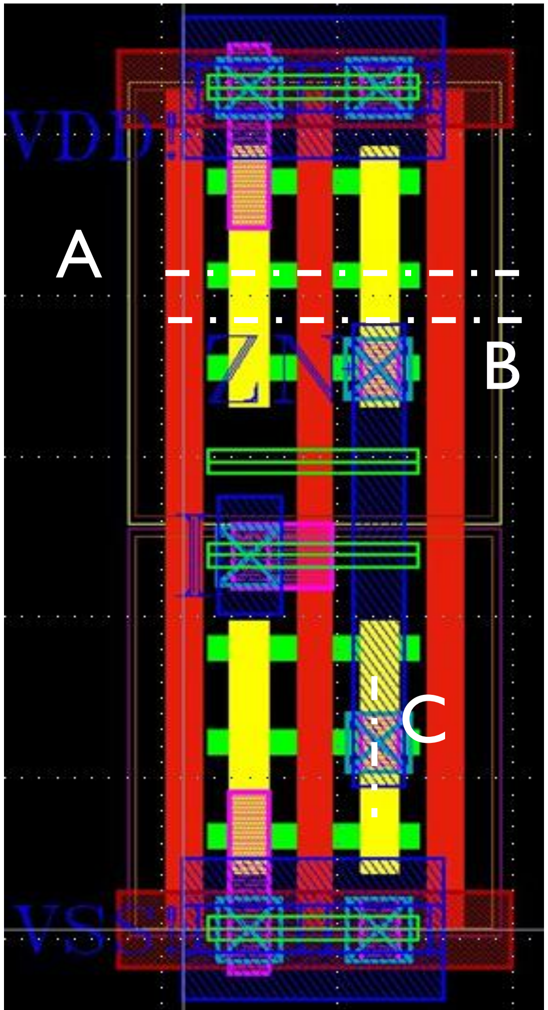
Similar assumption for Everest LI28 (under processing..)

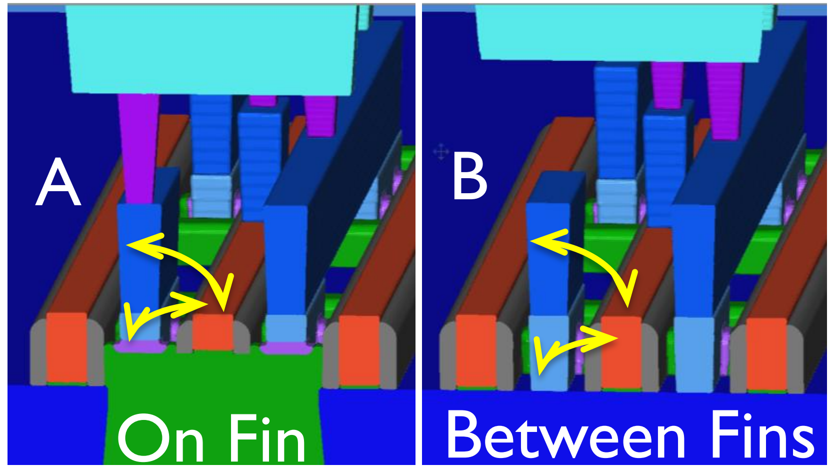


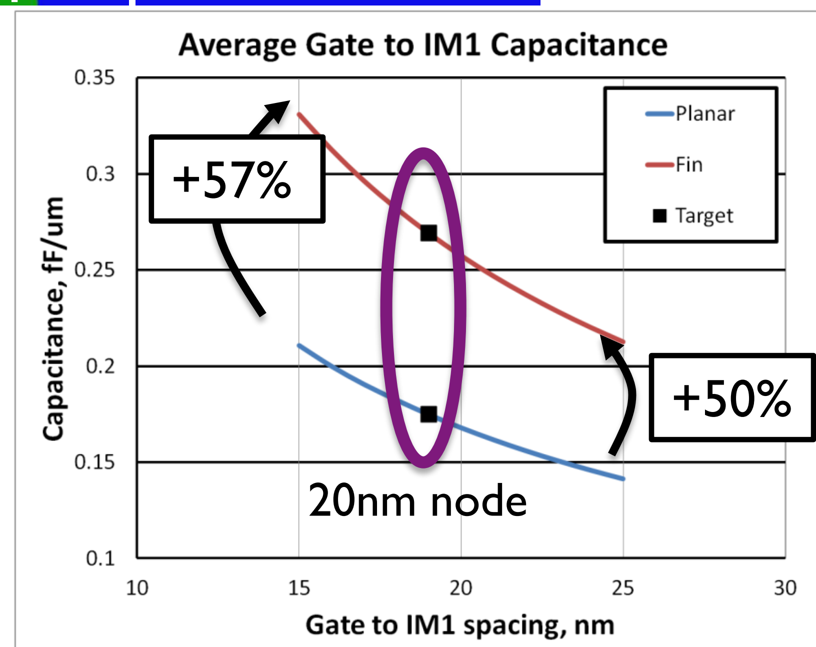


Double patterning M1(LELE)

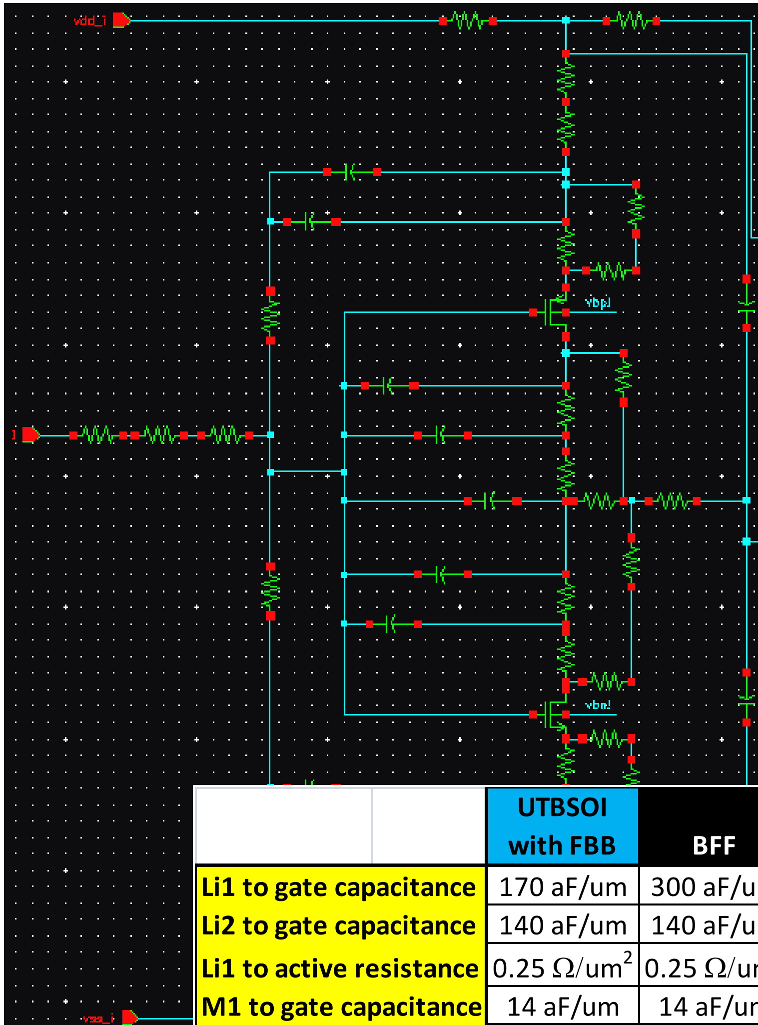
LOCAL INTERCONNECT (IM1) TO GATE COUPLING IS DOMINANT





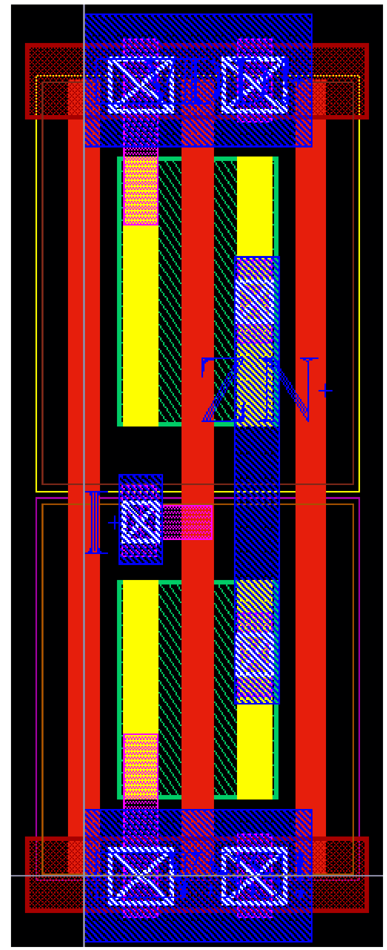


AN INVERTER WITH PARASITICS



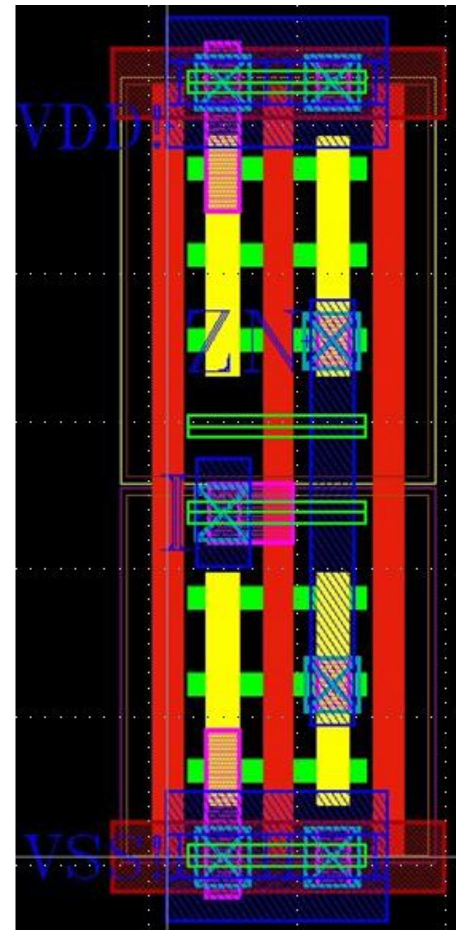
	UTBSOI with FBB	BFF
Li1 to gate capacitance	170 aF/um	300 aF/um
Li2 to gate capacitance	140 aF/um	140 aF/um
Li1 to active resistance	0.25 Ω/um^2	0.25 Ω/um^2
M1 to gate capacitance	14 aF/um	14 aF/um
Via0 resistance	17.9 Ω	17.9 Ω
M1 routing capacitance	16.5 aF/um	16.5 aF/um
M1 routing resistance	0.84 Ω/□	0.84 Ω/□
Li1 routing resistance	29.45 Ω/□	14.73 Ω/□

Wp=192n, Wn=160n



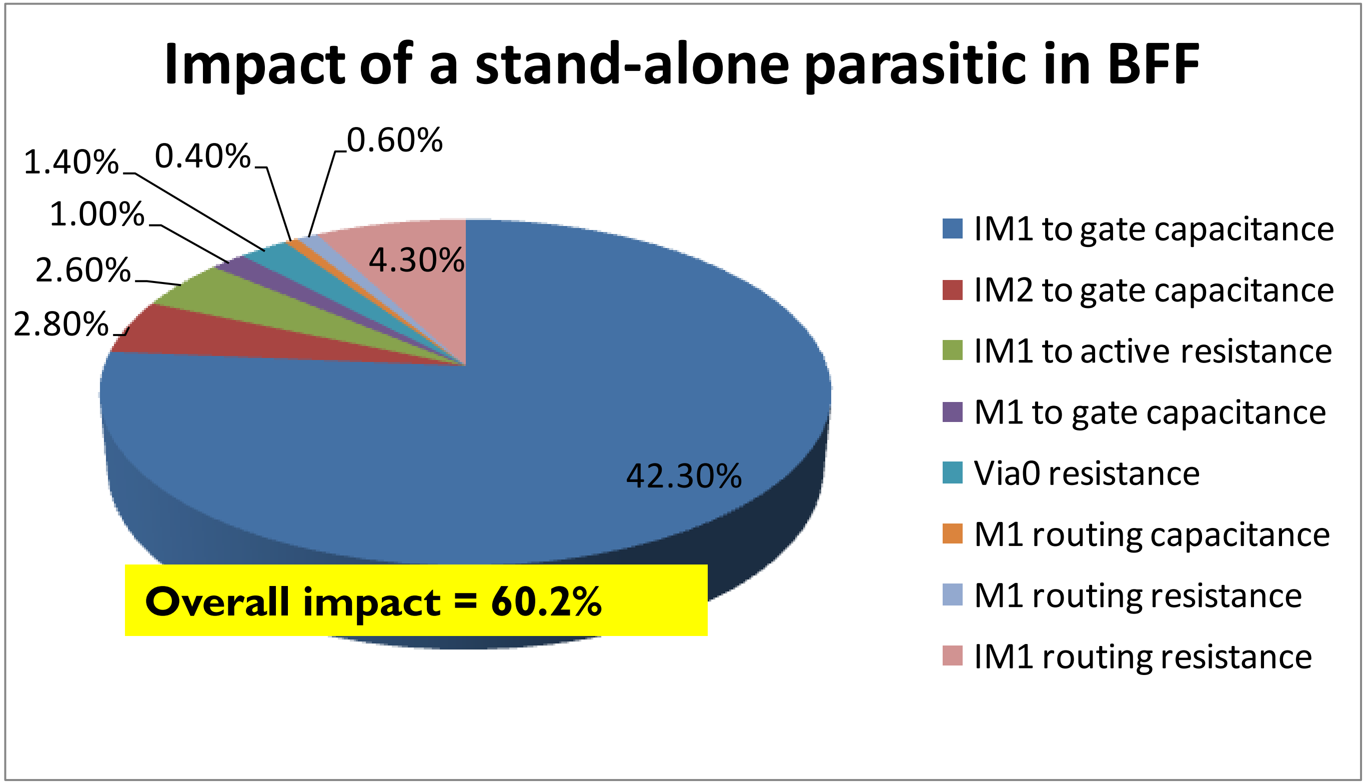
Planar / UTB-SOI inverter

Wp=258n, Wn=258n



Bulk finFET inverter

STAND-ALONE IMPACT OF A PARASITIC WHEN OTHERS ARE EXCLUDED



- IM1-to-gate coupling capacitance impacts the delay most
- Its stand-alone impact in delay is 42.3%

CONCLUSIONS

Analog scaling challenged by parasitics, matching, and low headroom

- Mitigated with circuit and device innovations that exploits advantages of scaling

New device architectures help analog scaling in logic technologies

- Lower gm/gds is mitigated by new device architectures
- Advanced gate stack engineering improves 1/f and device reliability

Compact model must be compatible with the process assumptions baseline

FinFETs suffer from extrinsic parasitics: particularly due to capacitance between gate and S/D

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