# *Advances on Compact Multi-Gate MOSFET Modeling*

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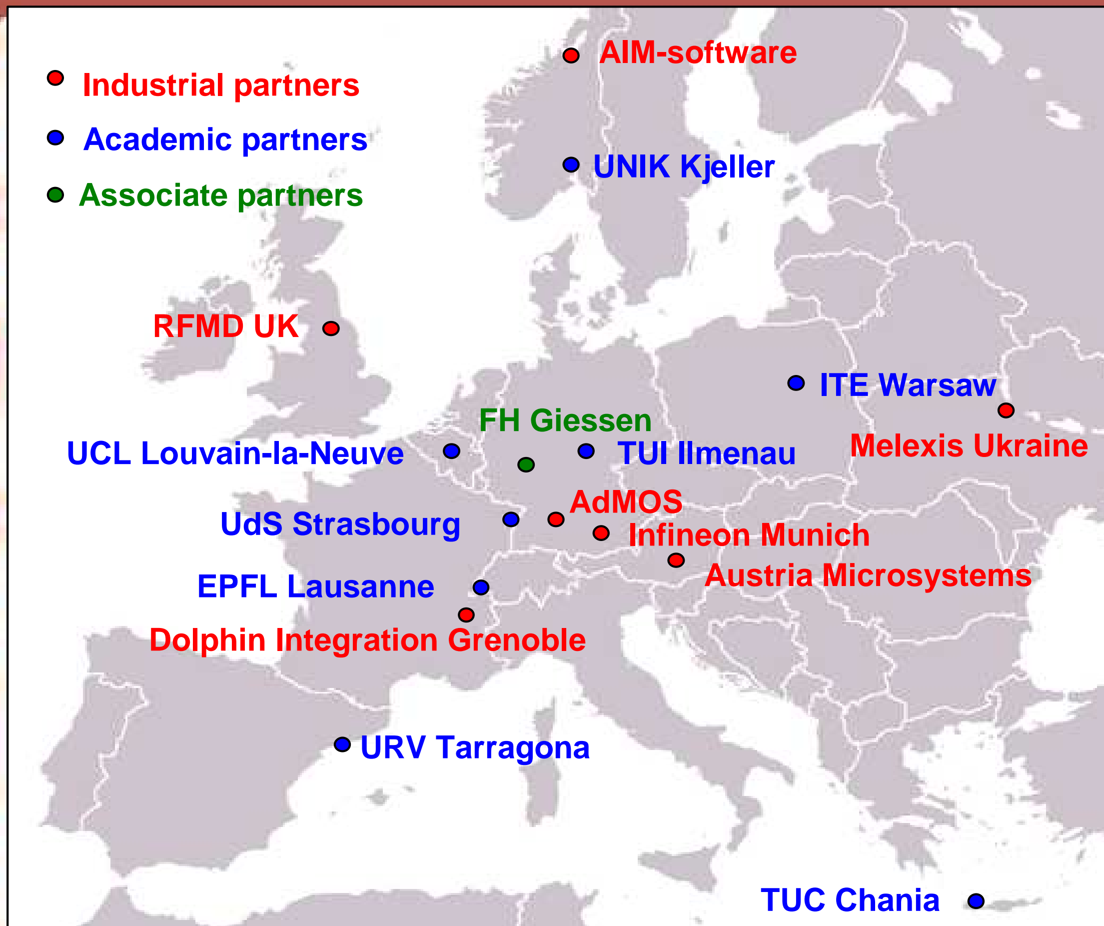

- Marie-Curie PEOPLE Programme: Industry-Academia Partneship and Pathways Project (IAPP FP7, ref. pro. 218255)

- Duration:4 years started Dec. 1, 2008

- For more information visit website: http://www.compactmodelling.eu

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# COMON Working Groups

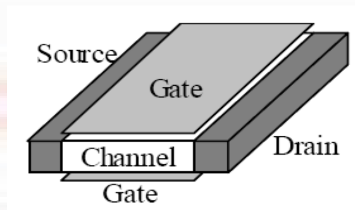
- The COMON Network consists of three Working Groups (WGs). Each WG will address one specific targeted Compact Model (CM) of the semiconductor device. WG is composed of the partners who work on the different Work Packages related to that specific device

- **WG1: Multiple-Gate SOI MOSFETs**
  - UCL, URV, UniK, EPFL, ULP, TUC, ITE, Infineon, AdMOS, AIM-Software
- **WG2: High Voltage MOSFETs**
  - AMS, EPFL, TUC, AdMOS, Dolphin, Melexis, AIM-Software
- **WG3: Advanced III-V HEMTs**
  - TU-Ilmenau, UniK, URV, RFDM , AIM-Software

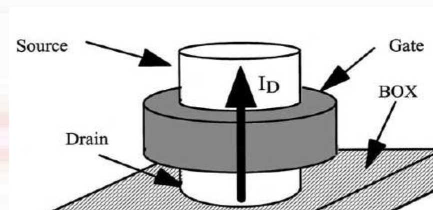
- Annual meetings for every WG will be held to discuss and coordinate the work for each specific device

# Multi-Gate MOSFETs

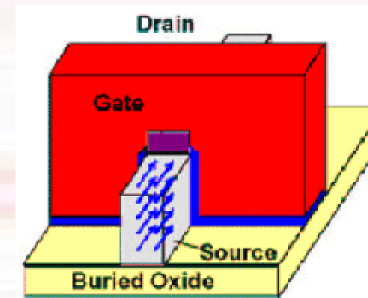
- The non-classical multi-gate devices such as Double-Gate (DG) MOSFETs, FinFETs or Gate-All-Around (GAA) MOSFETs show an even stronger control of short channel effects, and increase of on-currents taking advantage of volume inversion/accumulation.




DG MOSFET

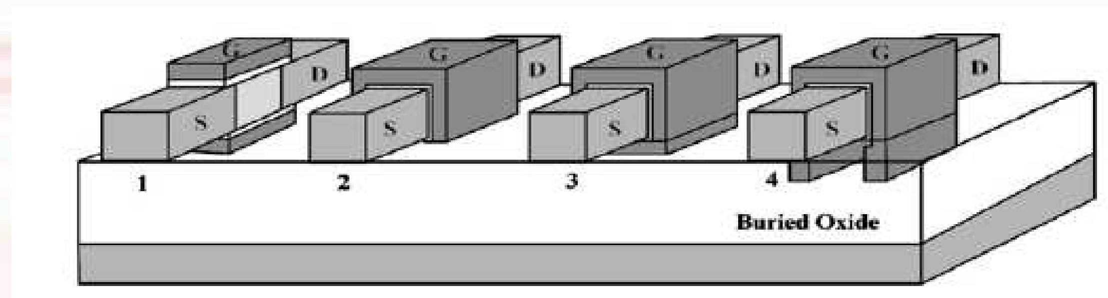



GAA MOSFET




FinFET

# Multi-Gate MOSFETs




*Schematic device structures of MuGFETs:1) double-gate; 2) triple-gate; 3) quadruple-gate; 4) PI-gate*

# 1D Models

The first step to develop a compact model is to consider a well behaved device, with good electrostatic control by the vertical field (from the gate) and where the derivative of the lateral field in the direction of the channel length can be neglected compared to the derivative of the vertical field in the direction perpendicular to the channel.

- This is the gradual channel approximation, and simplifies the electrostatic analysis.
- This leads to neglect the short-channel effects
- In thin-film Multi-Gate MOSFETs, we expect that a long-channel device model can be applied to significantly shorter channels than in standard MOSFETs
- We also have considered an n-channel device, with acceptor doping or with no doping. The hole concentration can be neglected in the normal operation regime.
  - Of course, our analysis can easily be extended to p-channel devices

# 1D models: DG MOSFETs

By integrating the Poisson's equation between the centre (y=0) and the top surface of the film ($y=-t_{si}/2$) we get:

$$E_S(x)=\sqrt{\frac{2qN_A}{\varepsilon_{Si}}}\sqrt{(\phi_s-\phi_0)+\frac{kT}{q}\frac{n_i^2}{N_A^2}e^{\frac{q}{kT}[\phi_s-V(x)]}\left(1-e^{-\frac{q}{kT}(\phi_s-\phi_0)}\right)}$$

where $\phi_S=\phi(x,-t_{Si}/2)$ is the surface potential and $\phi_o=\phi(x,0)$ is the potential in the middle of the film.

Unfortunately, the potential at the center is unknown and we cannot analytically integrated for the potential.

An analytical model is possible with an approximate expression of the difference between the two potentials:

An empirical expression that, using adjustable parameters, fits the entire range of operation

# Modeling Approaches

1) Undoped Multi-Gate MOSFET model, based on a core model derived from the 1D Poisson's equation. Incorporation of short-channel by means ofadditional equations using adjustable parameters.

2) Doped Multi-Gate MOSFET model, based on a core model derived from the 1D Poisson's equation. Incorporation of short-channel by means of additional equations using adjustable parameters.

3) A fully 2D/3D Multi-Gate MOSFET model based on the solution Poisson's equation using conformal mapping

Approaches 1) and 2) lead to a very similar formulation of the drain current and charges and are being unified

# Core (1D) undoped DG MOSFET Model

- An analytical solution is possible in the case of undoped DG MOSFET or cylindrical Surrounding-Gate MOSFETs
- For undoped DG MOSFETs, Poisson's equation:

$$\frac{d^2\psi(x)}{dx^2} = \frac{d^2(\psi(x)-V)}{dx^2} = \frac{q}{\varepsilon_{Si}} \cdot n_i \cdot e^{\frac{q(\psi(x)-V)}{kT}}$$

- The resulting charge control model can be written as:

$$(V_{GS} - V_0 - V) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

# Core (1D) Undoped DG MOSFET Model

- The drain current is obtained as:

$$I_{DS} = \frac{W\mu}{L}\int_0^{V_{DS}} Q(V)\,dV$$

- From the charge control model:

$$dV = -\frac{dQ}{2C_{ox}} - \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+2Q_0}\right)$$

- Where $Q_0 = 4\frac{kT}{q}C_{Si}$

- Finally we get the expression:

$$I_{DS} = \frac{W\mu}{L}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{Si}\log\left[\frac{Q_d + 2Q_0}{Q_s + 2Q_0}\right]\right]$$

# Core (1D) undoped Cylindrical GAA MOSFET Model

- From Gauss law:

$$C_{ox}(V_{GS} - \Delta\varphi - \psi_s) = Q = \varepsilon_{Si} \left.\frac{d\psi}{dr}\right|_{r=R} \quad (4)$$

- Using $\left.\frac{d\psi}{dr}\right|_{r=R} = -\frac{kT}{q}\frac{4BR}{1+BR^2}$ ,the charge control model that is obtained is:

$$(V_{GS} - \Delta\varphi - V) - \frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

- where

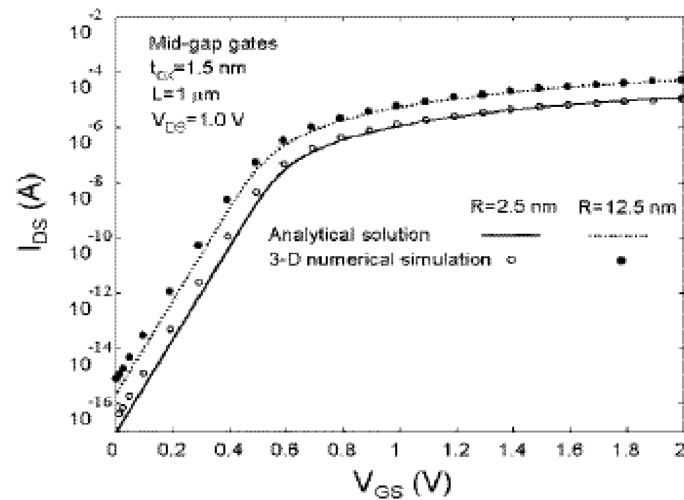
$$Q_0 = \frac{4\varepsilon_{Si}}{R}\frac{kT}{q}$$

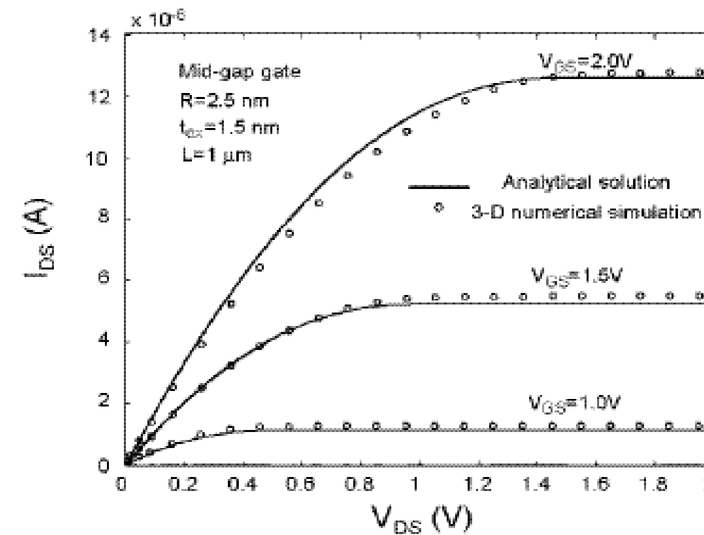
- The drain current is calculated from: $I_{DS} = \mu\frac{2\pi R}{L}\int_0^{V_{DS}} Q(V)dV$

- Using $dV = -\frac{dQ}{C_{ox}} + \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+Q_0}\right)$ we obtain:

$$I_{ds} = \frac{2\pi R}{L}\mu\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kT}{q}Q_0\log\left[\frac{Q_d + Q_0}{Q_s + Q_0}\right]\right]$$

# 1D models: Cylindrical GAA MOSFET

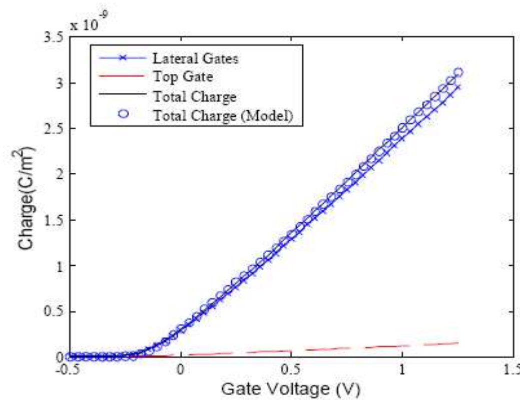



Output and transfer characteristics of cylindrical GAA MOSFETs obtained from the analyticalmodel (solid lines) compared with numerical simulations from DESSIS-ISE® (symbols).

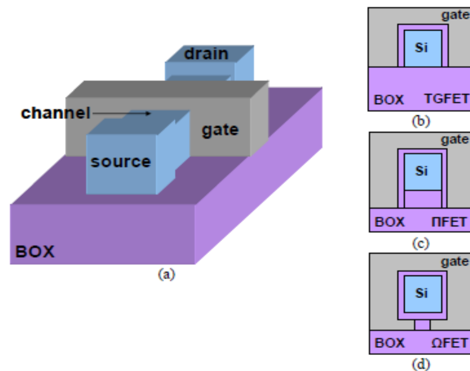
# *1D models: FinFET and Tri-Gate FET*

In general, in symmetric Multi-Gate MOSFETs




$$(V_{GS} - V_0 - V) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

Charge associated to top, lateral and total charge calculated with ATLAS 3-D simulations and with the unified charge control model (FinFET with $W_{fin}$=10 nm, $H_{fin}$=50 nm)




Anyway, a more physical and scalable model is needed, taking also into account the back-bias effects

# Charge modeling

The total channel charge is obtained by integrating the mobile charge density over the channel length.

Capacitances are obtained by differentiating the total charges with respect to the applied voltages.

- In undoped DG MOSFETs:

$$Q_{Tot} = -W\int_0^L Q dx = -W^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 dV$$

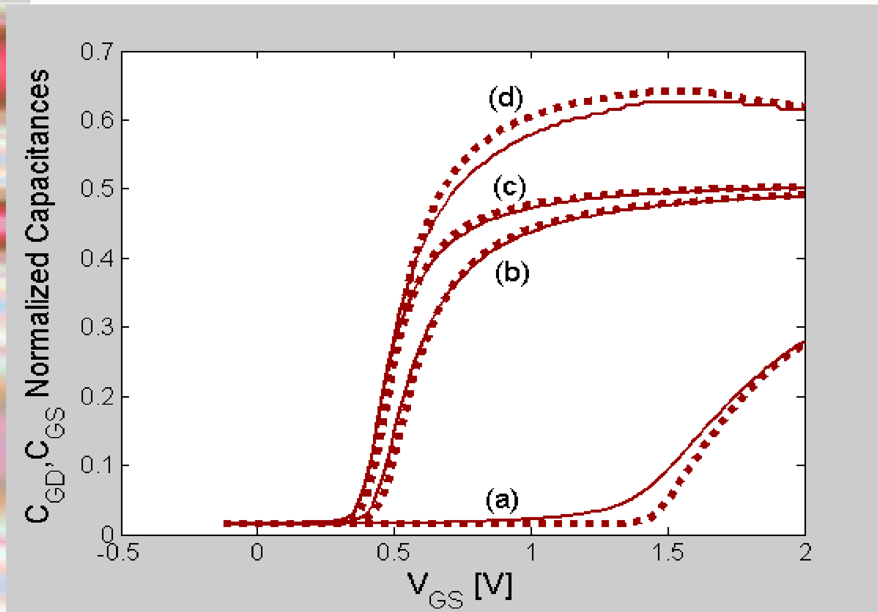
$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left( \frac{Q^2}{2C_{ox}} + \frac{kT}{q} Q + \frac{kT}{q} \frac{Q^2}{Q + 2Q_0} \right) dQ$$

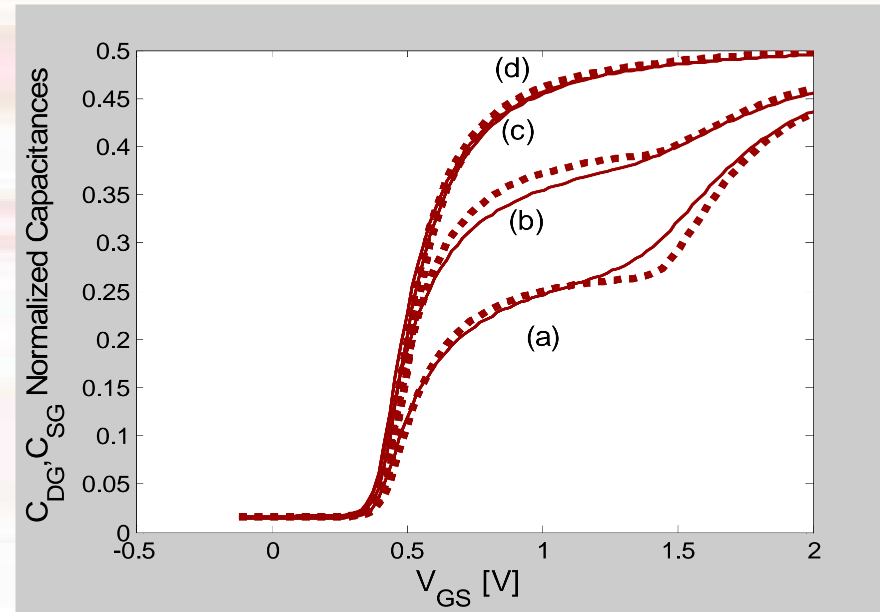
$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \left( \frac{Q^3}{6C_{ox}} + \frac{kT}{q} \frac{Q^2}{2} + 2\frac{kT}{q} \left( -Q_0 Q + \frac{Q^2}{4} + 2Q_0^2 \log\left[2Q_0 + Q\right] \right) \right) \Bigg|_{Q_s}^{Q_d}$$

$$Q_D = -W\int_0^L \frac{x}{L} Q dx = -\frac{W^3 \mu^2}{L(I_{DS})^2} \int_{Q_s}^{Q_d} Q^2 \left( \left( \frac{Q^2 - Q_s^{\,2}}{4C_{ox}} \right) + \frac{kT}{q} \left( 2(Q - Q_s) - 2Q_0 \log\left[ \frac{Q + 2Q_0}{Q_s + 2Q_0} \right] \right) \right) \cdot$$

$$\cdot \left( \frac{1}{2C_{ox}} + \frac{kT}{q} \left( \frac{1}{Q} + \frac{1}{Q + 2Q_0} \right) \right) dQ$$

# Charge modelling: symmetric DG MOSFET

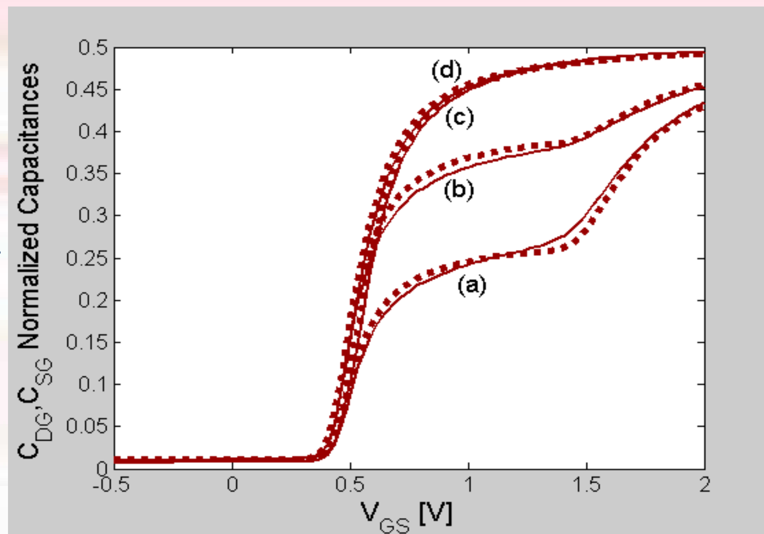


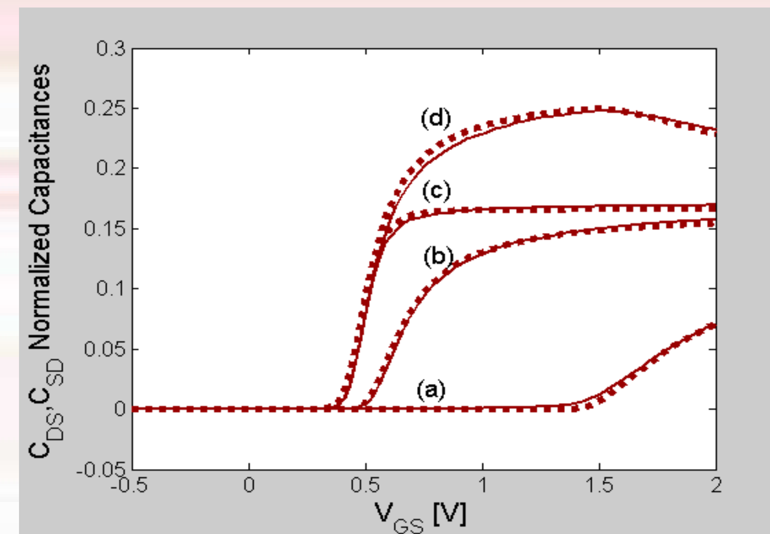

**Normalized gate to drain capacitance (a, b) and gate to source capacitance (c, d) with respect to the gate voltage, for $V_{DS}$=0.05V (b,c) and $V_{DS}$=1V (a,d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model**

**Normalized drain to gate capacitance (a, c) and source to gate capacitance (b, d) with respect to the gate voltage, for $V_{DS}$=1V (a, b) and $V_{DS}$=0.05V (c, d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model**

# *Charge modelling: GAA MOSFETs*




Normalized drain to gate capacitance (a, c) and source to gate capacitance (b, d) with respect to the gate voltage, for $V_{DS}$=1V (a, b) and $V_{DS}$=0.1V (c, d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model



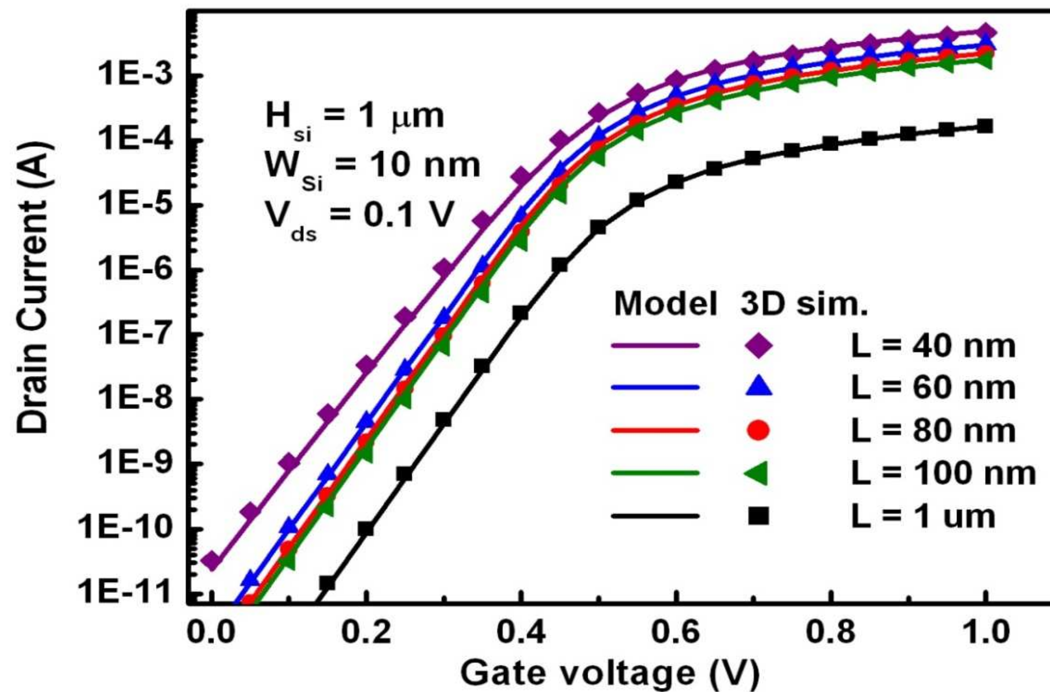

Normalized drain to source capacitance (c,d) and source to drain capacitance (a, b) with respect to the gate voltage, for $V_{DS}$=1V (a, d) and $V_{DS}$=0.1V (b, c). Solid line: DESSIS-ISE simulations; Symbol line: analytical model

# *Improved Undoped Multi-Gate MOSFET Model: Short-Channel Effects*

## Validity of the extended model:

Gate length (L): down to 25 nm
Silicon width ($W_{Si}$): down to 3 nm
Silicon height ($H_{Si}$): down to 50 nm
Channel doping ($N_a$): intrinsic to $10^{17}$ $cm^{-3}$
nMOS and pMOS

# Improved Undoped Multi-Gate MOSFET Model:

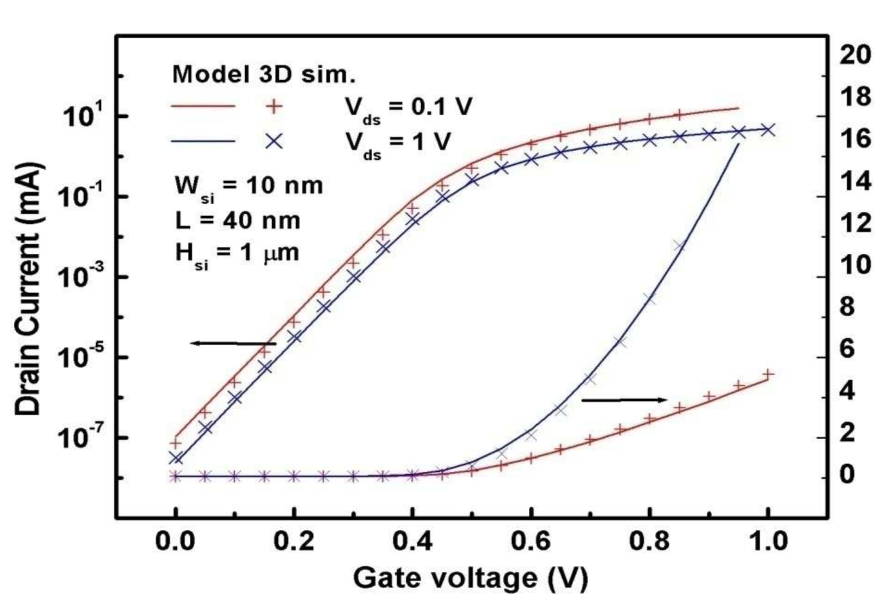


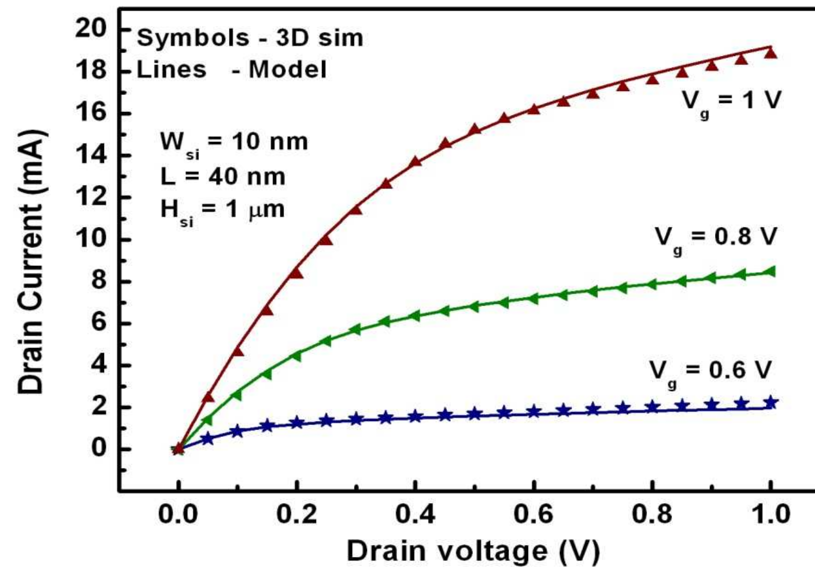

*Drain [...] s.*

*The above figure is w/o QME and with a constant mobility.*

*Lines: compact model; symbols: TCAD simulations.*

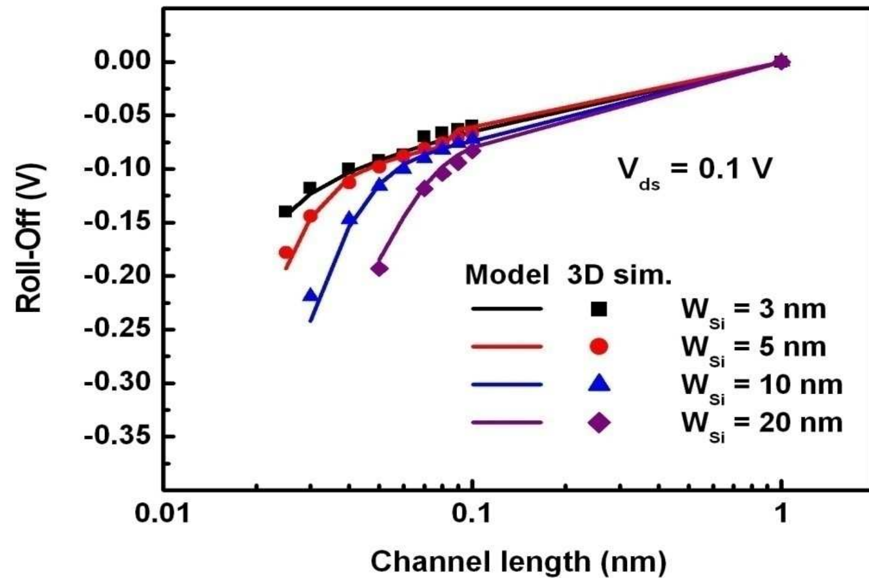
# Improved Undoped Multi-Gate MOSFET Model:

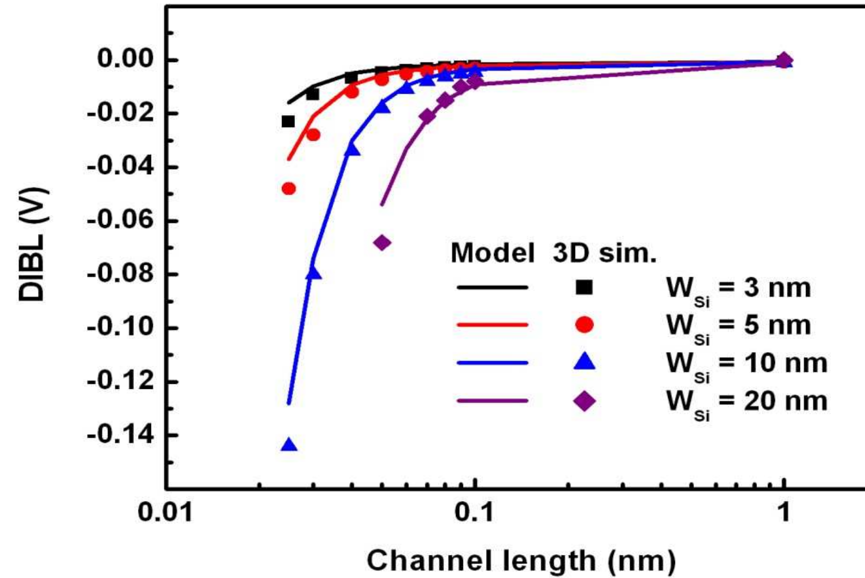



*Lines: compact model; symbols: TCAD simulations.*
*The above figures are w/o QME and with a constant mobility.*

# *Improved Undoped Multi-Gate MOSFET Model*

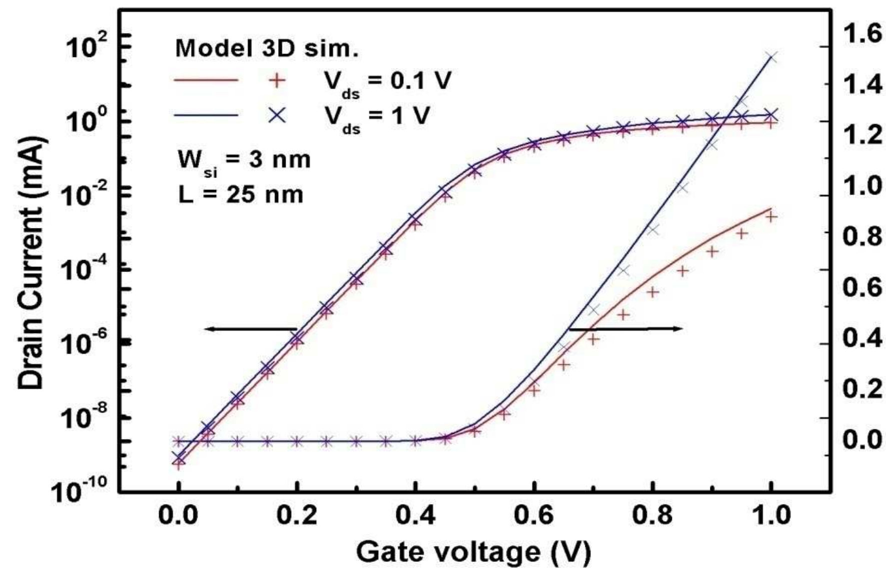


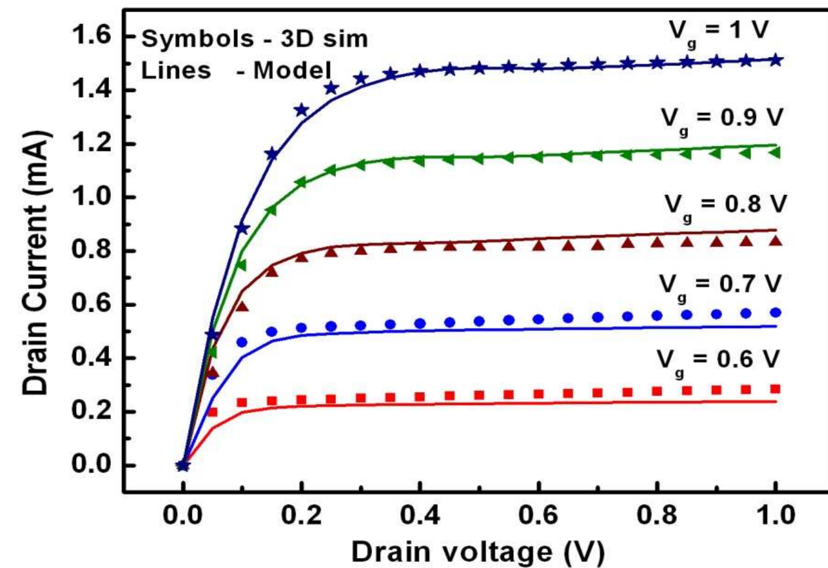




*Influence of the channel width WSi on both roll-off and DIBL. A thinner silicon film is desirable to limit short-channel effects. However, let us note that quantum effects play a major role for WSi < 10 nm.*

*QME are not accounted for in the above figures in order to focus only on SCE.*

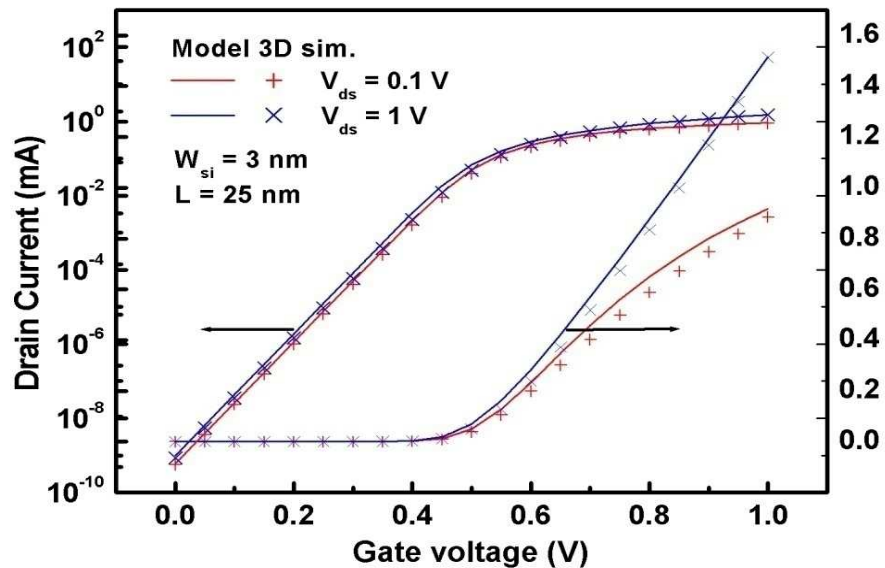
# Improved Undoped Multi-Gate MOSFET Model

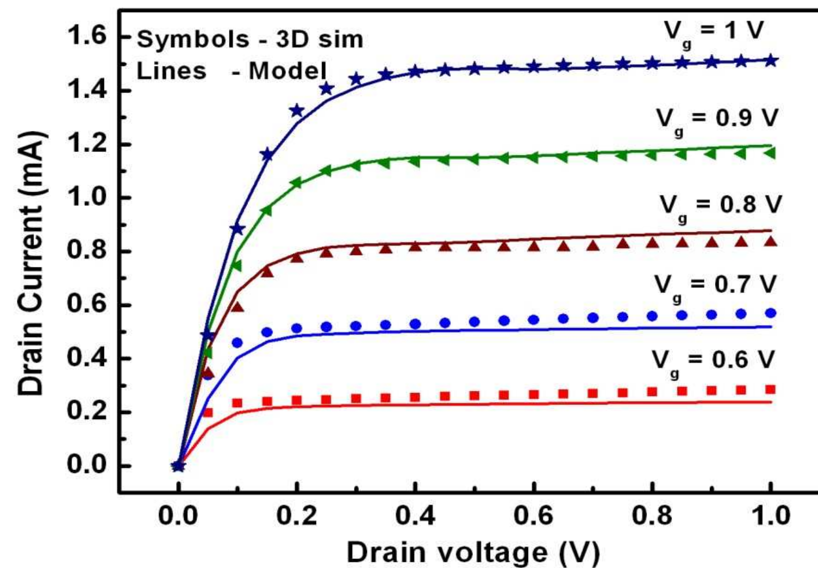



*Drain current for an ultrashort and ultrathin device: L = 25 nm and WSi = 3 nm.*
*QME are not accounted for here in order to focus only on mobility reduction.*
*Lines: compact model; symbols: TCAD simulations with CVT mobility model.*

# Improved Undoped Multi-Gate MOSFET Model




*Drain current for an ultrashort and ultrathin device: L = 25 nm and WSi = 3 nm.*
*QME are not accounted for here in order to focus only on mobility reduction.*
*Lines: compact model; symbols: TCAD simulations with CVT mobility model.*

# Core (1D) doped DG MOSFET model - Calculation of $\phi d=\phi s-\phi o$ in all regions

1) Below threshold region $\phi d_1 = \phi d_{BT} + 1.19\phi t \left[ \frac{e^{\frac{V_G - V_T - V}{1.1\phi t}}}{1 + e^{\frac{V_G - V_T - V}{1.1\phi t}}} \right]$

2) Above threshold region for $V \le V_M = 2,\ \phi_M$ can be empirically expressed as:

$$\phi d_M = 0.197 - 0.047\, t_{ox} + 0.0045\, t_{ox}^2 + 0.00418\, t_s - 3 \cdot 10^{-5}\, t_s^2;$$

For Na < $Na_{max}$
$$\phi d_{2a} = \left( \frac{\phi d_{BT}}{3} + \phi d_M - 0.042\, V \right) - \left( \frac{\phi d_{BT}}{3} + \phi d_M - 0.042\, V - \phi d_T \right) \left( \frac{1 - \frac{V_G - V_T - V}{V_M - V_T - V}}{1 + 1.357\,(V_G - V_T - V)} \right)$$

For Na > $Na_{max}$
$$\phi d_{2b} = \left( \frac{\phi d_{BT}}{2} + \phi d_M - 0.042\, V \right) - \left( \frac{\phi d_{BT}}{2} + \phi d_M - 0.042\, V - \phi d_T \right) \left( \frac{1 - \frac{V_G - V_T - V}{V_M - V_T - V}}{1 + 0.5(V_G - V_T - V)} \right)$$

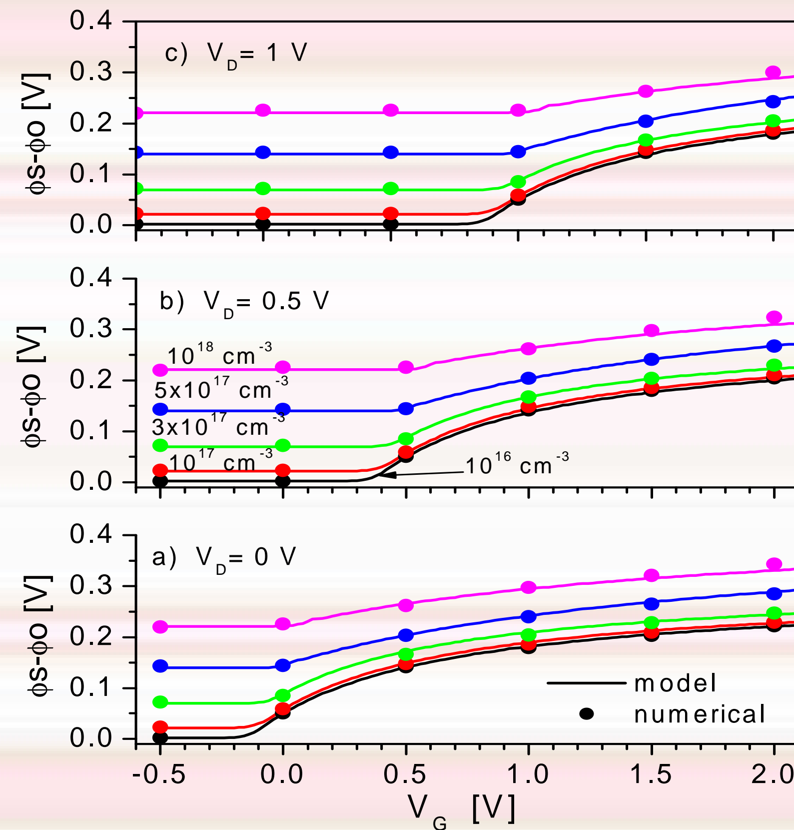
## In all regions for above threshold conditions:

$$\phi d_2 = \frac{\phi d_{2a}}{2} \left[ 1 - \tanh\left[ 10\left( \log(Na) - \log(Na_{max}) - 0.5 \right) \right] \right] + \frac{\phi d_{2b}}{2} \left[ 1 + \tanh\left[ 10\left( \log(Na) - \log(Na_{max}) - 0.5 \right) \right] \right]$$

**General expression for $\phi d$**

$$\phi d = \frac{\phi d_1}{2} \left[ 1 - \tanh\left[ 30(V_G - V_T - V) \right] \right] + \frac{\phi d_2}{2} \left[ 1 + \tanh\left[ 30(V_G - V_T - V) \right] \right]$$

# Core doped DG MOSFET model - Calculation of $\phi d=\phi s-\phi o$ in all regions



# Core doped DG MOSFET model - Calculation of surface potentials

$\phi s_{bt}$ approximation below threshold

$$\phi s_{bt} = V_G - V_{FB} - \phi t \frac{q_b}{2} - \phi t \cdot LambW\left[\frac{q_b}{4} e^{\frac{V_G - V_{FB} - 2\phi_F - \phi t \frac{q_b}{2}}{\phi t}}\right]$$

$\phi s_{at}$ approximation above threshold

$$\phi s_{at} = V_G - V_{FB} - 2\phi t \cdot LambW\left[\frac{1}{2}\sqrt{\frac{q_b}{2}\frac{1}{\gamma}}\sqrt{1 - e^{-\alpha}}\, e^{\frac{V_G - V_{FB} - 2\phi_F - V}{2\phi t}}\right]$$

Surface potential

$$\phi s = \frac{\phi s_{bt}}{2}\left[1 - \tanh\left[20 \cdot \left(V_G - V_T\right)\right]\right] + \frac{\phi s_{at}}{2}\left[1 + \tanh\left[20 \cdot \left(V_G - V_T\right)\right]\right]$$

# Core doped DG MOSFET Model: Charge Control Model

The general expression for the **Charge Control Model** is obtained:

$$V_G - V_{FB} - 2\phi_F - V - \phi t \frac{q_b}{2} + \phi t \ln\left(\frac{1-e^{-\alpha}}{\alpha}\right) = \phi t\, q_n + \phi t \ln\left[\frac{\alpha_{BT}}{\alpha}\left(\frac{4q_n}{q_b}\cdot\left(1+\frac{q_n}{q_b}\right)+1\right)-1\right]$$

$$\frac{\alpha_{BT}}{\alpha}\left(\frac{4q_n}{q_b}\cdot\left(1+\frac{q_n}{q_b}\right)+1\right) >> 1$$

Approximation valid for Na from $10^{14}$ to $3\text{x}10^{18}$ $cm^{-3}$

The derivative with respect to *V* is equal to:

$$-1+\frac{d}{dV}\left[\phi t \ln\left(\frac{1-e^{-\alpha}}{\alpha}\right)\right] = \phi t\left[1+\frac{1}{q_n}+\frac{1}{q_n+q_b}\right]\frac{dq_n}{dV} + \phi t \frac{d}{dV}\left[\ln\left(4\frac{\alpha_{BT}}{\alpha}\right)\right]$$

After neglecting the *ln* terms

$$dV = -\phi t\left[1+\frac{1}{q_n}+\frac{1}{q_n+q_b}\right]\cdot dq_n \qquad dV_G = \phi t\left[1+\frac{1}{q_n}+\frac{1}{q_n+q_b}\right]\cdot dq_n$$

# Core Doped DG MOSFET ModelCharge Control Model - Drain current

Total drain current considering both surfaces

$$I_{DS} = 2\frac{W}{L}\mu C_{ox}\phi t\int_{V_S}^{V_D} q_n(V)\,dV$$

## Long channel and $\mu = const$

Using the relation between $V$ and $q_n$ the following expression for total current is obtained:

$$I_{DS} = I_0\left[\frac{q_{ns}^2 - q_{nd}^2}{2} + 2(q_{ns} - q_{nd}) - q_b \ln\left(\frac{q_{ns} + q_b}{q_{nd} + q_b}\right)\right]$$

Where $I_0$ is equal to:

$$I_0 = 2\frac{W}{L}\mu_0 C_{ox}\phi t^2$$

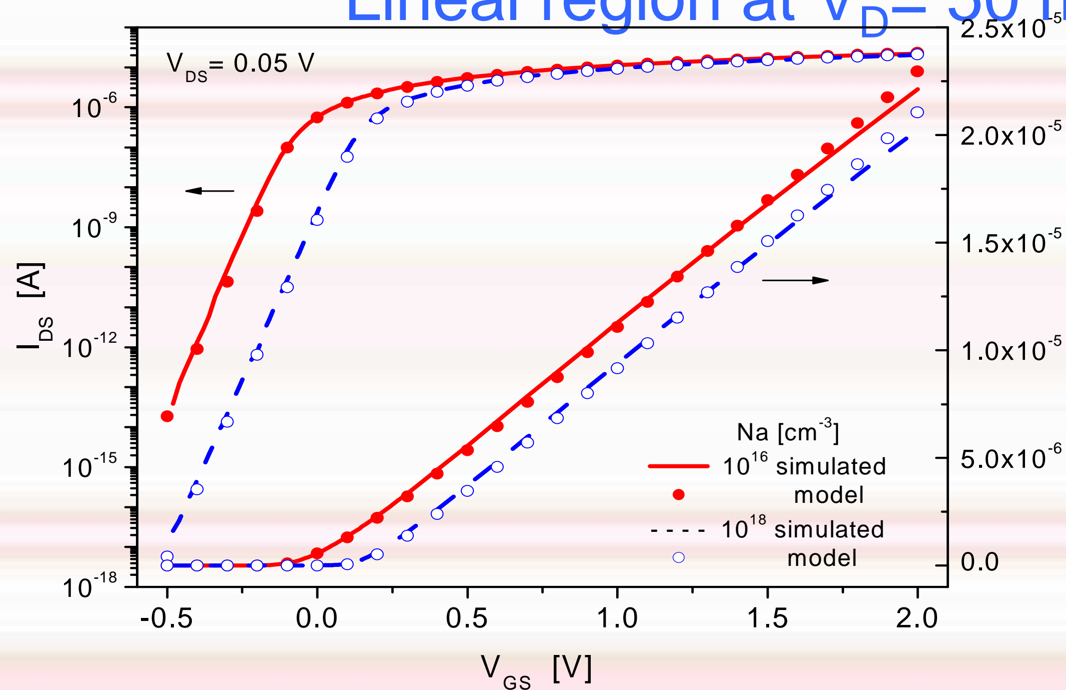
## *Current model validation*

L= 5 μm

μ= 400 $cm^2/Vs$

Comparison of modeled and simulated transfer characteristics

Lineal region at $V_D$= 50 mV

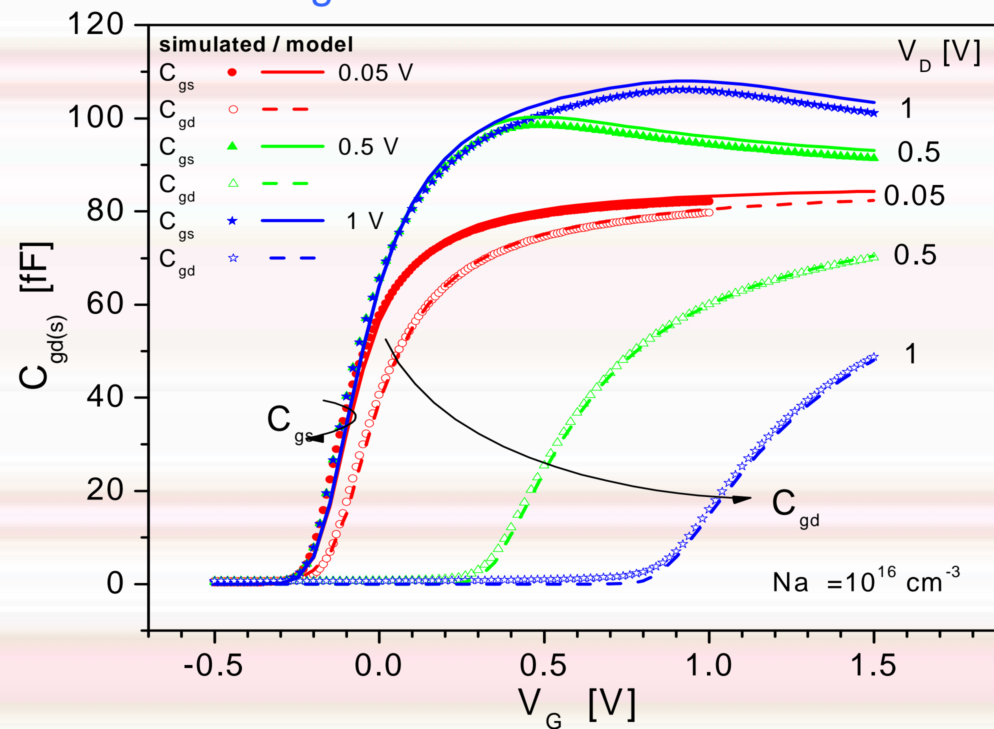


# *Capacitance model*

L= 5 μm

μ= 400 cm²/Vs

Modeling of $C_{gd}$ and $C_{gs}$



## *Doped DG MOSFET Model with variable mobility and short channel effects*

### INTRODUCTION OF SHORT-CHANNEL EFFETS (SCE) IN THE CORE MODEL

- Variable mobility considering transversal and longitudinal electric fields
- Short channel effects (SCE) taken into acount:
  - $V_T$ variation with channel length reduction and DIBL;
  - Velocity saturation effects;
  - Series resistance;
  - Channel shortening;
  - Subthreshold slope degradation

# Doped DG MOSFET Model: Short Channel Effects – Drain current

Effect of series resistance *R* as function of the external voltages.

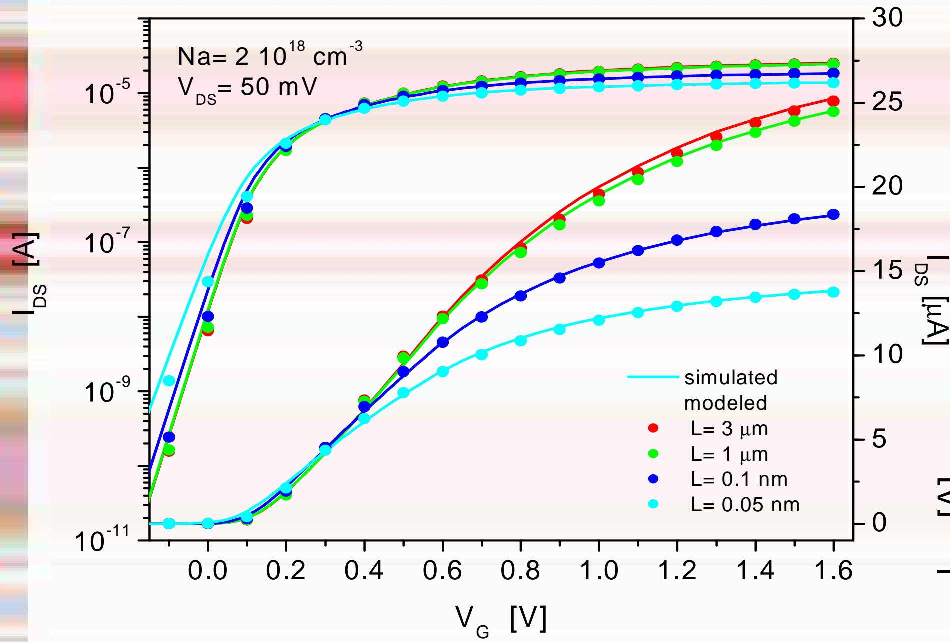
$$I_D \propto \frac{1}{1+\left[2\frac{W}{L}C_{ox}\mu_{eff}\cdot R\cdot\left|V_{GT}-\beta\cdot V_{Def}\right|\right]\cdot\frac{1}{2}\left[1+\tanh\left(60\cdot V_{GT}\right)\right]}$$

$$I_D = \frac{\left(2\frac{W}{L}C_{ox}\phi t^2\mu_{eff}\right)}{\left(1-\frac{\Delta L}{L}\right)}\frac{\left[\frac{1}{2}\left(q_{ns}^2-q_{nd}^2\right)+\left[2\left(q_{ns}-q_{nd}\right)-q_b\ln\left(\frac{q_{ns}+q_b}{q_{nd}+q_b}\right)\right]^n\right]}{1+\left[2\frac{W}{L}C_{ox}\mu_{eff}\cdot R\cdot\left|V_{GT}-\beta\cdot V_{Def}\right|\right]\cdot\frac{1}{2}\left[1+\tanh\left(60\cdot V_{GT}\right)\right]}$$

$$q_{ns} = q_n(V_G+\Delta V_T, V=0) \qquad q_{nd} = q_n(V_G+\Delta V_T, V=V_{efs})$$

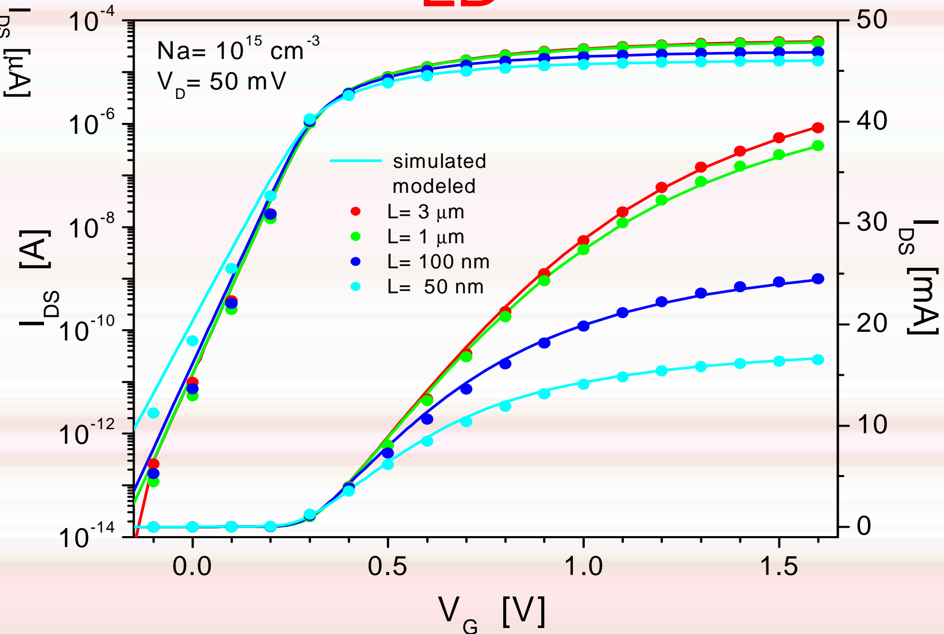
# Doped DG MOSFET Model: Short channel model validation

HD




Simulated and modeled transfer characteristics at $V_D = 50$ mV

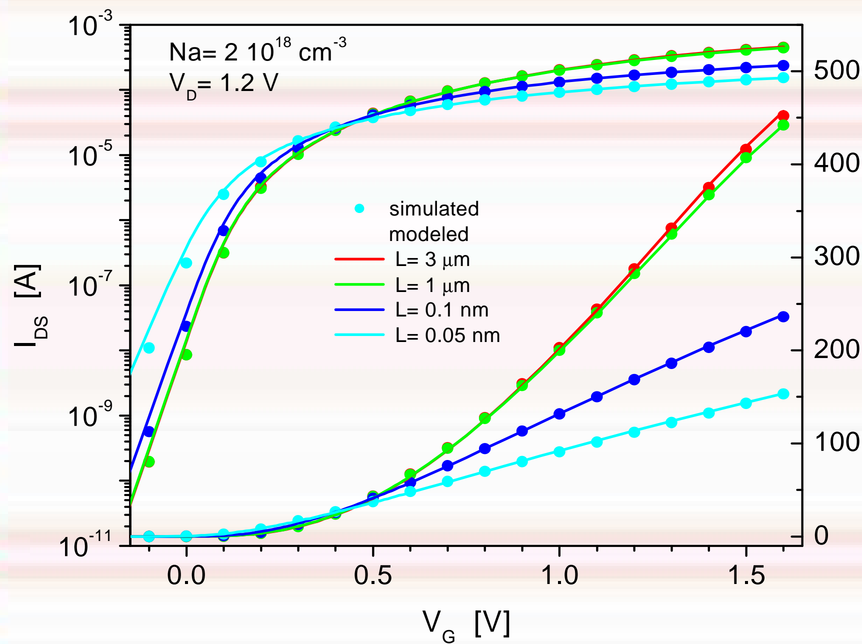
LD



# *Doped DG MOSFET Model: Short channel model validation:*

Simulated and modeled transfer characteristics at $V_D$= 1.2 V

HD

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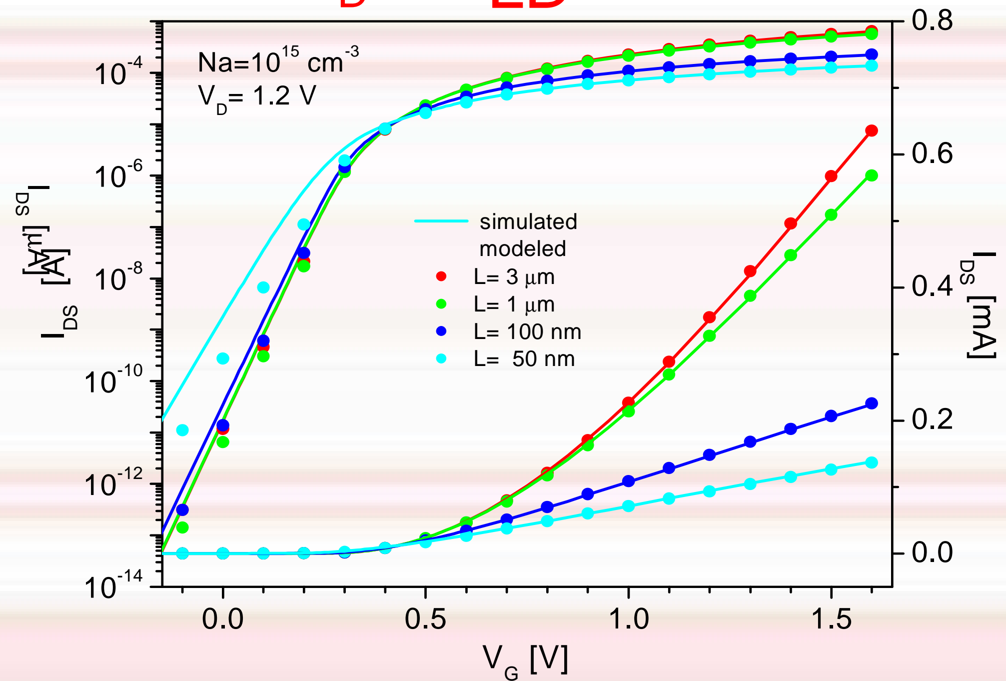
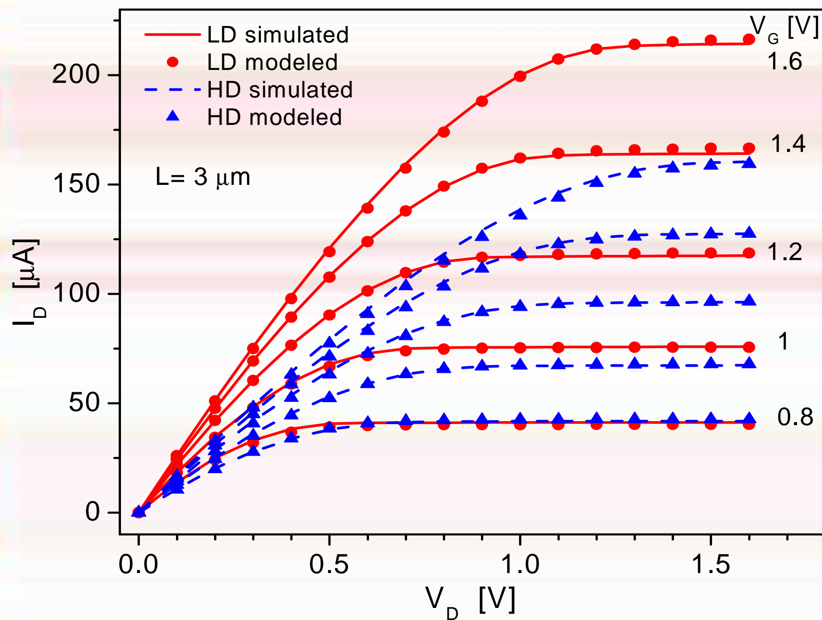


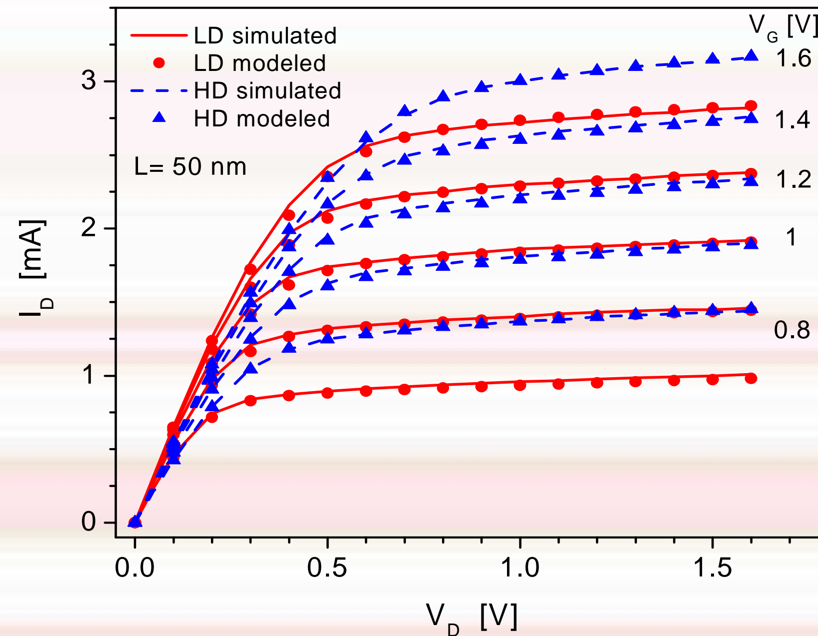
# Doped DG MOSFET Model: Short channel model validation




Simulated and modeled output characteristics at $V_G$= 0.8; 1;1.2; 1.4; 1.6 V

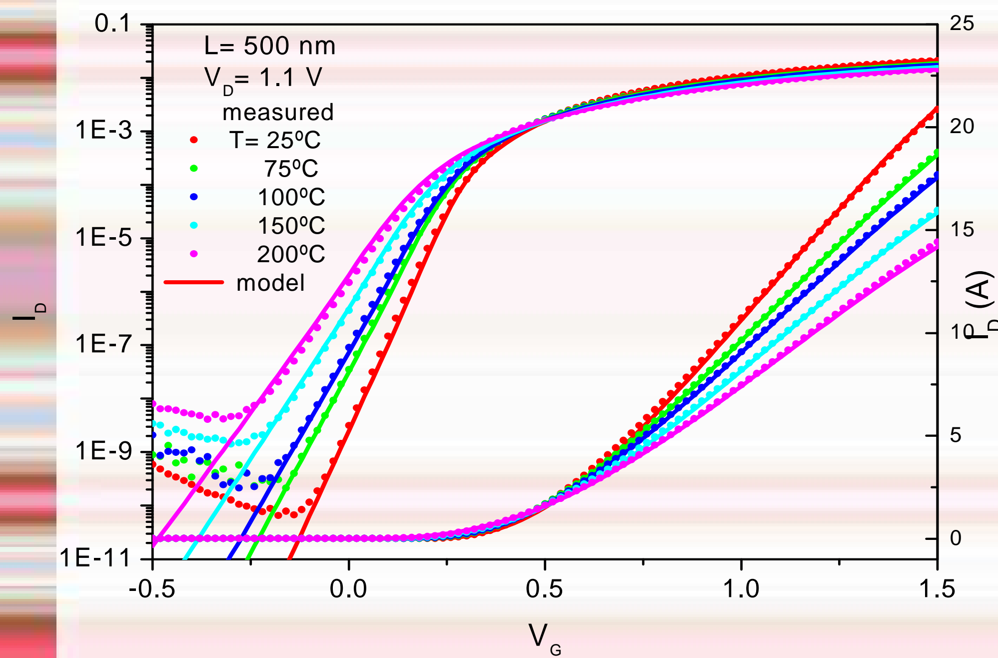
L= 3 µm

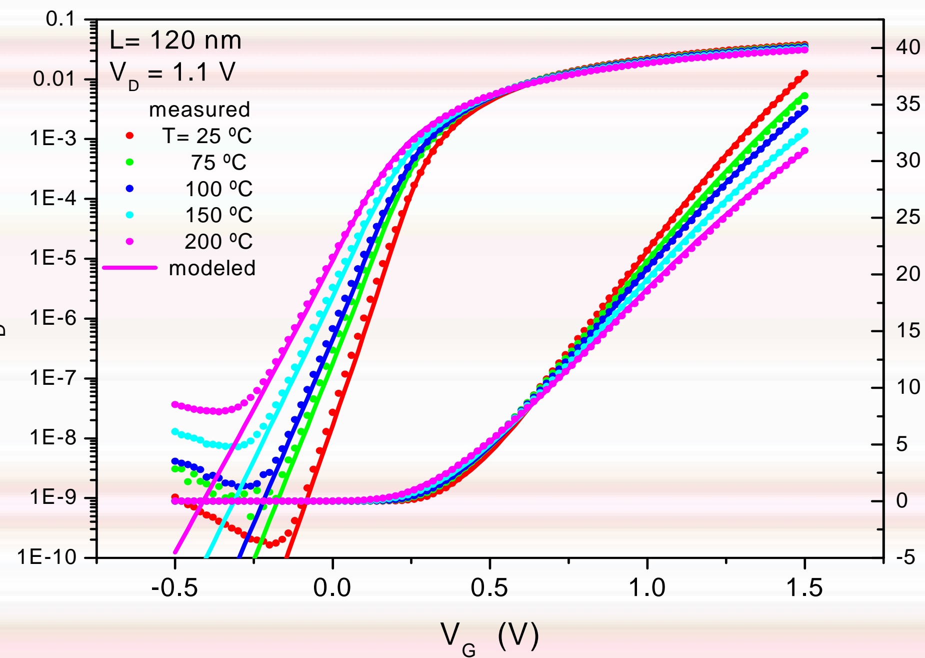
L= 50 nm



# Doped DG MOSFET Model:Measured and modeled transfer characteristics at 1.1 V

## T = 20, 75, 100, 150 and 200 ℃



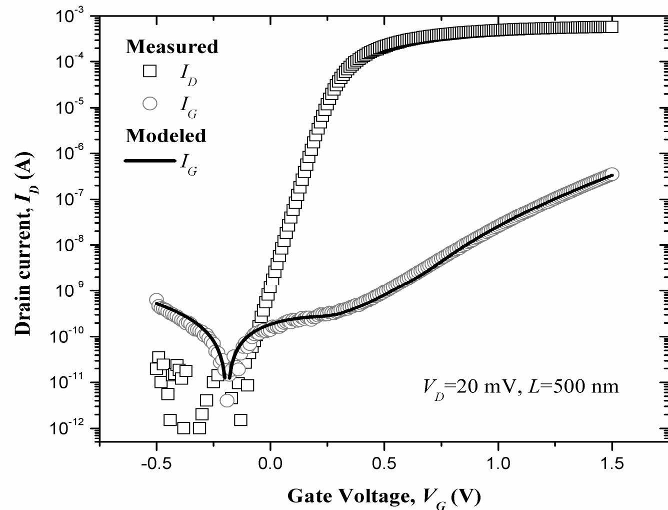



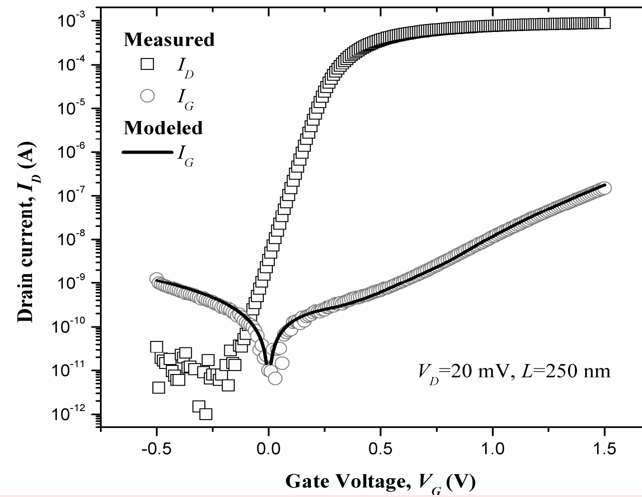
# DG MOSFET: Gate Current

Comparison of calculated gate current and measured for FinFETs.

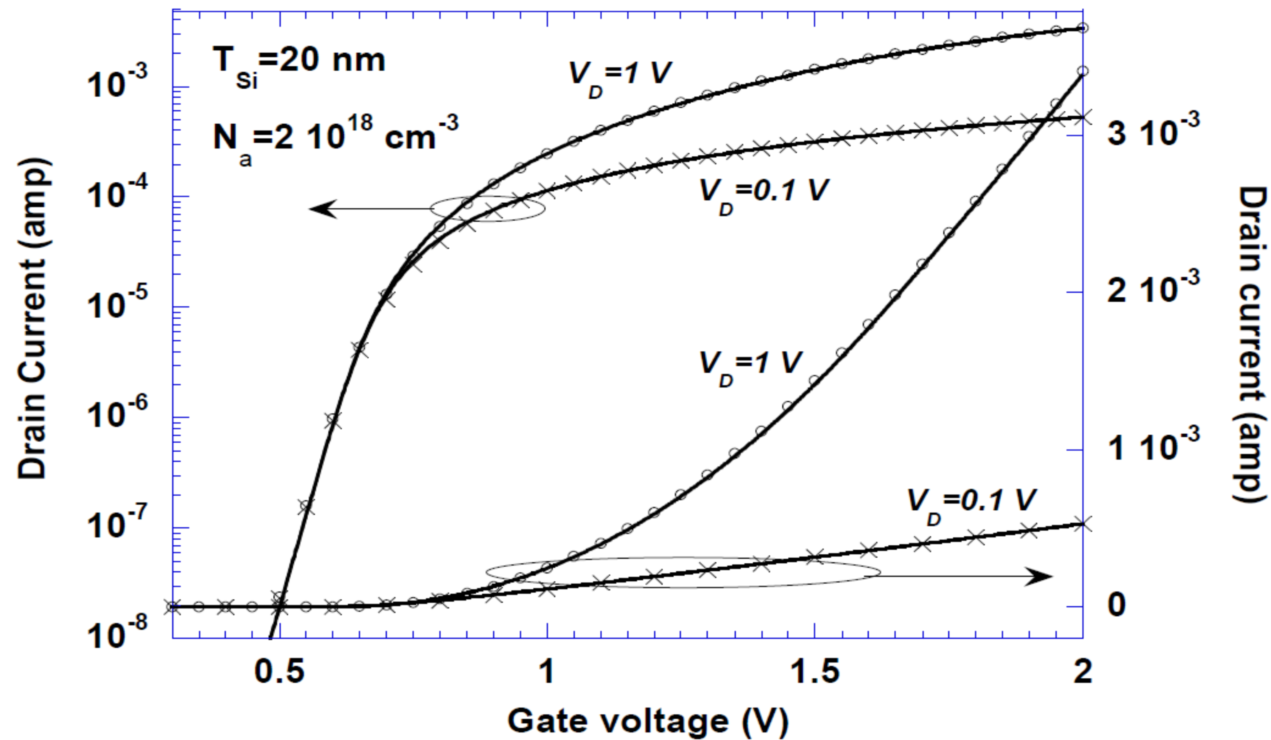
| Channel Length (nm) | Applied $V_D$ (V) | Tunneling Parar | | Fitting Parame | | | |
|---|---|---|---|---|---|---|---|
| | | $t_{pi}$ (nm) | $\varphi_{bECB}$ (eV) | $m_{iECB}$ (kg) | $\Delta V_G$ (V) | $\alpha_{ECB}$ | $\Delta V_{FB}$ (V) |
| 500 | 0.02 | 2.37 | 3.04 | $0.44\times m_0$ | +0.19 | 0.6 | 1.09 |
| | 1.1 | 2.37 | 3.04 | $0.44\times m_0$ | +0.12 | 1.0 | 1.3 |
| 200 | 0.02 | 2.3 | 3.04 | $0.44\times m_0$ | 0 | 0.9 | 1.22 |
| | 1.1 | 2.3 | 3.04 | $0.44\times m_0$ | -0.12 | 2.0 | 1.27 |

Linear region



# Undoped-Doped DG MOSFET: Unified Formulation




*Drain current versus gate voltage in linear and saturation regimes for a long channel device (1 µm).*

*Lines: compact model; symbols: TCAD simulations.*

# 2D/3D Multi-Gate MOSFET Modeling

***Objectives:***

- Establish unified analytical models for nanoscale MugFETs (multigate MOSFETs) including FinFET and GAA devices

***Procedure :***

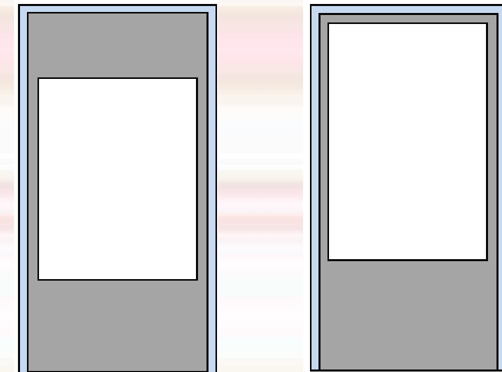
- Decompose Poisson's equation into a Laplace equation and a residual Poisson's equation (superposition principle)

***Capacitive inter-electrode effects***

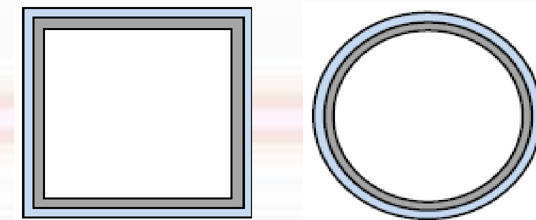
- From 2D/3D Laplace equation determine potential distribution associated with capacitive inter-electrode coupling.
- Use this to calculate *subthreshold* electrostatics, drain current and capacitances

***Near and above threshold***

- Apply residual Poisson's equation, boundary conditions, and modeling expressions to determine *self-consistent* device properties



**Schematic representation of 2D cut-plane of DG FinFET and trigate FinFET respectively**



**Schematic representation of 2D cut-plane of quad- and cylindrical GAA devices respectively**

# 3D GAA MOSFETs Modeling

## Long-channel electrostatics

Potential distribution in the central parts of the device is modeled as (non-parabolic term in x and y included)

$$\hat{\varphi}(x,y,z)=\hat{\varphi}(0,0,z)\left\{\alpha\left[1-\left(\frac{2r}{a}\right)^{2}\right]+\beta\left[1-\left(\frac{2r}{a}\right)^{4}\right]\right\}$$ CirG

$$\hat{\varphi}(x,y,z)=\hat{\varphi}(0,0,z)\left\{\alpha\left[1-\left(\frac{2x}{a}\right)^{2}\right]\left[1-\left(\frac{2y}{a}\right)^{2}\right]+..\right\}$$ SqG

Apply to 3D Laplace equation, solution along source-drain symmetry axis

$$\hat{\varphi}(0,0,z)=\frac{\left(V_{bi}-V_{gs}+V_{FB}\right)\sinh\left(\frac{L-z}{\lambda}\right)+\left(V_{bi}+V_{ds}-V_{gs}+V_{FB}\right)\sinh\left(\frac{z}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$$

Similar procedure for rectangular gate device (RecG).

## Potential distribution near source and drain

1D Laplace solution near source and drain (flattening of (*x*,*y*) potential distribution) is modeled by introducing a *z*-dependent equipotential region that tapers off within distance λ of S and D (grey area indicated in figure)

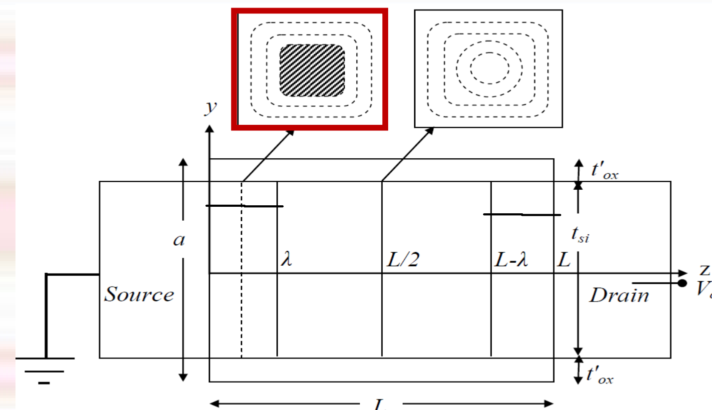
## Short-channel electrostatics

- Non-parabolic adjustment applied in the (*x*,*y*) potential profiles affects the solution along the symmetry axis.

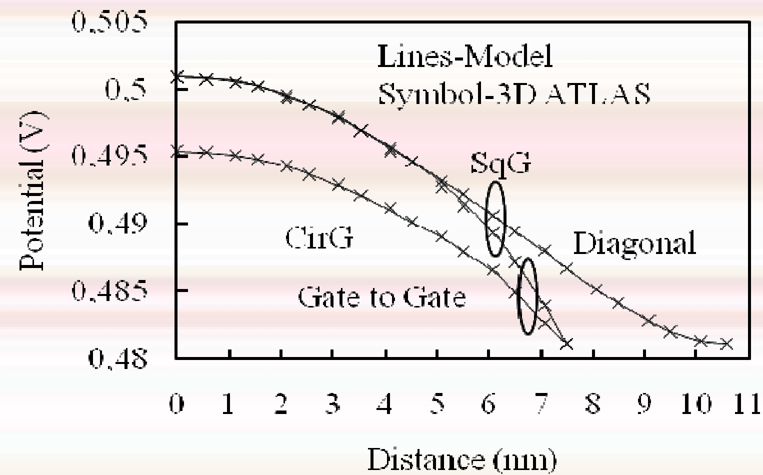
**Remedy**

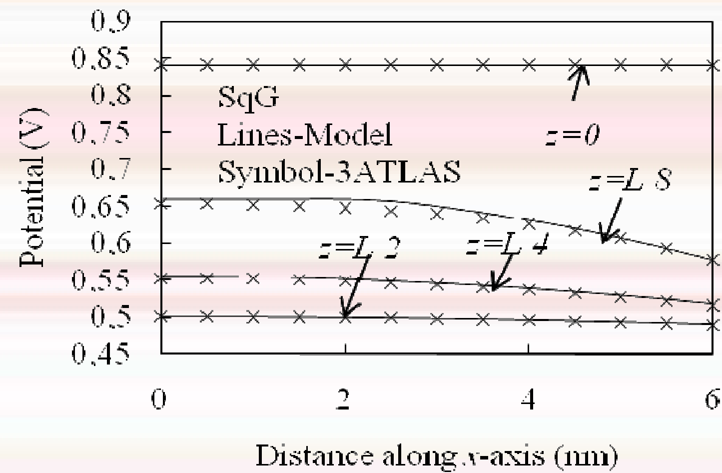
- Introduce precise auxiliary boundary conditions derived from conformal mapping techniques:
  - Potential at device center
  - E-field at source and drain
- Introduce *z*- dependent scale length λ to fit new boundary conditions

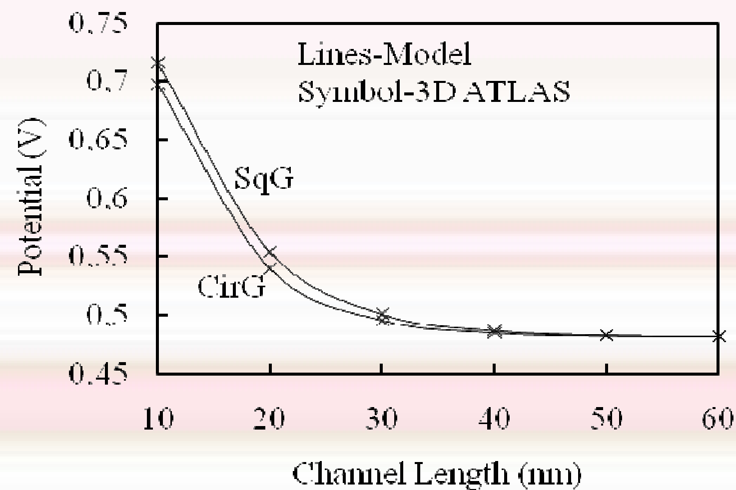
$$\lambda(z)=\lambda_{c}+\alpha\left(z-\frac{L}{2}\right)^{2}$$

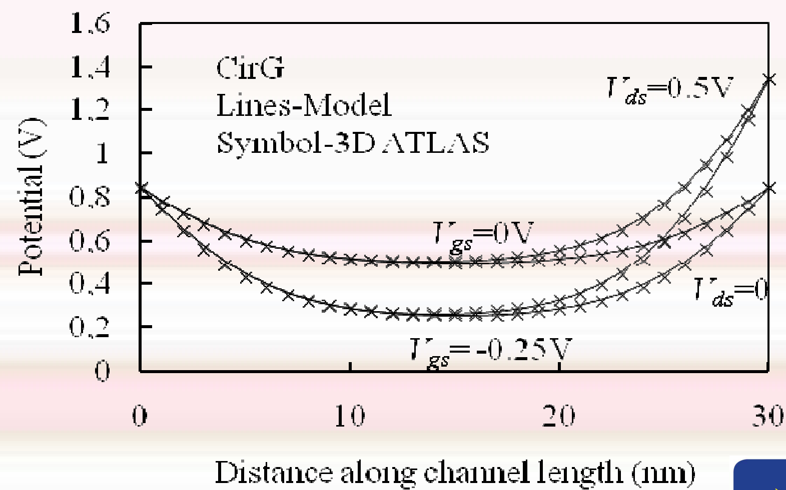


# 3D GAA MOSFETs (modeling results)



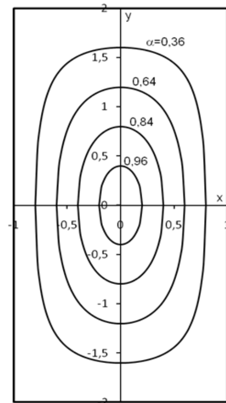
# FinFET Modeling

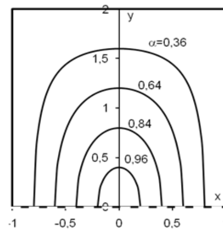
## Trigate FinFET

The modeling of the trigate FinFET is based on the observation that this structure is a symmetric half of a rectangular GAA device.

### *Remedy to correct electrostatics*

- *Use results from RecG devive (rectangular GAA) to obtain ground plane potential distribution of trigate FinFET*
- *Model the center plane of trigate FinFET, which corresponds to* $H_{rec}$/4 above the center plane of the rectangular GAA device with an adjusted scaling length $\lambda$



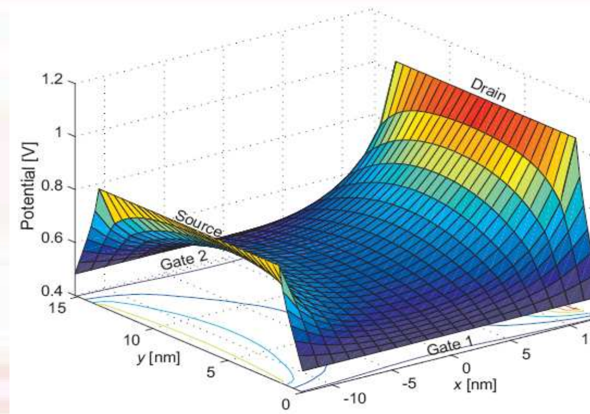




Equipotential contours in (x,y) cross sections of a rectangular GAA MOSFET and the corresponding trigate MOSFET

## DG (double gate) FinFET

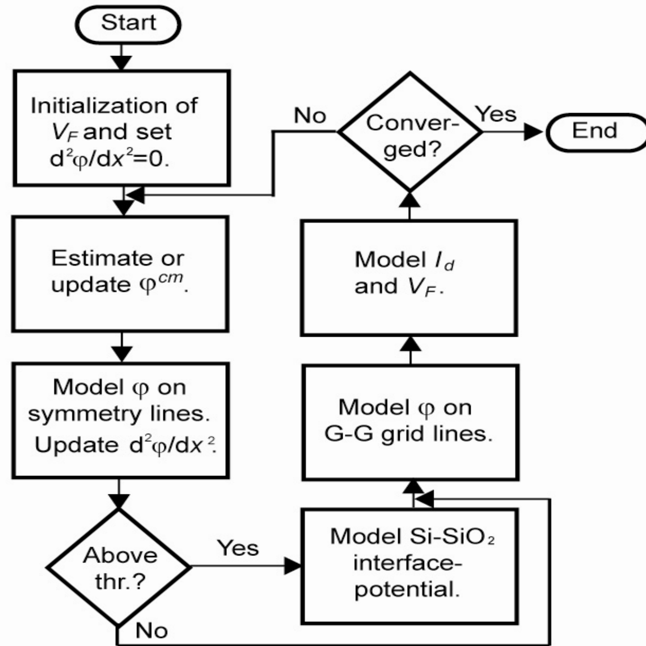
IIn case of DG FinFETs, the height to width ratio is quite large and the top electrode is separated from the channel by a thick oxide, hence the variation of potential along the fin height is negligible

*A 2D solution can thus be directly extended to 3D device*




2D potential distribution in double-gate device at $V_{GS} = V_{DS} = 0.2$ V

# Near-threshold and Strong Inversion Modeling




***The iterations are computationally efficient!***

***In strong-inversion, the device attains long channel behavior, and can be modeled with 1D Poisson's solutions***

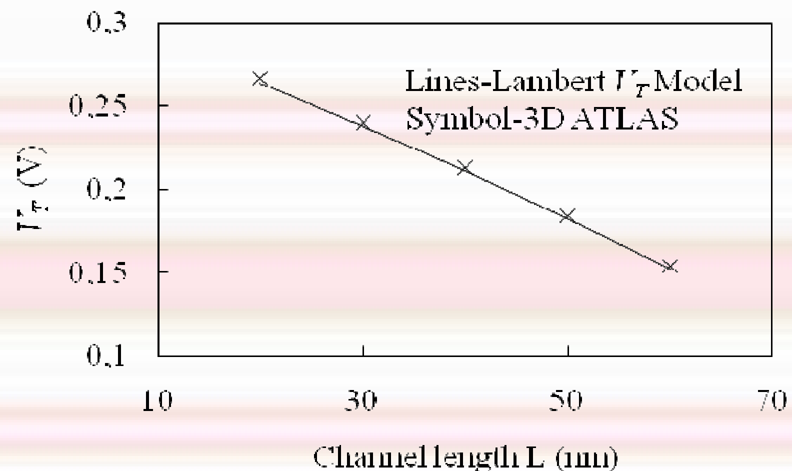
***Transition (threshold) voltage*** $(V_{DS}=0V)$:

**Defined as the gate voltage for which center G-G potential becomes flat– pseudo flatband condition**

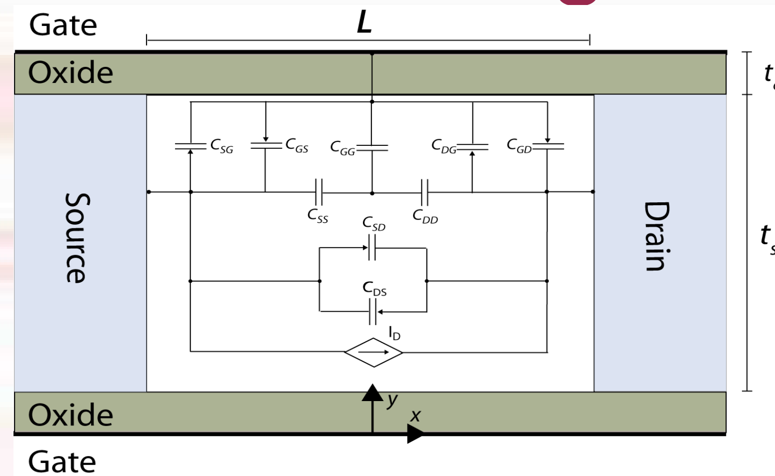
**Unified equation for transition voltage:**

$$\frac{V_{bi}-V_T+V_{FB}}{V_{th}}\exp\left(\frac{V_{bi}-V_T+V_{FB}}{V_{th}}\right)=\beta\left(\frac{V_{bi}}{V_{th}}\right)$$

$\beta$ **is a physical parameter dependent on device dimensions**



# Capacitance modeling




GAA and symmetric DG devices described by 9 trans- and self-capacitances $C_{XY}$, of which 4 are independent

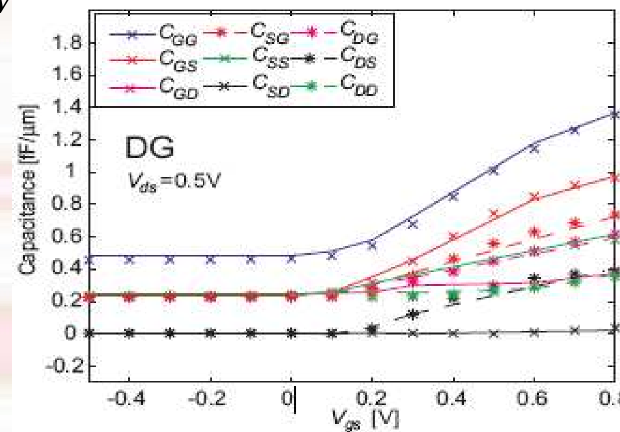
$C_{XY}$ reflects the change of charge $Q_X$ associated with electrode X due to a small variation in the terminal voltage $V_Y$:

$$C_{XY} = \pm \frac{\partial Q_X}{\partial V}$$

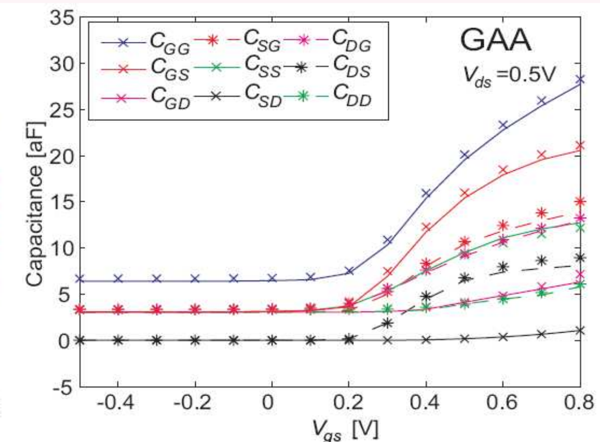
From symmetry and charge conservation at subthreshold:

$$C_{gs} = C_{gd} = C_{sg} = C_{dg} = C_{gg}/2$$

$$C_{ds} = C_{sd} \qquad C_{ss} = C_{dd} = C_{gs} + C_{ds}$$




Variation of intrinsic capacitance in DG device with gate voltage



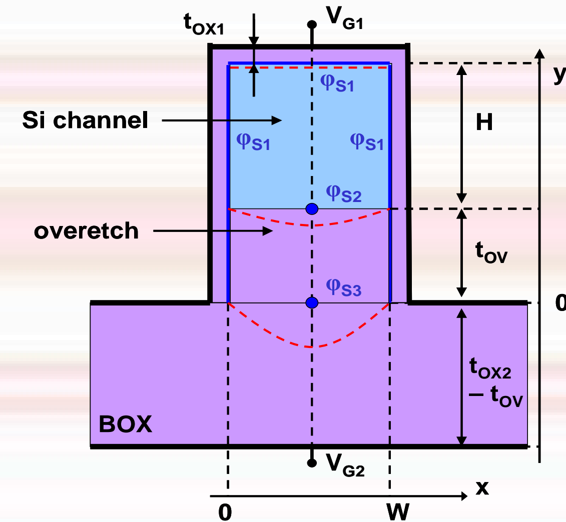

Variation of intrinsic capacitance in GAA device with gate voltage

# 3D potential, TGFETs/PiFETs

- 3D Laplace's equation to solve:

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2}+\frac{\partial^2\psi(x,y,z)}{\partial y^2}+\frac{\partial^2\psi(x,y,z)}{\partial z^2}\approx 0$$

- Boundary conditions:
  - ✓ Influence of the 6 terminals (3 sides of the top-gate, back-gate, source and drain) considered separately.
  - ✓ Dirichlet (with constant or parababolic boundary conditions) or Neumann.




*Transversal cross-section TGFET/PiFET, with notations.*

- 3D potential:

$$\varphi(x,y,z)=\varphi_{\text{Top-gate (TG)}}(x,y,z)+\varphi_{\text{Back-gate (BG)}}(x,y,z)+\varphi_{\text{Lateral-gates (LG)}}(x,y,z)+\varphi_{\text{Source / Drain (SD)}}(x,y,z)$$

$$\varphi_{TG}(x,y,z)=(V_{G1}-V_{FB1})\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_C(m)F_C(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{n\pi z}{L_G}\right)\left[\cosh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi y\right)\Big/\cosh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi(H+t_{OV})\right)\right]$$

$$\varphi_{LG}(x,y,z)=(V_{G1}-V_{FB1})\sum_{m=1}^{+\infty}\sum_{n=0}^{+\infty}F_P(m)F_n(n)\sin\left(\frac{m\pi z}{L_G}\right)\sin\left(\frac{(2n+1)\pi(H+t_{OV}-y)}{2(H+t_{OV})}\right)\left[\frac{\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+t_{OV})}\right)^2}\,\pi(W-x)\right)+\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+t_{OV})}\right)^2}\,\pi x\right)}{\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+t_{OV})}\right)^2}\,\pi W\right)}\right]$$

$$\varphi_{SD}(x,y,z)=\sum_{m=1}^{+\infty}\sum_{n=0}^{+\infty}F_P(m)F_n(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{(2n+1)\pi(H+t_{OV}-y)}{2(H+t_{OV})}\right)\left[\frac{V_S\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+t_{OV})}\right)^2}\,\pi(L_G-z)\right)+V_D\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+t_{OV})}\right)^2}\,\pi z\right)}{\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+t_{OV})}\right)^2}\,\pi L_G\right)}\right]$$

$$\varphi_{BG}(x,y,z)=\varphi_{S3}\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_P(m)F_P(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{n\pi z}{L_G}\right)\left[\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi(H+t_{OV}-y)\right)\Big/\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi(H+t_{OV})\right)\right]$$

with:

$$\varphi_{S3}=(V_{G2}-V_{FB2})\Big/\left(1+\frac{\varepsilon_{Si}}{\varepsilon_{BOX}/(t_{OX2}-t_{OV})}\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_P(m)F_P(n)\sin\left(\frac{m\pi}{2}\right)\sin\left(\frac{n\pi}{2}\right)\left[\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi\Big/\tanh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi(H+t_{OV})\right)\right]\right)$$

W being the fin width, H the fin height, $L_G$ the gate length, $t_{OV}$ the overetch depth, $\varepsilon_{BOX}$ the BOX permittivity, $\varepsilon_{Si}$ the silicon permittivity, $V_{FB1}$ (resp. $V_{FB2}$) the front-gate (resp. back-gate) flat band voltage. The series coefficient $F_p$, $F_n$, and $F_c$ are defined in the Appendix.

# 3D potential validation, TG and PiFETs

- Crucial role of the boundary conditions coefficients:

- Constant potential boundary condition :

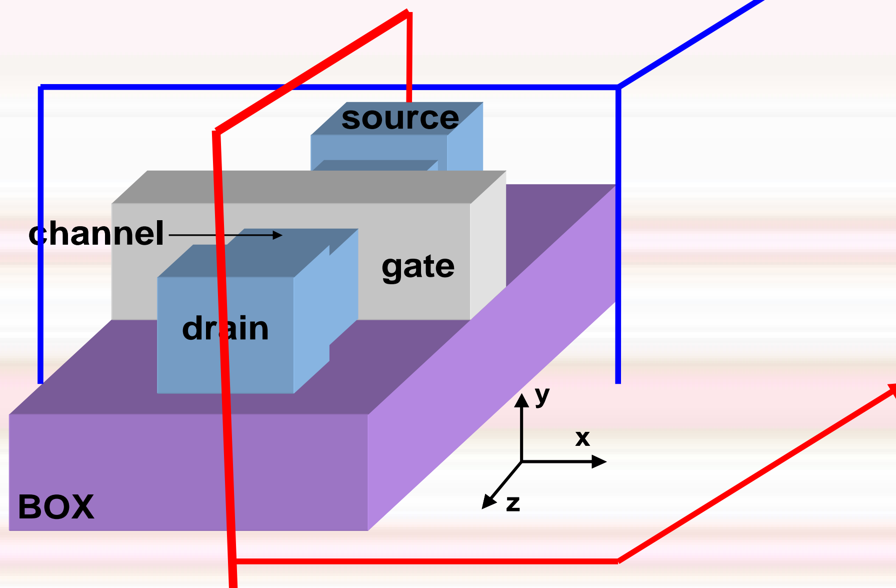
$$F_c(n) = \frac{2(1-\cos(n\pi))}{n\pi}$$

- Parabolic potential boundary condition

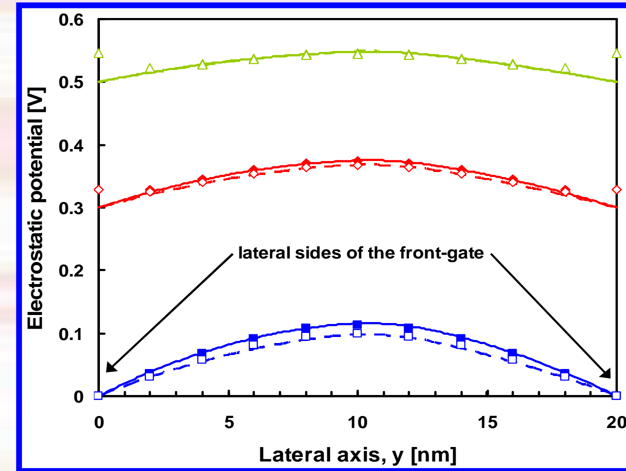
$$F_P(n) = \frac{2(1-\cos(n\pi)) - n\pi\sin(n\pi)}{(\frac{n\pi}{2})^3}$$

- Neumann boundary condition :

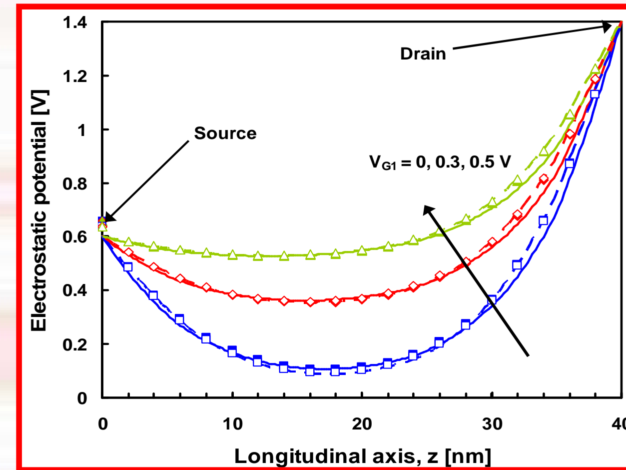
$$F_n(n) = \frac{4}{(2n+1)\pi}(1-\cos(\frac{(2n+1)\pi}{2}))$$




- **Validation of the model:**




*TGFET (closed symbols) and PiFET (open symbols)*




*TGFET (closed symbols) and PiFET (open symbols)*

# 3D potential:calculation of minimum of potential

- Position of the 'most leaky path':
  - At mid-channel ($y=W/2$) for obvious symmetry considerations
  - At the body/BOX interface ($x = t_{OV}$): generally true, not necessarily for L<(W,H) but is a correct approximation
  - Along the Source/Drain axis:
    - Low $V_{DS}$: $Z_C = L_G/2$
    - High $V_{DS}$: minimum of potential moving
- Formula from [Pei'02]:

$$Z_C = \frac{L_G}{2} + \frac{L_D}{2\pi}\ln\left(\frac{-\varphi_{MS}}{-\varphi_{MS} + V_{DS}}\right)$$

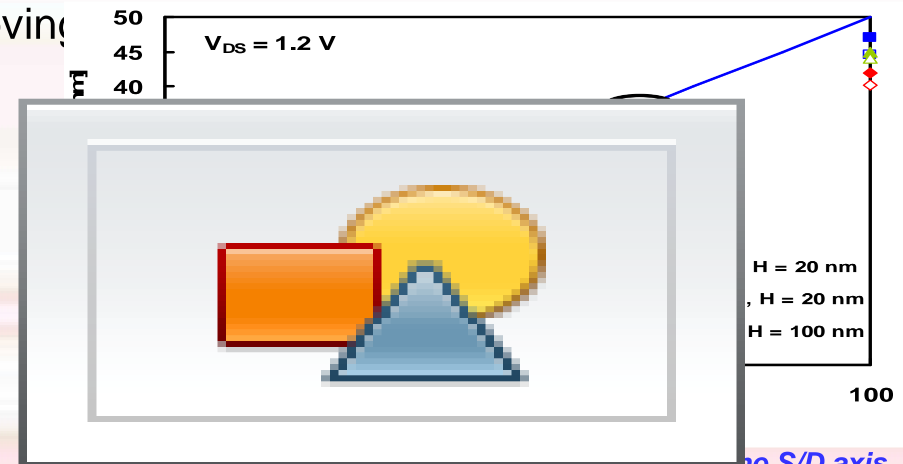
with:

$$L_D = \left(\frac{1}{W^2} + \frac{0.5}{H^2}\right)^{-1/2}$$

→ Simpler and acceptable approximation

- Finally: $\varphi_{MIN} = \varphi(t_{OV}, W/2, Z_C)$

[Pei'02] G. Pei et al., IEEE TED, 2002.



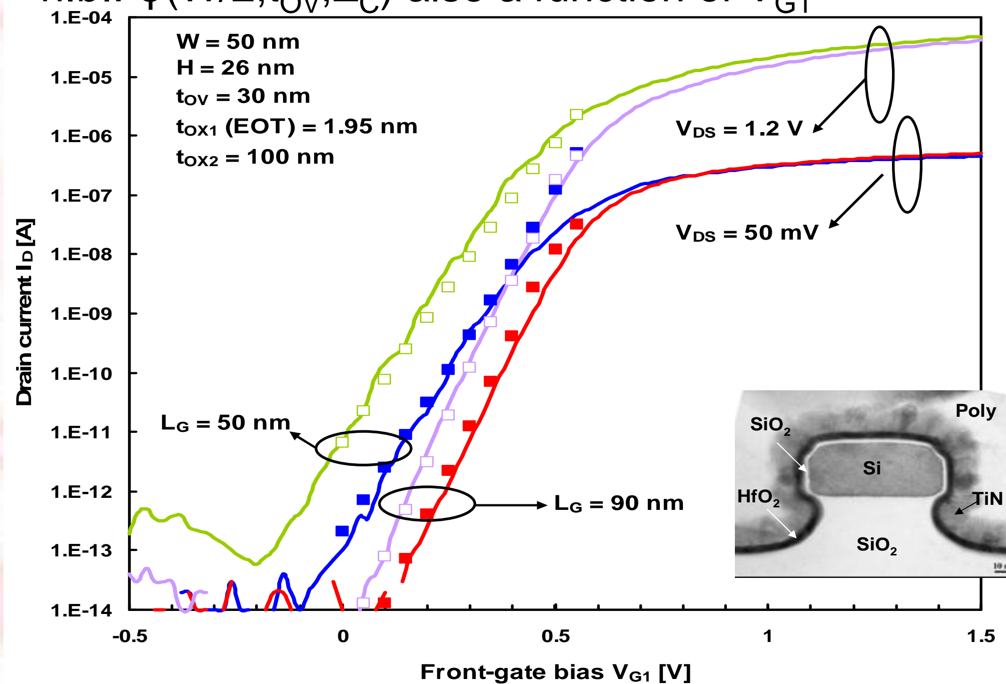

*Position of the minimum of potential along the S/D axis – comparison between the results given by the numerical simulations (closed symbols) and the analytical formula (open symbols)*

# 3D potential- Subthreshold Current

- ✓ Finally, after integration:

$$I_{DS} = \frac{\mu q n_i V_T}{L_G}(1-e^{V_{DS}/V_t})WH\frac{2e^{\varphi(W/2,t_{OV},Z_C)/V_t}+e^{V_{G1}/V_t}}{3}$$

n.b.: $\varphi(W/2,t_{OV},Z_C)$ also a function of $V_{G1}$



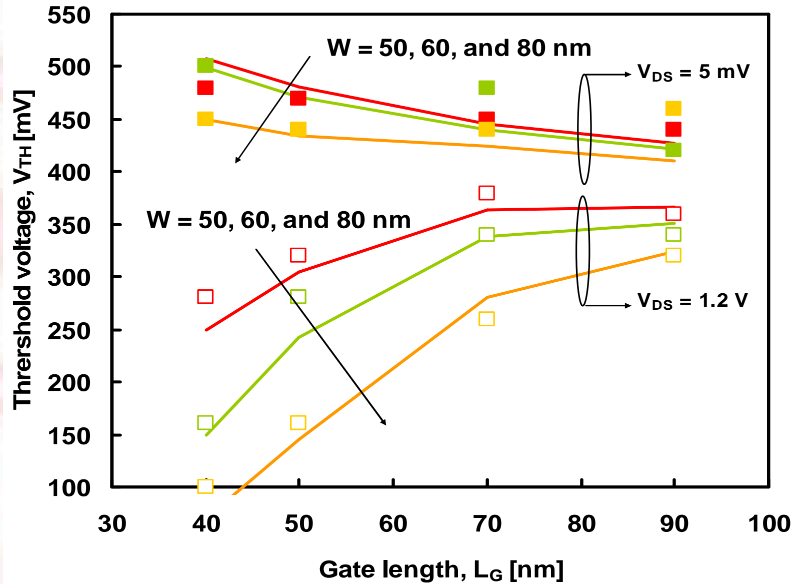

*Subthreshold analytical (symbols) and experimental (solid lines) drain currents $I_D$ vs. front-gate bias $V_{G1}$ for gate lengths $L_G$ of 90 nm (squares) and 50 nm (diamonds). Gate width W = 50 nm, H = 26 nm.*

Good precision obtained compared to experimental measurements [Jahan'05]

Formula allowing to take into account the drain and short channels effect in the subthreshold regime

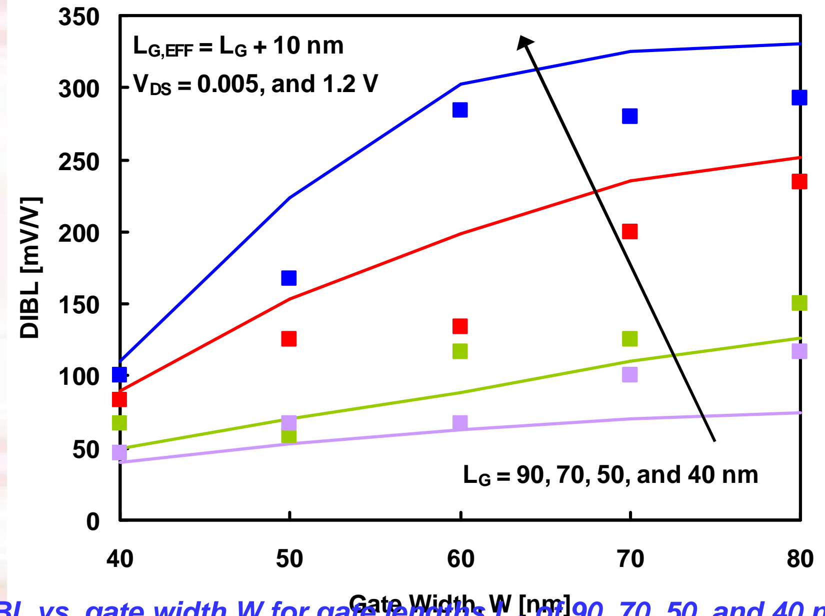
*[Jahan'05] C. Jahan et al., VLSI tech. dig., 2005.*

# 3D Potential- Roll-off, DIBL




*Threshold voltage $V_{TH}$ extracted with the constant current method (at 0.1 µA, symbols) and with the analytical model (solid lines) vs. gate length $L_G$. the gate width W varies from 50 to 80 nm, and $V_{DS}$ from 5 mV (closed symbols) to 1.2 V (open symbols). $t_{OX1}$=1.95 nm, $t_{OX2}$ = 100 nm, H = 26 nm.*

- Roll-off effect: decrease of threshold voltage when $L_G$ is reduced
- Better Roll-off for narrow devices




*DIBL vs. gate width W for gate lengths $L_G$ of 90, 70, 50, and 40 nm. Comparison between experimental extractions (symbols) and analytical model (solid lines). $t_{OX1}$=1.95 nm, $t_{OX2}$ = 100 nm, H = 26 nm.*

- DIBL straigthtforwardly calculated.
- Good agreement model/experimental measurements.

# Conclusions

Under the framework of the "COMON" EU Project, compact models for several types Multi-Gate MOSFETs are been developed.

By the end of "COMON" (Nov 2012) two types of models will be completed and ready for standardization:

1) A design oriented explicit Multi-Gate MOSFET model, based on the solution of the 1D Poisson's equation plus additional equations containing short-channel and quantum effects.

2) A predictive Multi-Gate MOSFET model, based on a full 2D/3D electrostatic analysis with self-consistency between Poisson's and transport equation

***Thank you for your attention!***