Overview and Parameter Extraction of L-UTSOI Model for FDSOI Technologies

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Agenda

• Fully Depleted Silicon On Insulator (FDSOI) Technology
• L-UTSOI Model
• Parameter Extraction of L-UTSOI
• Summary
Quiz #1: What are the technology solutions that Prof. Chenming Hu came up with in the late 1990s to replace bulk CMOS?

**FinFET and UTB-SOI (FD-SOI)**

FinFET pictures are from UC Berkeley BSIM Group website: [http://bsim.berkeley.edu/models/bsimcmg/](http://bsim.berkeley.edu/models/bsimcmg/)

Quiz #2. What’s the most advanced technology node under mass production now for FD-SOI?

A. 28 nm  <- STM: mass production since 2012
B. 22 nm  <- GLOBALFOUNDRIES 22FDX: mass production since 2017
✓ C. 18 nm  <- Samsung 18FDS: due in late 2019
D. 12 nm  <- GLOBALFOUNDRIES 12FDX: due in 2020
Quiz #3. What are the CMC standard SPICE models for FD-SOI technology?

- **BSIM-IMG** developed by UC Berkeley
- **HiSIM-SOTB** developed by Hiroshima University

*SOTB: Silicon-On-Thin-Buried-Oxide*

One more coming soon –

- **L-UTSOI** developed by CEA Leti (in Phase IV now)
Fully Depleted Silicon On Insulator (FDSOI) Technology
Challenges in Traditional Bulk CMOS Scaling

Bulk CMOS

* https://en.wikipedia.org/wiki/CMOS
The Advantages of FDSOI

**Ultra-Thin Body**
- Excellent electrostatic control of the channel
- Less SCE, DIBL effects
- Moore’s Law → continue device gate length scaling

**Undoped Channel**
- No Random Dopant Fluctuation!
- Less process variation, less local mismatch
- Lower power consumption

**Total Dielectric Isolation**
- No source-bulk and drain-bulk junction current
- Small source/drain-UTB capacitance
- Lower source-to-drain leakage
- Less sensitive to temperature
- Higher power efficiency

**Ultra-Thin Buried Oxide**
- Stronger body biasing (BB) than bulk technology, FBB&RBB
- Speed boost due to BB
- Vt adjustment

**More Cost Efficient**
- Simpler process development
- Fewer mask counts than FinFET
- Shorter design spins
- Analog & RF integration

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- RDF picture captured from: https://www.youtube.com/watch?v=uvV7jcpiQ7UY

SCE: Short Channel Effect
DIBL: Drain Induced Barrier Lowering
RDF: Random Dopant Fluctuation
FBB & RBB: Forward & Reverse Body Biasing
STI: Shallow Trench Isolation
# APPLICATION BENEFITS BY MARKET SEGMENT

## Internet of Things, Wearable
- Ultra-low-voltage operation
- FBB optimizes power/performance
- Efficient RF and analog integration

## Automotive
- Well-managed leakage in high-temperature environments
- High reliability thanks to highly-efficient memories

## Networking Infrastructure
- Energy-efficient multicore
- Adapt performance & power to workload via FBB
- Excellent performance in memories

## Consumer Multimedia
- Optimized SoC integration (Mixed-signal & RF)
- Energy-efficient SoC under all thermal conditions
- Optimized leakage in idle mode

- Picture cited from ST’s 28nm FD-SOI Technology Catalog
L-UTSOI Model
CMOS Compact Models Progress Overview

- **1990**: BSIM3
- **1995**: BSIM4
- **2000**: BSIM SOI (Partially and Fully Depleted)
- **2005**: EKV
- **2010**: BSIM-BULK
- **2015**: HiSIM (HV, SOI)
- **2020**: BSIM-CMG/IMG

- **Surface Potential**
  - Local / Global
  - PSP
  - UT-SOI
  - UT-SOI2
L-UTSOI Model Structure

- L-UTSOI is a surface potential based model featuring local/global scale modes, with a structure similar to PSP.

+ thermal node for self-heating
Parameter Extraction of L-UTSOI
Keysight Device Modeling Portfolio

END-TO-END, ENTERPRISE GROUP USE AND OPEN PLATFORM

- IC-CAP/MBP Bundle
  - IC-CAP – User Programmable Solution
  - MBP – Turn-key CMOS modeling Solution
  - PEMG – Power Electronics Model Generator

WaferPro Express

Advanced Low Freq Noise Analyzer

MQA

Automated Measurements

Model Extraction

Model Verification

IC-CAP Common Data Format, Measurement Information, and Dynamic Links

2019 Keysight EEsof EDA
Model Builder Program (MBP)

L-UTSOI MODEL EXTRACTION PACKAGE

Hierarchical extraction flow control
Script driving flow customization
Model history and version control
Data/Simu visualization
Script driving FoM/Scaling customization
Parameter tuning and optimization
Automated Extraction Flow in MBP

**LOCAL TO GLOBAL APPROACH FOR ROOM TEMP**

- CV Extraction for Wide/Long
- DC Extraction for Wide/Long
- DC Extraction for Wide/Short
- L-array Scaling Extraction
- W-array Scaling Extraction
- Global Model Extraction and Generation
CV Extraction for Wide/Long (Local Model)
DC Extraction for Wide/Long (Local Model)
L-array and W-Larry Local Model Generation

- Generate local (point) models for L-array and W-Larry devices
Global Parameter Optimization Example

\[ L_{\text{eff}} = \text{LP1} \times \max \left\{ 1 + \text{LP1} \frac{W_{\text{CN}}}{W_e}, 10^{-3} \right\} \]
\[ G_{FE} = \max \left\{ 1 + \text{FBET1} \left( 1 + \text{FBET1} \frac{W_{\text{BE}}} {W_e} \frac{1 - \exp(-L_e/L_{\text{eff}})}{L_e/L_{\text{eff}}} + \text{FBET2} \frac{1 - \exp(-L_e/L_{\text{eff}})}{L_e/L_{\text{eff}}} \right), 10^{-6} \right\} \]
\[ G_{\text{WF}} = \max \left\{ 1 - \text{BETW1} \frac{W_{\text{CN}}}{W_e} - \text{BETW2} \frac{W_{\text{CN}}}{W_e} \ln \left( \frac{1 + W_{\text{CN}}}{W_{\text{BE}}} \right), 10^{-6} \right\} \]
\[ G_e = UO \frac{G_{\text{WF}}}{G_{FE}} \]

\[ \text{BETN} = G_e \frac{W_e}{L_e} \]

BETN: Front channel aspect ratio times low field mobility at TR

Global Extraction
- Parameter Initialization
- Opt_VFB_vs_L
- Opt_VFB_vs_W
- Opt_PSCFE_vs_L
- Opt_PSCFE_vs_W
- Opt_CF_vs_L
- Opt_CF_vs_W
- Opt_BETN_vs_L
- Opt_BETN_vs_W
- Opt_THESEAT_vs_L
- Opt_THESEAT_vs_W
- Opt_AY_vs_L
- Opt_AY_vs_W
- Opt_ALP_vs_L
- Opt_ALP_vs_W
- Opt_RS_vs_W
- Opt_XCOR_vs_L
- Opt_XCOR_vs_W
- Opt_CSO_vs_L
- Opt_CSO_vs_W
- Opt_AGICL_vs_W
Global Model Tuning and Optimization

- Built-in and customizable Figure-of-Merits scaling analysis across W/L/T and biases.
Create Optimization in GUI

- Device Select
- Plot Select
- Parameter Select
- Optimizer Select

- Search:
  - Name
  - Value
  - Min
  - Max

- Notes:
  - The parameters should be independent.

- Optimizer Select:
  - Optimize when RMS > 0.3
  - Type: Differential operator selected in Psp
  - PM: 3
  - MX: 4
  - Number: 1000
  - Synthesis:
    - MH:
    - Extent:
      - Enable extend boundary: [ ]
      - Extend boundary when RMS > 0.5
      - Extend percent: 10

2019 Keysight EEsof EDA
Create Extraction and Optimization with Script

```c
void runStep()
{
    flow,Util::clearAll();
    cmu, setPlotLayout(2,2);
    //RETH: Freq channel aspect ratio times low freq mobility at TR
    def pg = cmu.getPageGroup(flow,SetupNames::get_data_name_ids_vgs_vbe());
    def plot = pg.build(flow,SetupNames::get_condition_Vlin()).build(flow,SetupNames::get_current_WL_device());
    def pPlot(0)
    cmu.plot(pPlot());
    pg = cmu.getPageGroup(flow,SetupNames::get_data_name_ids_vgs_vbe());
    plot = pg.build(flow,SetupNames::get_condition_Vlin()).build(flow,SetupNames::get_current_WL_device());
    double x = pg.getData(p);
    int iIdx = x, indexOf(0);
    //plotCurveSelected(new int[] {iIdx}, true);
    double[] x = flow,Util::getXdata();
    double y = flow,Util::getYHeight();
    double g = cmu, getDerivative(x);
    int maxIndx = g, index(x, g, maxIndx); 9/10;
    //p.selectRegion(x[0], x[1, x, index-1]);
    cmu.plot(pPlot());
    pg = cmu.getPageGroup(flow,SetupNames::get_name_QN_VGS_VBE());
    plot = pg.build(flow,SetupNames::get_condition_max_wear());
    pPlot.build(flow,SetupNames::get_current_WL_device());
    p.selectRegion(x[0], x[1, x, index-1]);
    cmu.plot(pPlot());
    pg = cmu.getPageGroup(flow,SetupNames::get_name_QN2_VGS_VBE());
    plot = pg.build(flow,SetupNames::get_condition_max_wear());
    pPlot.build(flow,SetupNames::get_current_WL_device());
    p.selectRegion(x[0], x[1, x, index-1]);
    cmu.plot(pPlot());
    String[] param = new String[]("RETH", "VFB");
    //optimize, and auto expand param boundary for 5 times
    flow,Util::optimize(param, 5); runStep();
}
```
Summary & Acknowledgement
Summary

• FDSOI enables better transistor electrostatic characteristics versus conventional bulk technology.
• Compared to FinFET, FDSOI technology has a simpler process. Thus, FDSOI can be chosen as a lower cost alternative for IoT, automotive and mobile applications.
• L-UTSOI is a high accurate and maturity model, to describe FDSOI transistor behavior in all biasing configurations, and has been supported by mainstreamed simulators.
• The turnkey baseband model extraction flow of L-UTSOI is implemented in Keysight’s MBP software. The flow is fully customizable and easy to maintain.
Acknowledgement

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