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New analytical model for AOSTFTs

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Introduction

Nowadays **Amorphous Metal-Oxide Semiconductor Thin-Film Transistors (AOSTFTs)** are important device, specially in flat panels for Monitors and TV.

These TFTs show high mobility values, which can reach much more than 10 cm^2/Vs . Under some conditions, their I-V characteristic can even show a behavior, similar, to those of crystalline TFTs.

A full model, including static and dynamic characteristics, is required for circuit simulation. This model must consider the operation principles of amorphous TFTs and specific characteristics of AOSTFTs.

Introduction

In 2001, we developed the **Universal Model and Extraction Method (UMEM)** that is applicable for different types of TFTs, where all model parameters are extracted individually and analytically.

This model was updated for the new AOSTFTs dynamic model including the I-V and C-V characteristics.

The new AOSTFT model was described in Verilog-A in order to be used in circuit simulators like SmartSPICE.

AOSTFT characteristics

Amorphous TFTs have a Density of States (DOS) that can be described as <u>two non-symmetrical types of states, exponentially dependent.</u>

For AOSTFTs, the DOS can be considered formed only by tail states, due to the relatively low density of states and that typically, the Fermi level lies inside this tail region, very close to the conduction band (CB)

For these devices, it was proposed the **Extended Mobility Edge Model**, which considers different conduction mechanisms in AOSTFTs: the mobility edge or multiple trapping and release mechanism typical of amorphous TFTs, as well as band conduction, including percolation.

The predominant conduction mechanism will depend on the characteristics of the materials, of the fabrication process and on the operation regime.

AOSTFT characteristics

- AOS involuntary doped charge concentration N_d is usually in the range from 1×10^{16} to 5×10^{18} cm^{-3};
- Operation voltage range is around 10 V for SiO_2, but can be reduced to less than 5 V if high-k dielectrics are used;
- Operation temperature range is between 300 and 370 K;
- Localized DOS: characteristics $g_{ato} < 1 \times 10^{20}$ $cm^{-3}eV^{-1}$, $kT_t < 100$ mV;
- Devices are accumulation type, without doping or junctions;
- The most frequent structure is the bottom gate staggered.

AOSTFT Internal model parameters

DEFINING THE FOLLOWING INTERNAL PARAMETERS [*]

φ_t Thermal potential at T
φf Fermi potential
N_d Involuntary doping concentration
N_C Density of states at the bottom of the CB

T_t Characteristic temperature
T_{eff} Effective characteristic temperature
g_{ato} Density of acceptor states at CB

$$\varphi_t = kb\,T\,/q$$

$$\varphi f = -\varphi_t \ln\left(\frac{N_d}{N_c}\right)$$

$$T_{eff} = T\left(1 + \frac{\gamma}{2}\right)$$

$$T_t = 2\,T_{eff} - T$$

$$g_{ato} = \frac{N_c}{kb\,T_t}\,\frac{e^{-\frac{\varphi f}{kb\,T}} - e^{-\frac{\varphi f}{kb\,T_{eff}}}}{J1\,e^{-\frac{\varphi f}{kb\,T_{eff}}} - J0\,e^{-\frac{\varphi f}{kb\,T_t}}}$$

$$J1 = 0.695\left(\frac{T_t}{T}\right)^{0.18} \qquad J0 = 1 - \frac{1}{1.185\left(1 - 1.185\,\frac{T_t}{T}\right)}$$

[*] Y. Hernandez-Barrios, et all., "An insight to mobility parameters for AOSTFTs, when the effect of both, localized and free carriers, must be considered to describe the device behavior", Solid State Electronics 149 (2018) 32–37.

AOSTFT Internal model parameters

localized carrier density n_{loc}

$$n_{loc} = g_{ato} \cdot kb \cdot \mathrm{Tt} \cdot e^{\frac{\phi s - \phi f}{kb\,T_t}} \int_0^{e^{\frac{\phi s - \phi f}{kb\,T_t}}} \frac{dz}{1 + z^{\frac{T_t}{T}}}$$

free carrier density n_{free}

$$n_{free} = Nc \frac{2}{\sqrt{\pi}} \int_0^{\infty} \frac{\sqrt{x}}{1 + e^{x - \frac{\phi s - \phi f}{kb\,T}}} \mathrm{dx}$$

total carrier density n_{tot}

$$n_{tot} = n_{free} + n_{loc}$$

effective carrier density $n_{eff}=n_{tot}$

$$\boldsymbol{n_{eff} = N_{eff}\, e^{\frac{\phi s - \phi f}{kb\,T_{eff}}}}$$

$$\boldsymbol{N_{eff} = N_C + g_{ato}\, kb\, T_t\, Jf}$$

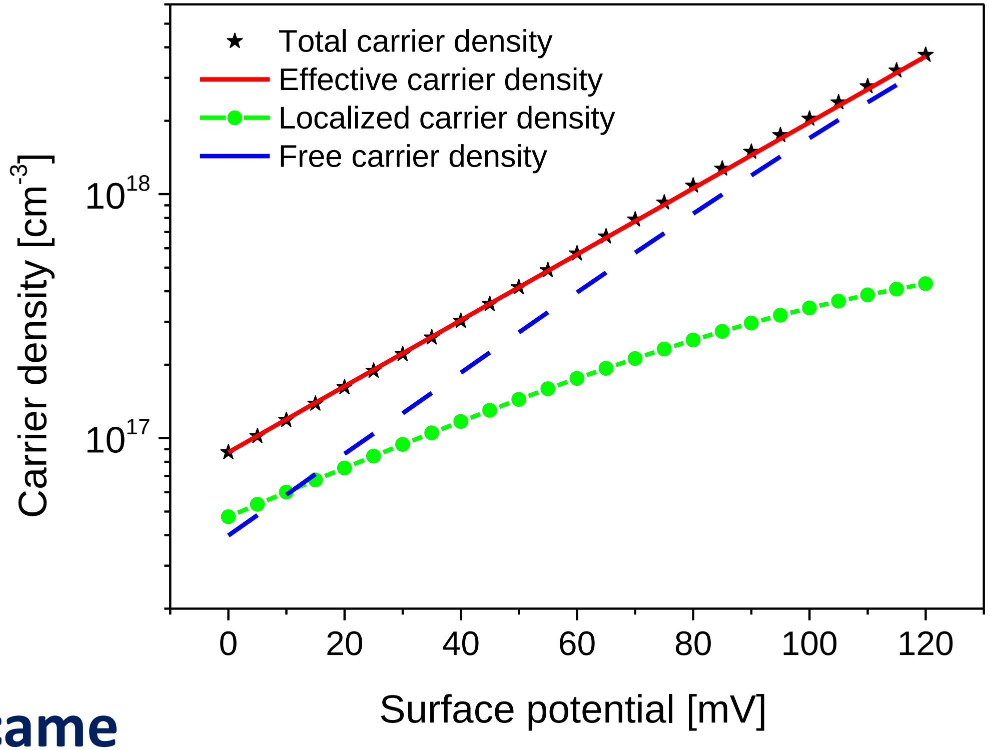
***N**eff* - effective carrier density, when the surface potential equals the Fermi potential

***T**eff* - effective characteristic temperature;

AOSTFT Conduction mechanism – carrier density

In [*], the different carrier densities were calculated for an IGZO AOSTFT with:

W = 100 μm
L = 40 μm
di = 200 nm
εi = 5.2
εs = 9
$Nd=4x10^{16}$ cm^{-3}



It is seen that the free carrier density became predominant when surface potential was above 20 mV.
This is the cause of their high mobility

[*] Y. Hernandez-Barrios, et all., "An insight to mobility parameters for AOSTFTs, when the effect of both, localized and free carriers, must be considered to describe the device behavior", Solid State Electronics 149 (2018) 32–37.

AOSTFT Conduction mechanism - Field-Effect mobility

The Field-Effect Mobility μ_{FE} is now calculated through AOSTFT internal parameters.

Considering the Boltzmann distribution; μ_0 -the band mobility;

C_i -dielectric capacitance per unit area; Q_s -total charge associated with the effective carrier density and γ - mobility power parameter.

$$Q_S = Q_0\, e^{-\frac{\varphi f}{2\, kb\, T_{eff}}}; \qquad Q_0 = \sqrt{2q\, \varepsilon_S \epsilon o N_{eff} kbT_{eff}}$$

$$\mu_{FE} = \mu_0 \left[\frac{n_{free}}{n_{tot}}\right] = \mu_0 \left[\frac{n_{free}}{n_{eff}}\right] = \mu_0 \left[\frac{N_C\, e^{\frac{\phi s - \phi f}{kb\, T}}}{N_{eff}\, e^{\frac{\phi s - \phi f}{kb\, T_{eff}}}}\right] = \mu_0 \left[\frac{N_C}{N_{eff}}\right] \left(\frac{C_i}{Q_0}\right)^{\gamma} \left(V_g - V_t\right)^{\gamma}$$

AOSTFT I-V characteristics

Auxiliary expresions

$$K = \frac{W}{L} C_i$$

V_g-V_t

$$V_{gt} = \frac{V_{min}}{2}\left[1 + \frac{V_g - V_t}{10^{-6}} + \sqrt{100 + \left(\frac{V_g - V_t}{10^{-6}} - 1\right)^2}\right]$$

V_g-V_{fb}

$$V_{gf} = \frac{V_{min}}{2}\left[1 + \frac{V_g - V_{fb}}{10^{-6}} + \sqrt{100 + \left(\frac{V_g - V_{fb}}{10^{-6}} - 1\right)^2}\right]$$

V_d effective

$$V_{def} = \frac{1}{\left[1 + \left(\frac{V_d}{\alpha s}\right)^m\right]^{\frac{1}{m}}}$$

AOSTFT I-V characteristics

Mobility

$$\mu_{FE} = \mu_0 \frac{N_c}{N_{eff}} \left(\frac{C_i}{Q_0}\right)^{\gamma} V_{gt}^{\gamma}$$

Current above V_t

$$I_{at} = \frac{K\,\mu_{FE}\,V_{gt}}{1+R\,K\,\mu_{FE}\,V_{gt}} V_{def}\left(1+\lambda\left(V_d - V_{def}\right)\right)$$

Current below V_t

$$I_{bt} = \left\{K\,\mu 1b\,V_{gf}{}^{1+\gamma_b}\,V_{dl}\,e^{\frac{V_t - V_t - V1}{S}2.3} + I_0\right\}\frac{1}{2}\left[1 - th\left(\left(V_g - V_{fb} - V1\right)Q1\right)\right] + \\ + \left\{K\,\mu 1b\,V_{gf}{}^{1+\gamma_b}\,V_{dl}\,e^{\frac{V_g - V_t - V1}{S}2.3}\right\}\frac{1}{2}\left[1 + th\left(\left(V_g - V_{fb} - V1\right)Q1\right)\right]$$

Total current

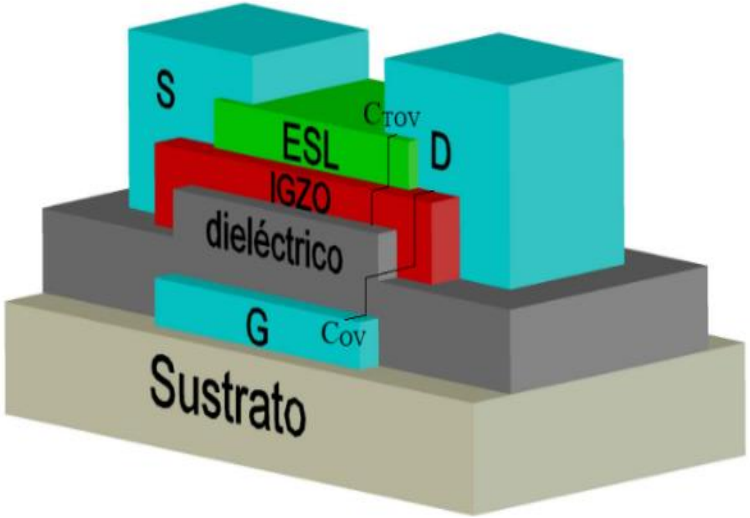
$$I_{ds} = \{I_{bt}\}\frac{1}{2}\left[1 - th\left(\left(V_g - V_t - V2\right)Q2\right)\right] + \{I_{at}\}\frac{1}{2}\left[1 + th\left(\left(V_g - V_t - V2\right)Q2\right)\right]$$

AOSTFT Structure parameters

AOSTFTs - staggered, *bottom-gate top-contact (BGTC)* structure.

As an example, we will use an *IGZO AOSTFT* with the following structure parameters:

Channel width	**W= 900 μm**;
Channel length	**L= 30 μm**;
Gate dielectric thickness	**di= 200 nm**;
Passivation dielectric thickness	**dipas= 200 nm**;
Semiconductor thickness	**ts= 12 nm**;
D and S overlap length	**t_{ov}= 5 nm**;
D and S top overlap length	**L_{tov} = 5 nm**



AOSTFT   Extraction of model parameters

Extraction of DC model parameters using the UMEM extraction procedure [*].

Above threshold:

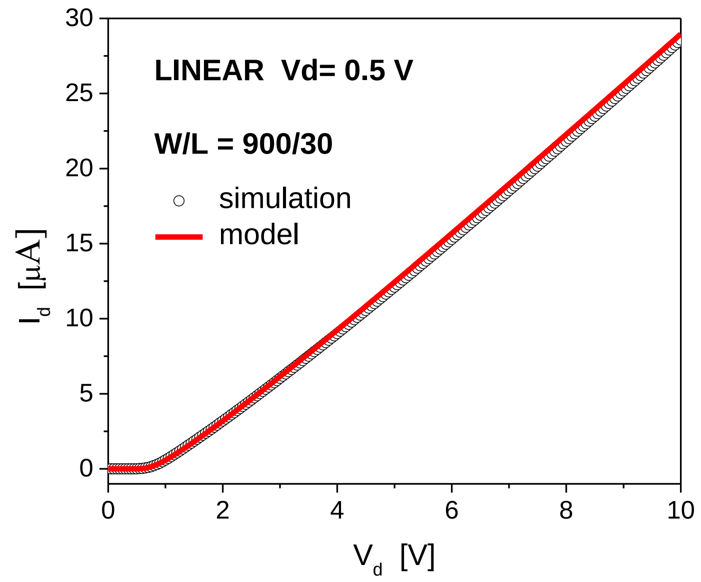
- Band mobility — $\mu_0 = 9.1\ cm^2/Vs$
- Threshold voltage — $V_T = 0.47\ V$
- Mob. power parameter — $\gamma = 0.14$
- Series resistance — $R = 190\ \Omega$
- Saturation voltaje parameter — $\alpha_S = 0.83$
- Knee of output characteristic — $m = 1.6$
- Output conductance param. — $\lambda = -0.015$

Below threshold:

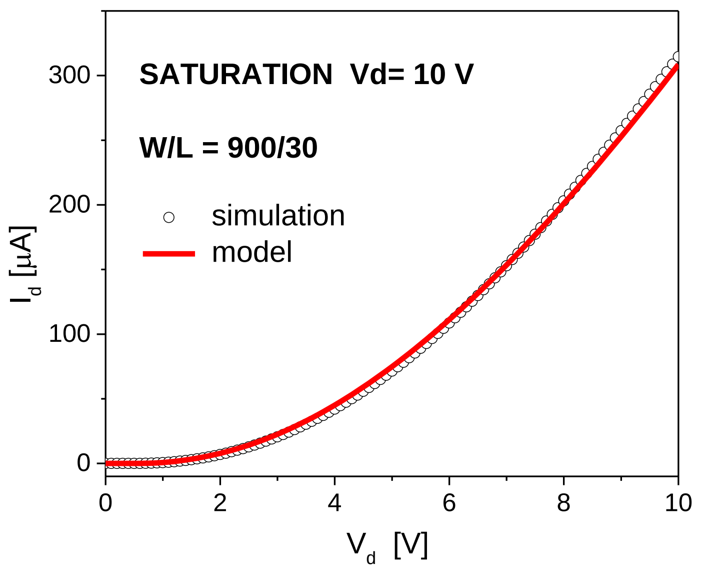
- Flat band voltaje, — $V_{FB} = 0.46\ V$
- Mob. power parameter — $\gamma_b = 0.28$
- Mob. at Vg=Vfb — $\mu b1 = 0.73$
- Subtrheshold slope — $S = 0.15$

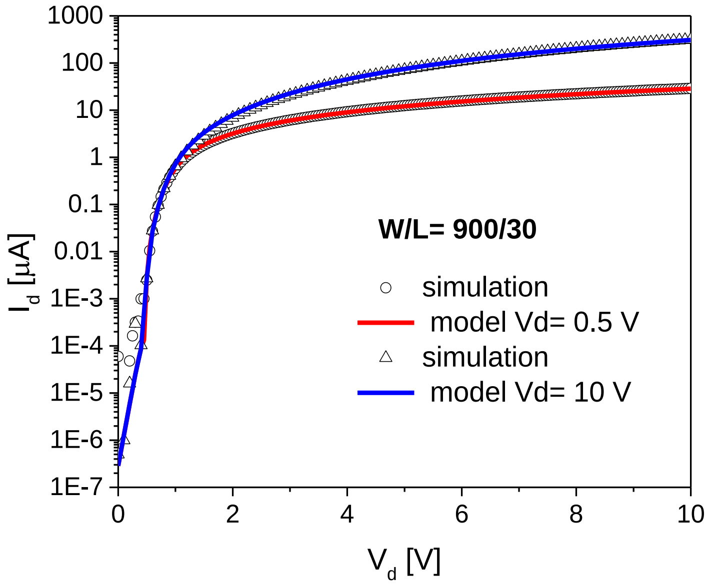
Parameters of the smoothing functions used: ***V1 = 0, Q1 = 10, V2 = 0.24 V, Q2 = 3.***

[*] A. Cerdeira *et al.*, "New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions", *Solid State Electronics*, 45, pp. 1077-1080, March 2001.

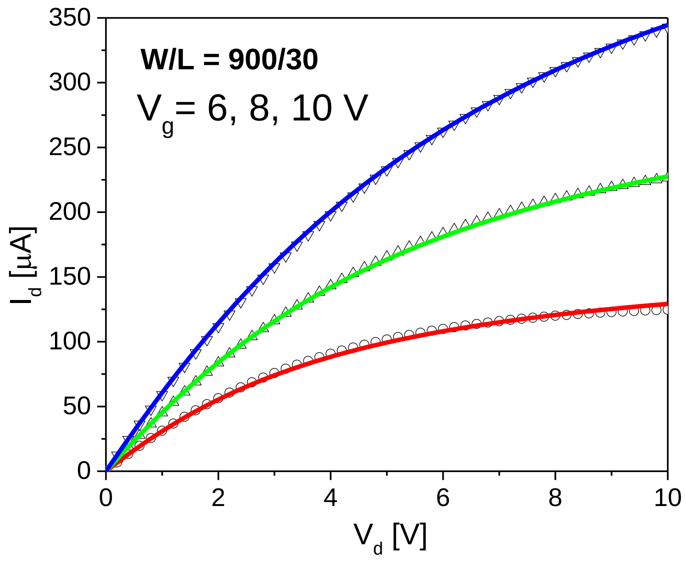


AOSTFT
I-V characteristics





I-V curves modeled, considering the structure parameters, the internal parameters and the model parameters



CAPACITANCE-VOLTAGE MODEL FOR AOSTFT

AOSTFT C-V modeling

Capacitance-Voltage modeling

For dynamic circuit simulation, in addition to the current-voltage model, a capacitance-voltage model is required.

Internal capacitances must be a function of the applied bias and consider also, the parasitic capacitance values.

The developed model considers the effects of the top-metal-overlap (**TMO)** in the staggered, bottom-gate top-contact (BGTC) structure [*].

[*] A. Cerdeira, et al., “Full capacitance model, considering the specifics of amorphous oxide semiconductor thin film transistors structures”, Solid State Electronics 156 (2019) 16–22.

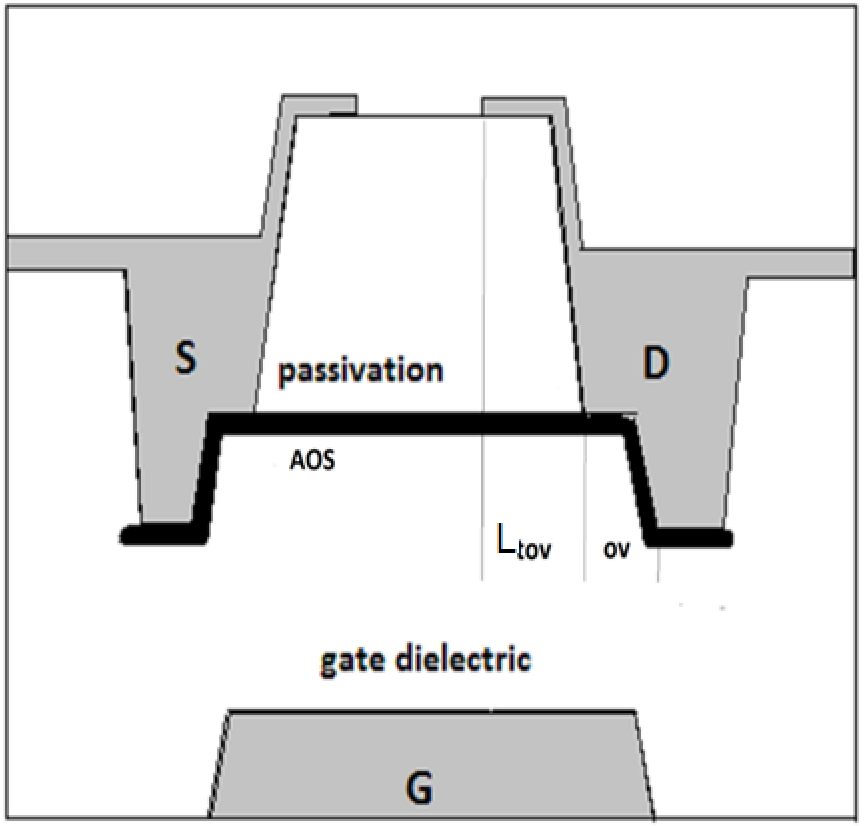
AOSTFT C-V characteristics. Top metal overlap

Cross section of a bottom gate AOSTFT using an Etch-Stop-Layer (ESL).

In AOSTFTs, the source/drain metal contacts extend on top of the passivation layer, producing an overlap with a length equal to $\boldsymbol{L_{tov}}$, is known as **Top-Metal-Overlap (TMO) [*].**

The TMO introduces a capacitance $\boldsymbol{C_{topov}}$, which depends on ***Vd*** as:

$$C_{topov} = \left(C_{pasiv}\, W\, L_{tov}\right) V_d^{0.8}\, M$$



[*] M. Estrada, et al., Effect of Drain Top Metal Overlap on the Current in Bottom-gate Thin Film Transistors, 2019 Latin American Electron Devices Conference (LAEDC), IEEE Xplorer 2019,

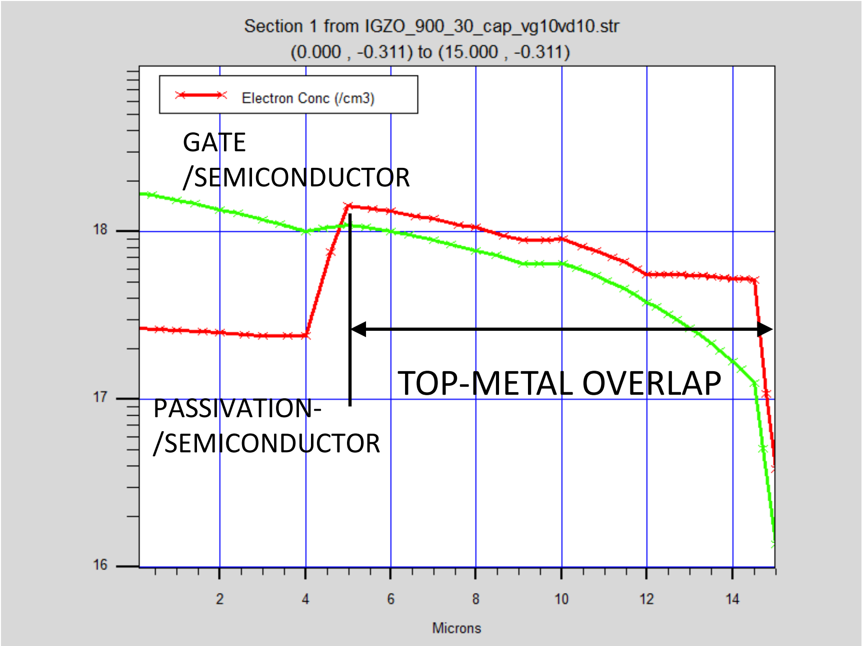
AOSTFT   C-V characteristics

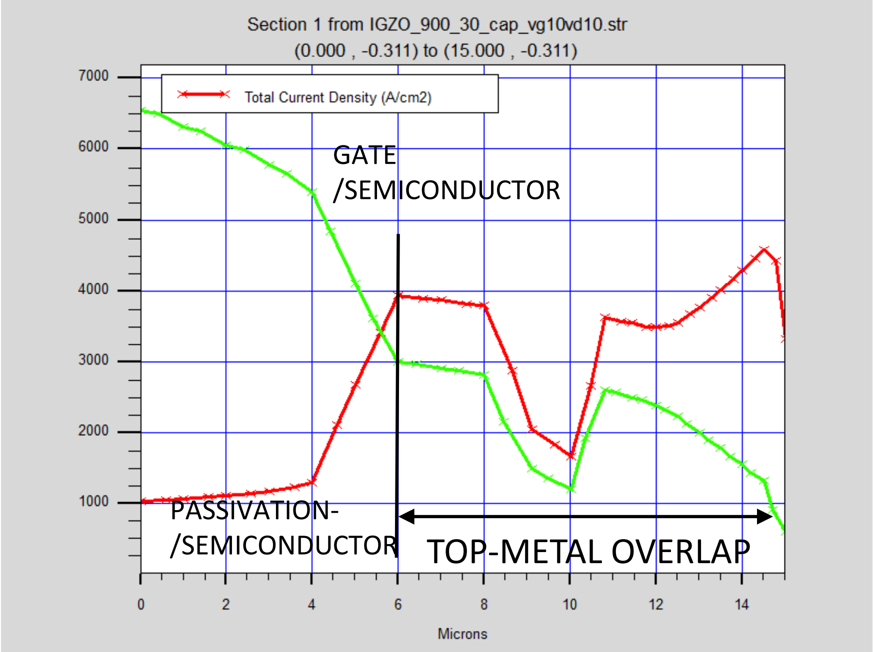
What is the TMO effect on capacitances?

Outside of the TMO region near the drain: charges at the semiconductor-passivation (S-P) interface are much lower than those at the gate-semiconductor interface (GD-S).

Within the TMO region near the drain: both charges at both interfaces are similar.

Why? Because the TMO near the drain, serves as a **second gate** with an applied gate voltage equal to V_d.





AOSTFT C-V characteristics - Calculation procedure

Calculation of transistor charges

Auxiliary expressions used: ***Vgt, Vdef*** and their derivatives**.**

Vg - Vt

$$Vgt := \frac{Vmin}{2}\cdot\left[1 + \frac{Vg - Vt}{Vmin} + \sqrt{\zeta^2 + \left(\frac{Vg - Vt}{Vmin} - 1\right)^2}\right]$$

Vd eff

$$Vdef := \frac{Vd}{\left[1 + \left(\left|\frac{Vd}{\alpha s\cdot Vgt}\right|\right)^m\right]^{\frac{1}{m}}}$$

Deriv Vgt / Vg

$$Dvgtg := \frac{1}{2}\cdot\left[1 + \frac{\left(\frac{Vg - Vt}{Vmin} - 1\right)}{\sqrt{\zeta^2 + \left(\frac{Vg - Vt}{Vmin} - 1\right)^2}}\right]$$

Deriv Vdef / Vg

$$Dvdg := \frac{\left(\left|\frac{Vd}{\alpha s\cdot Vgt}\right|\right)^{m+1}}{\left[1 + \left(\left|\frac{Vd}{\alpha s\cdot Vgt}\right|\right)^m\right]^{\frac{1}{m}+1}}\cdot\alpha s\cdot Dvgtg$$

Deriv Vdef / Vd

$$Dvdd := \frac{1}{\left[1 + \left(\left|\frac{Vd}{\alpha sVgt}\right|\right)^m\right]^{\frac{1}{m}+1}}$$

AOSTFT C-V characteristics – Calculation procedure

Auxiliary expressions A2, A3, A5 and their derivatives

$$A2 := \left[(Vgt)^{2+\gamma} - (Vgt - Vdef)^{2+\gamma}\right]$$

$$A3 := \left[(Vgt)^{3+\gamma} - (Vgt - Vdef)^{3+\gamma}\right]$$

$$A5 := \left[Vgt^{5+\gamma \cdot 2} - (Vgt - Vdef)^{5+\gamma \cdot 2}\right]$$

Deriv A2 / Vg $\quad Da2g := (2+\gamma)\cdot\left[A1\cdot Dvgtg + (Vgt - Vdef)^{1+\gamma}\cdot Dvdg\right]$

Deriv A3 / Vg $\quad Da3g := (3+\gamma)\cdot\left[A2\cdot Dvgtg + (Vgt - Vdef)^{2+\gamma}\cdot Dvdg\right]$

Deriv A2 / Vd $\quad Da2d := (2+\gamma)\cdot(Vgt - Vdef)^{1+\gamma}\cdot Dvdd$

Deriv A3 / Vd $\quad Da3d := (3+\gamma)\cdot(Vgt - Vdef)^{2+\gamma a}\cdot Dvdd$

Deriv A5 / Vg $\quad Da5g := (5+2\cdot\gamma)\cdot\left[A4\cdot Dvgtg + (Vgt - Vdef)^{4+2\cdot\gamma}\cdot Dvdg\right]$

AOSTFT Analytical expressions for the charges

Transistor charges in the channel, drain and source

Total charge in the channel = Qch = -Qg

$$Qch := (WLCi)\cdot\frac{(2+\gamma)}{(3+\gamma)}\cdot\frac{A3}{A2}$$

Charge at the drain

$$Qd := -(2+\gamma)\cdot W\cdot L\cdot Ci\cdot\left(\frac{\frac{A5}{5+2\cdot\gamma}-\frac{Vgt^{2+\gamma}\cdot A3}{3+\gamma}}{A2^{2}}\right)$$

Charge at the source

$$Qs := Qch - Qd$$

Capacitance values are calculated using the derivative of each charge

$$Cgg = \frac{dQg}{dVg};\quad Cgd = -\frac{dQg}{dVd};\quad Cgs = -\frac{dQg}{dVs};\quad Cdg = -\frac{dQd}{dVg};\quad Cdd = \frac{dQd}{dVd};\quad Cds = -\frac{dQd}{dVs}$$

AOSTFT   Analytical capacitance expressions

AOSTFT has 9 transcapacitance values, 4 of them are calculated analyticaly as:

Cgg

$$\mathrm{Cgg} := (\mathrm{WLCi})\cdot\frac{(2+\gamma)}{(3+\gamma)}\cdot\frac{1}{\mathrm{A2}}\cdot\left(\mathrm{Da3g}-\mathrm{Da2g}\cdot\frac{\mathrm{A3}}{\mathrm{A2}}\right)$$

Cgd

$$\mathrm{Cgd} := (\mathrm{WLCi})\cdot\frac{(2+\gamma)}{(3+\gamma)}\cdot\frac{1}{\mathrm{A2}}\cdot\left(\mathrm{Da3d}-\mathrm{Da2d}\cdot\frac{\mathrm{A3}}{\mathrm{A2}}\right)$$

Cgs

$$\mathrm{Cdg} := \frac{-\mathrm{WLCi}\cdot(2+\gamma)}{\mathrm{A2}^2}\cdot\left[\frac{\mathrm{Da5g}}{(5+2\cdot\gamma)}-\frac{2+\gamma}{3+\gamma}\cdot\mathrm{Vgt}^{1+\gamma}\cdot\mathrm{A3}\cdot\mathrm{Dvgtg}-\frac{\mathrm{Vgt}^{2+\gamma}}{(3+\gamma)}\cdot\mathrm{Da3g}-\left(\frac{\mathrm{A5}}{5+2\cdot\gamma}-\frac{\mathrm{Vgt}^{2+\gamma}\cdot\mathrm{A3}}{3+\gamma}\right)\cdot\frac{2}{\mathrm{A2}}\cdot\mathrm{Da2g}\right]$$

Cdd

$$\mathrm{Cdd} := \frac{-\mathrm{WLCi}\cdot(2+\gamma)}{\mathrm{A2}^2}\cdot\left[\frac{\mathrm{Vgt}^{2+\gamma}}{(3+\gamma)}\cdot\left(\mathrm{Da3d}-\frac{2\cdot\mathrm{A3}}{\mathrm{A2}}\cdot\mathrm{Da2d}\right)-\frac{1}{5+2\cdot\gamma}\cdot\left(\mathrm{Da5d}-\frac{2\cdot\mathrm{A5}}{\mathrm{A2}}\cdot\mathrm{Da2d}\right)\right]$$

The other 5 as:

$$\mathrm{Cgs} := \mathrm{Cgg}-\mathrm{Cgd}$$

$$\mathrm{Cds} := \mathrm{Cdg}-\mathrm{Cdd}$$

$$\mathrm{Csd} := \mathrm{Cgd}-\mathrm{Cdd}$$

$$\mathrm{Csg} := \mathrm{Cgg}-\mathrm{Cdg}$$

$$\mathrm{Css} := \mathrm{Cgs}-\mathrm{Cds}$$

AOSTFT Analytical capacitance expressions

Parasitic capacitances and adjusting parameters are:

The overlap capacitance, $C_{ov} = W\,L_{ov}\,C_i$

The top-metal-overlap capacitance , $C_{topov} = (W\,L_{tov}\,C_{pasiv})\,M\,(V_d)^{0.8}$

The parasitic capacitances (extracted), C_{par0}

Adjusting parameters - αss, a, D and M

Parameters of the smoothing function - ***VA, V3, Q3***

L_{tov}[μm]	α_{SS}	M	a	D	VA [V]	V3 [V]	Q3
5	1.6	0.03	0.024	0.1	0.45	0.55	7

AOSTFT   Analytical capacitance expressions

Total ***Cgg*** and ***Cgd*** in above threshold regime are calculated as:

$$CggB := Cgg\cdot(1 - Vd\cdot fa) + \left[2\cdot Cov + Cpar0 + Ctopov\cdot\left(Vd^{0.8}\right)\cdot M\right]$$

$$CgdB := (CgdA)\cdot(1 - Vd\cdot fa) + \left[Cov + \frac{Cpar0}{2} + Ctopov\cdot\left(Vd^{0.8}\right)\cdot M\right]$$

For above and below threshold regimes.

$$CggP := Cgg0\cdot\frac{1 - \tanh[(Vg - V3)\cdot Q3]}{2} + CggB\cdot\frac{1 + \tanh[(Vg - V3)\cdot Q3]}{2}$$

$$CgdP := \frac{1}{2}\cdot(Cgg0)\cdot\frac{1 - \tanh[(Vg - V3)\cdot Q3]}{2} + CgdB\cdot\frac{1 + \tanh[(Vg - V3)\cdot Q3]}{2}$$

$$CgsP := CggP - CgdP$$

AOSTFT Analytical capacitance expressions

Total ***Cdg*** and ***Cdd*** in above threshold regime are calculated as

$$CdgB := Cdg\cdot(1 - Vd\cdot fa) + Cov + \frac{Cpar0}{2} + Ctopov\cdot\left(Vd^{0.8}\right)\cdot M$$

$$CddB := Cdd\cdot(1 - Vd\cdot fa) + Cov + \frac{Cpar0}{2} + Ctopov\cdot\left(Vd^{0.8}\right)\cdot M$$

For above and below threshold regimes.

$$CdgP := \left(\frac{Cgg0}{2}\right)\cdot\frac{1 - \tanh[(Vg - V3)\cdot Q3]}{2} + CdgB\cdot\frac{1 + \tanh[(Vg - V3)\cdot Q3]}{2}$$

$$CddP := \frac{1}{2}\cdot(Cgg0)\cdot\frac{1 - \tanh[(Vg - V3)\cdot Q3]}{2} + (CddB)\cdot\frac{1 + \tanh[(Vg - V3)\cdot Q3]}{2}$$

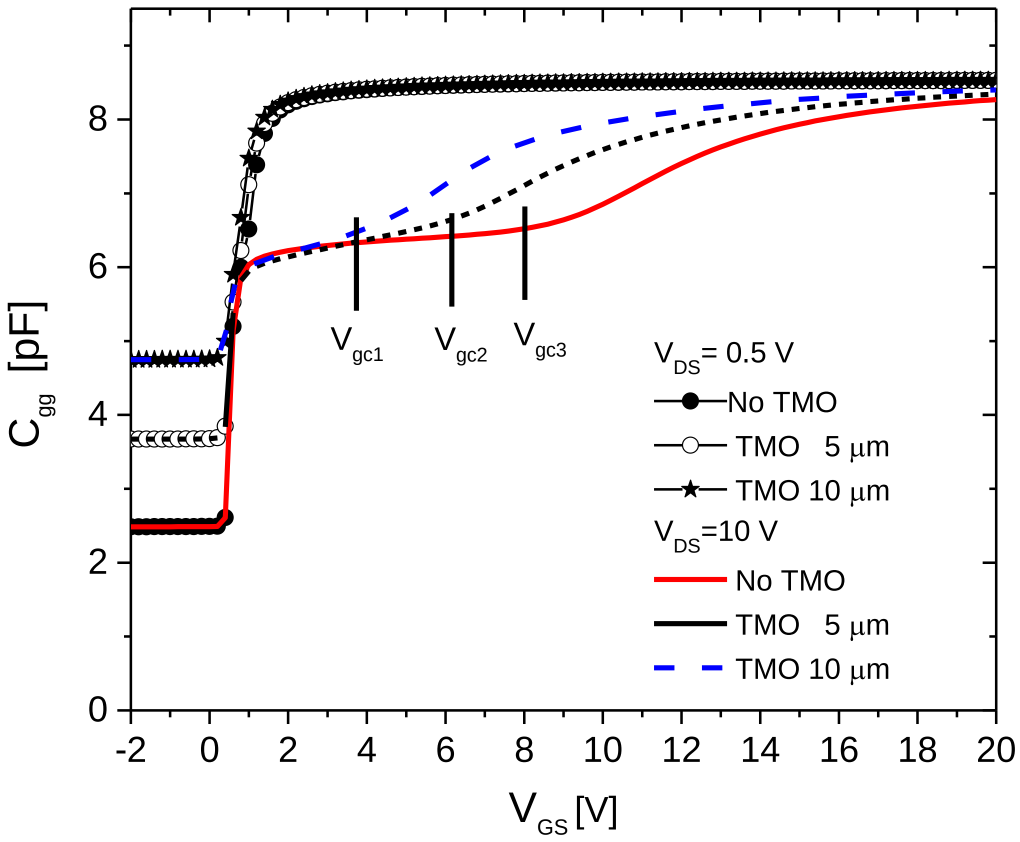
$$CdsP := CdgP - CddP$$

AOSTFT C-V characteristics. Effects of the TMO.

C_{gg} vs. V_{GS} at low drain voltage.
(V_d = 0.5V)

In ***subthreshold***, the capacitance is constant and increases with the TMO [***L_{tov}*** and ***C_{topov}***].

For **low drain voltage,** capacitances have a constant value in accumulation, independently of the TMO.



AOSTFT   C-V characteristics

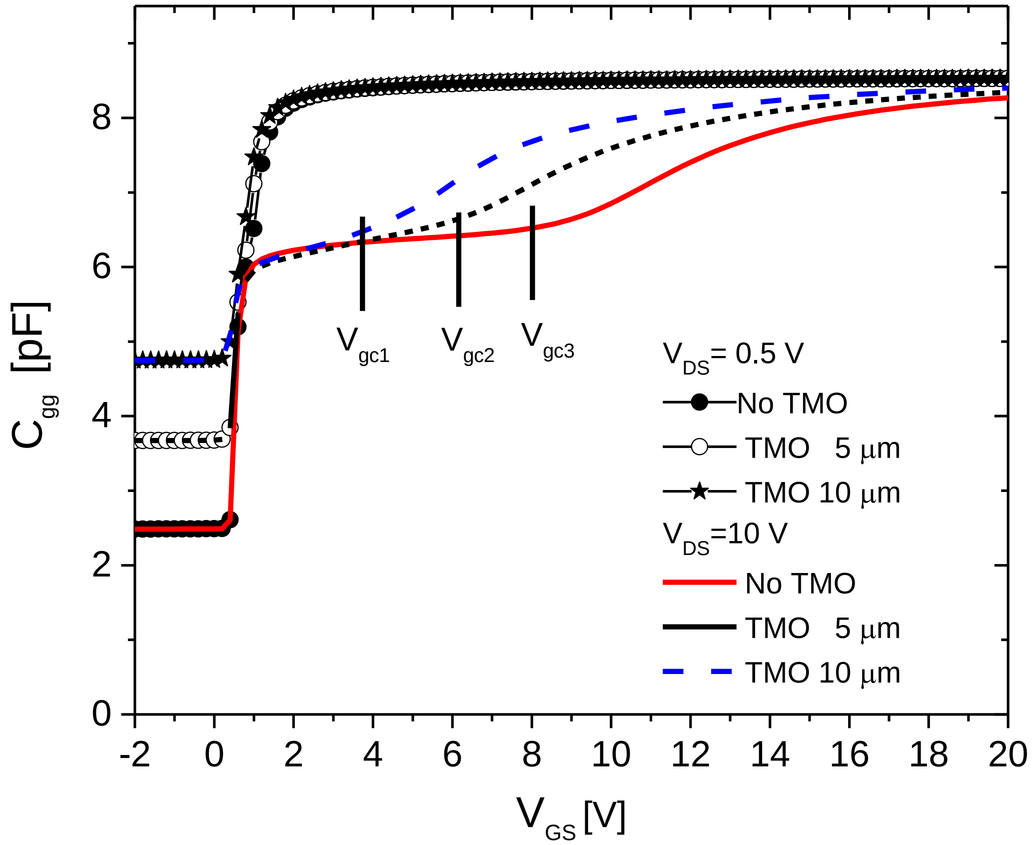
C_{gg} vs. V_{GS} at higher drain voltages

A shift of the transition voltage between saturation and linear regimes is observed. This transition voltage depends on the TMO.

$$V_{gc} = V_T + \frac{V_d}{\alpha_{ss}}$$

where V_T is the threshold voltage and α_{ss} is a modified value of the saturation parameter for amorphous thin film devices α_s

α_{ss} is extracted as a fitting parameter.



AOSTFT Analytical capacitance expressions

The voltage shift is modeled by the following expressions

Substituting the saturation parameter α_s by α_{s2} with the adjusting parameter ***αss*** and including factor ***fa*** with parameters ***a*** and ***b***,

$$Vgc := Vt + Vd\cdot\frac{1}{\alpha ss}$$

$$\alpha s2 := \left[\alpha s\cdot\frac{1 - \tanh[(Vg - Vgc)\cdot 0.5]}{2}\right] + \left[\alpha ss\cdot\frac{1 + \tanh[(Vg - Vgc)\cdot 0.5]}{2}\right]$$

$$fa := \left[a\cdot\frac{1 - \tanh[(Vg - Vgc)\cdot 0.5]}{2}\right] + b\cdot\frac{1 + \tanh[(Vg - Vgc)\cdot 0.5]}{2}$$

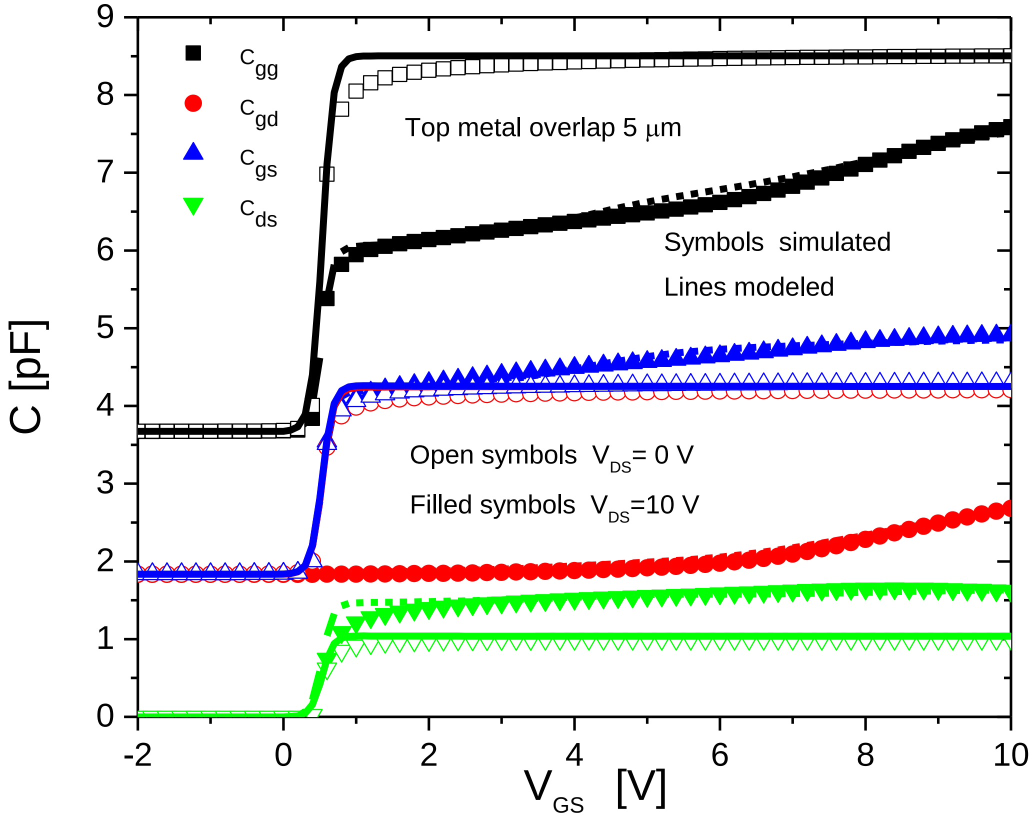
AOSTFT C-V characteristics

GATE VOLTAGE SWEEP

Comparison between simulated (*symbols*) and modeled capacitances (*lines*).

C_{gg}; C_{gd}; C_{gs}; C_{ds} vs. V_{GS}

Drain voltage: 0 and 10 V
TMO of 5 μm



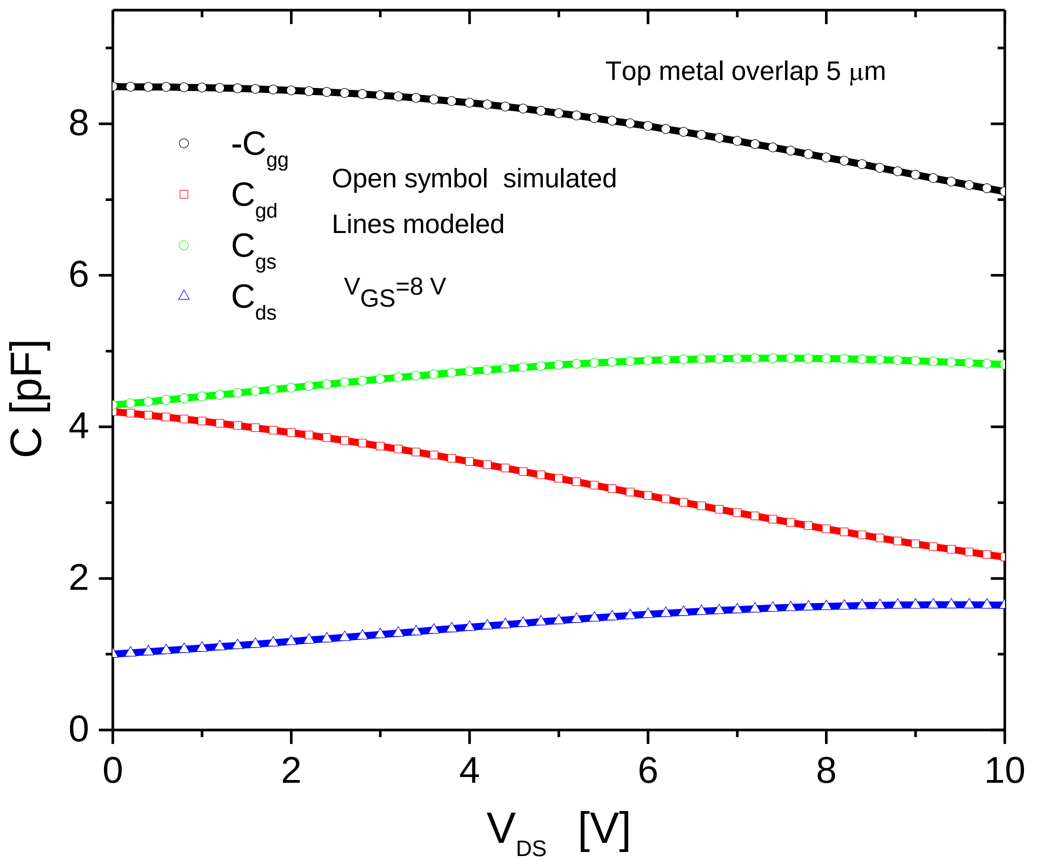
AOSTFT C-V characteristics

DRAIN VOLTAGE SWEEP

Comparison between simulated (*symbols*) and modeled capacitances (*lines*).

C_{gg}; C_{gd}; C_{gs}; C_{ds} vs. V_{DS}

Gate voltage = 8V
TMO length of 5 μm



AOSTFT

DINAMYC MODEL AND ITS VALIDATION IN SMARTSPICE

AOSTFT Dynamic model validation

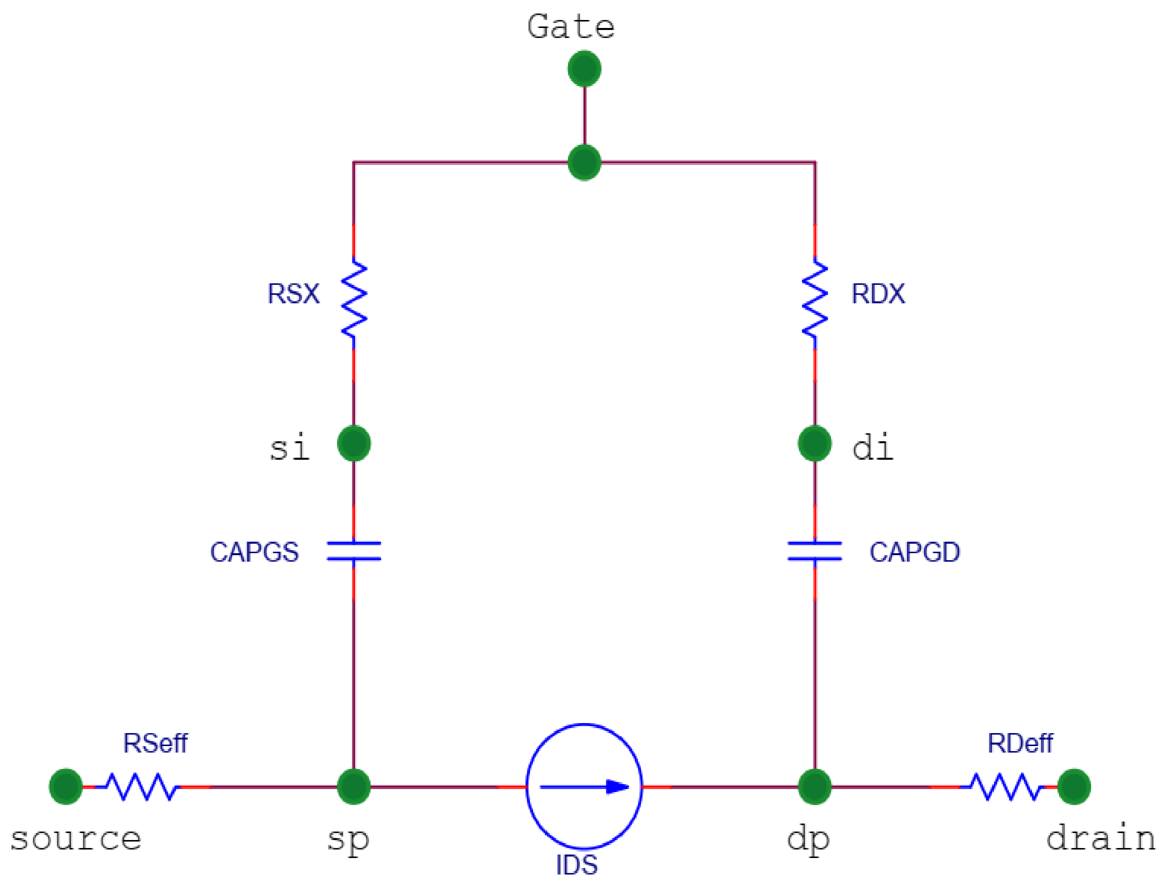
The dynamic AOSTFT model, including the current-voltage and capacitance–voltage characteristics, was described in **Verilog-A language and introduced in the circuit simulator SmartSPICE as an external model.**

For the validation of the dynamic model, an **inverter** and a **RING-OSCILATOR** of 19 inverters were simulated and results compared with experimental measurements.

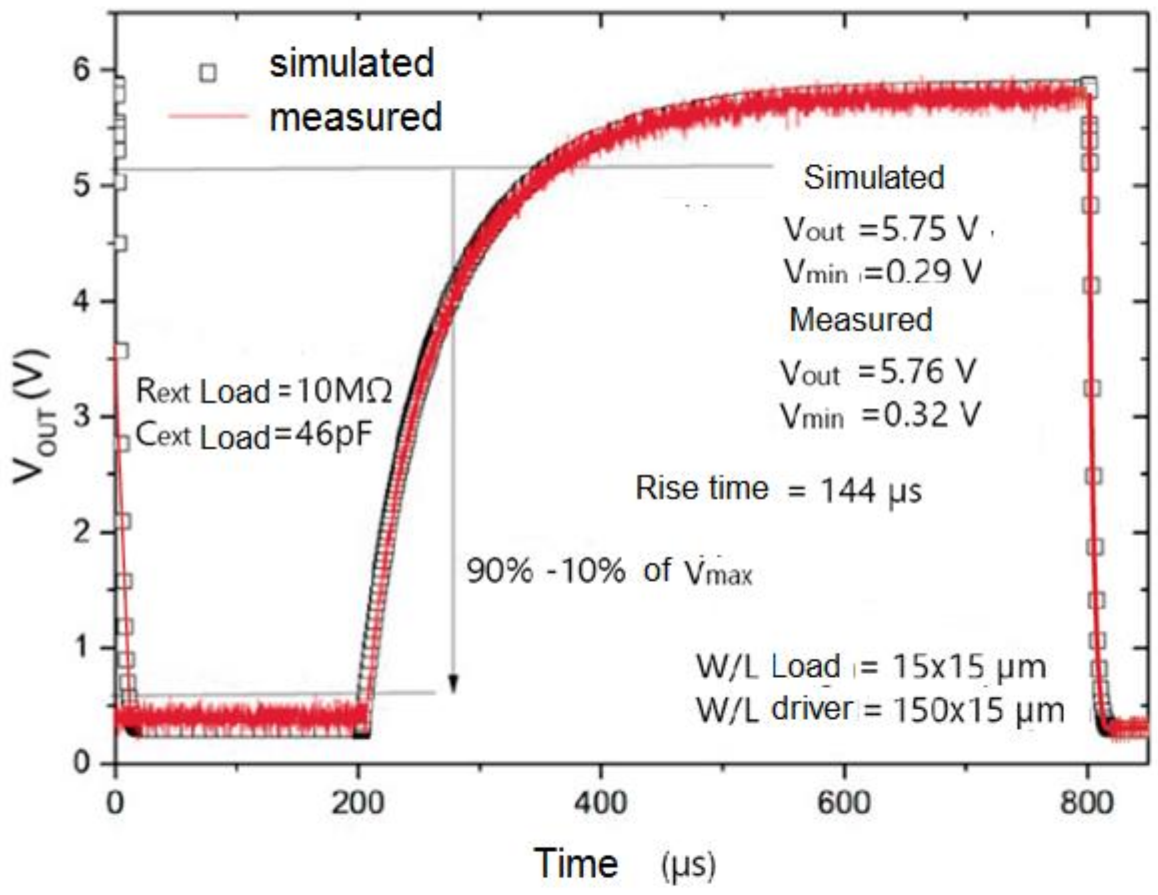
Load transistors have W/L = 15/15 and drivers have W/L=150/15.

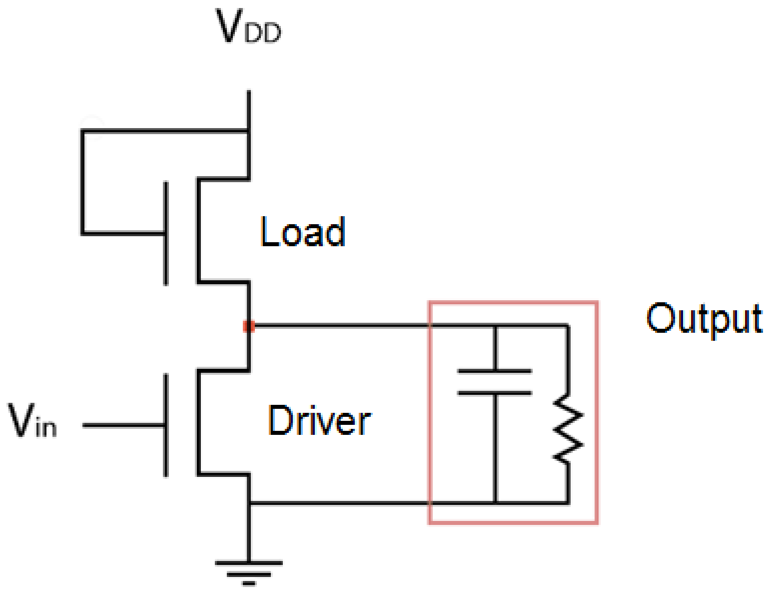
AOSTFT Dynamic model. Equivalent circuit

Equivalent circuit using the calculated currents, capacitance and resistance values



AOSTFT Transient characteristic

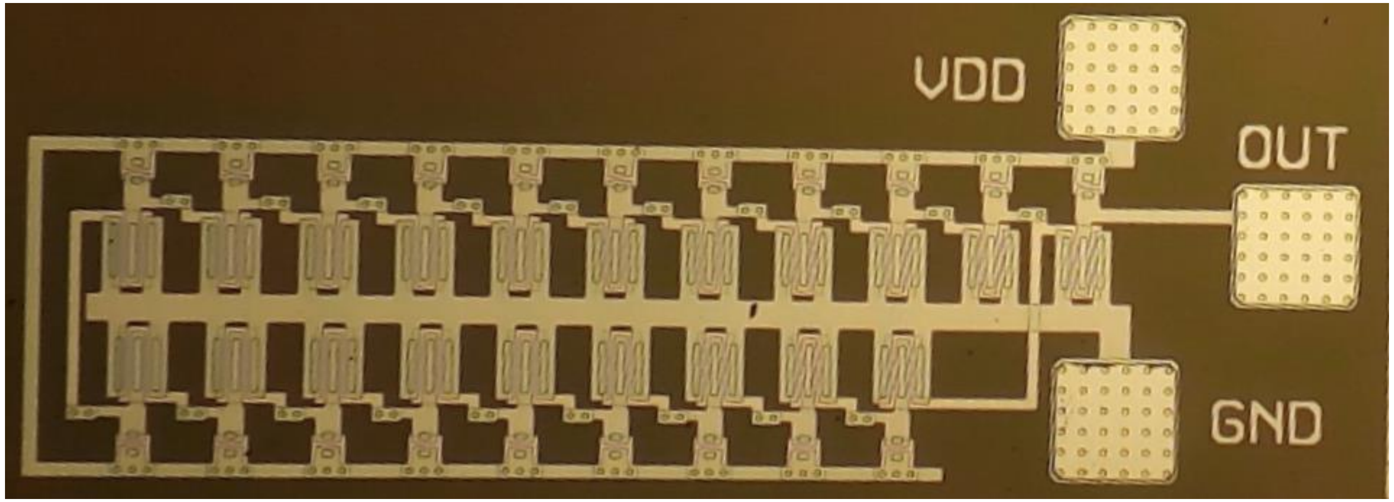


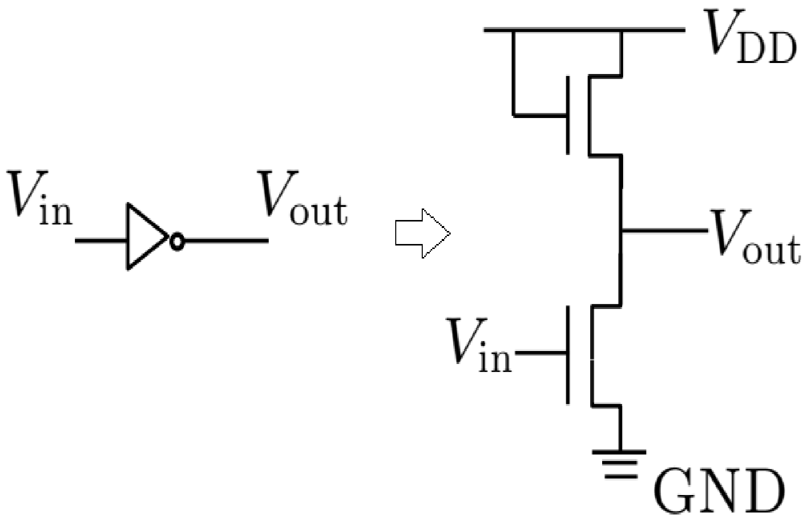


Simulated inverter at $\boldsymbol{V_d} = 10$ V

Very good coincidence between simulated and measured transient characteristic.

AOSTFT Ring-oscillator of 19 inverters





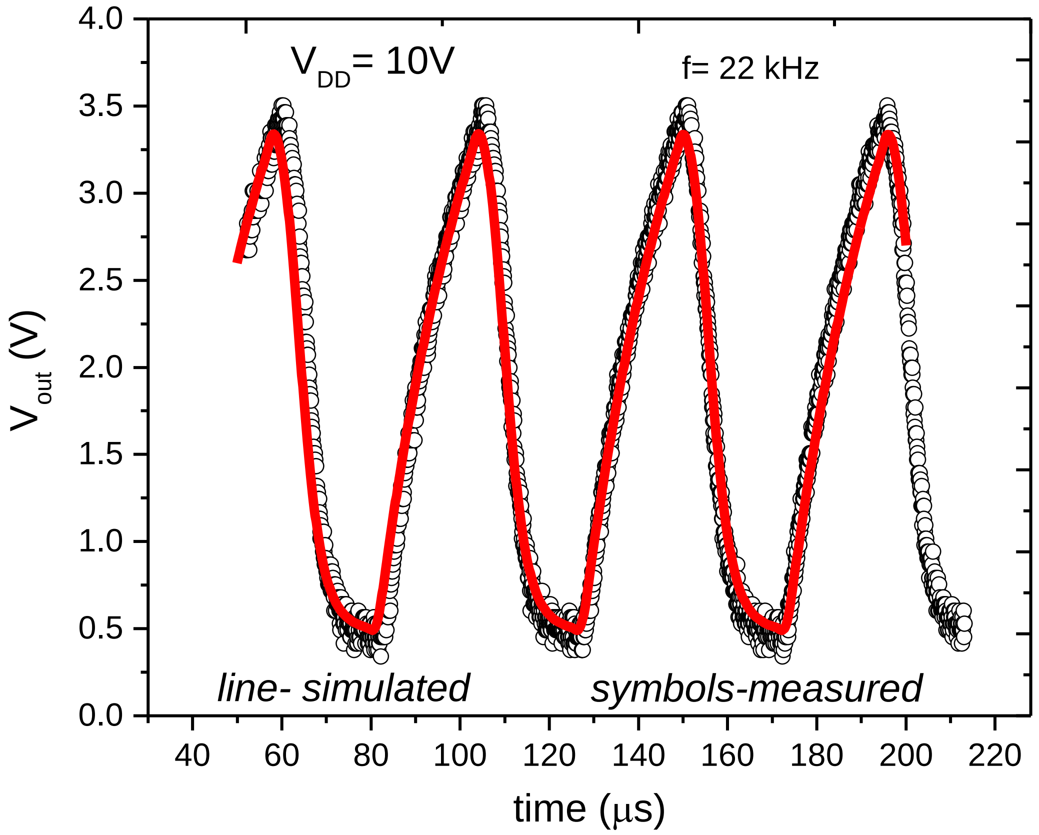
Load TFT - W= 15 µm and L= 15 µm.

Driver TFT - W=150 µm and L= 15 µm.

AOSTFT Ring-oscillator of 19 inverters

Measured oscillation frequency equal to 22 kHz.

The simulated oscillator has an excellent coincidence with the measured oscillator.



CONCLUSIONS

AOSTFT Conclusions - Full transistor model

A new full analytical model for AOSTFTs was developed. It considers internal parameters of the transistors.

The model considers specific features of AOSTFTs, as the top-metal overlap, typical for the bottom gate staggered structure, and DOS of the amorphous material used as semiconductor.

The description of the model in Verilog-A allows the simulation of DC and dynamic characteristics in circuit simulators.

Thanks for your attention